Module 8 : Numerical Relaying I : Fundamentals

Lecture 27 : An Introduction

Objectives

In this lecture, we will learn the following:

- Why Numerical relaying?

- Relay hardware.

  1) Sample and Hold circuit.

     a) Nonsimultaneous Sampling.

     b) Simultaneous Sampling.

  2) Relay Hardware.

  3) Open System relaying.

27.1 Why Numerical Relaying?

The first and foremost driving force for advances in relaying systems is the need to improve *reliability*. In turn, this implies increase in dependability as well as security. This need to improve reliability propelled the development of solid state relays. Solid state relays have inherent *self checking facility* which was not available with electromechanical relays. This feature is also available with numerical relays (fig 27.1). For example, when we boot a computer, it goes through a self checking phase where in it checks RAM, hard disk, etc. Also, with the reduced cost of computer hardware, and an exponential growth in processing capability, numerical relays can provide high performance at moderate costs.

Since, numerical relays are based on digital technology, they are more or less immune to variation or drift in parameters of individual components like OP-AMPS etc. due to changes in temperature, ageing etc. Numerical relays also help in reducing burden (volt-amperes) of Current Transformer (CT) and Voltage Transformer (VT). This is desirable because ideally sensors should not consume any power. If a sensor consumes energy from the measurand, it will automatically distort the signal. This problem is further aggravated in CTs due to non-linearity of iron core. Numerical relays offer very low impedance to the secondary of CT and hence reduce burden on CT.

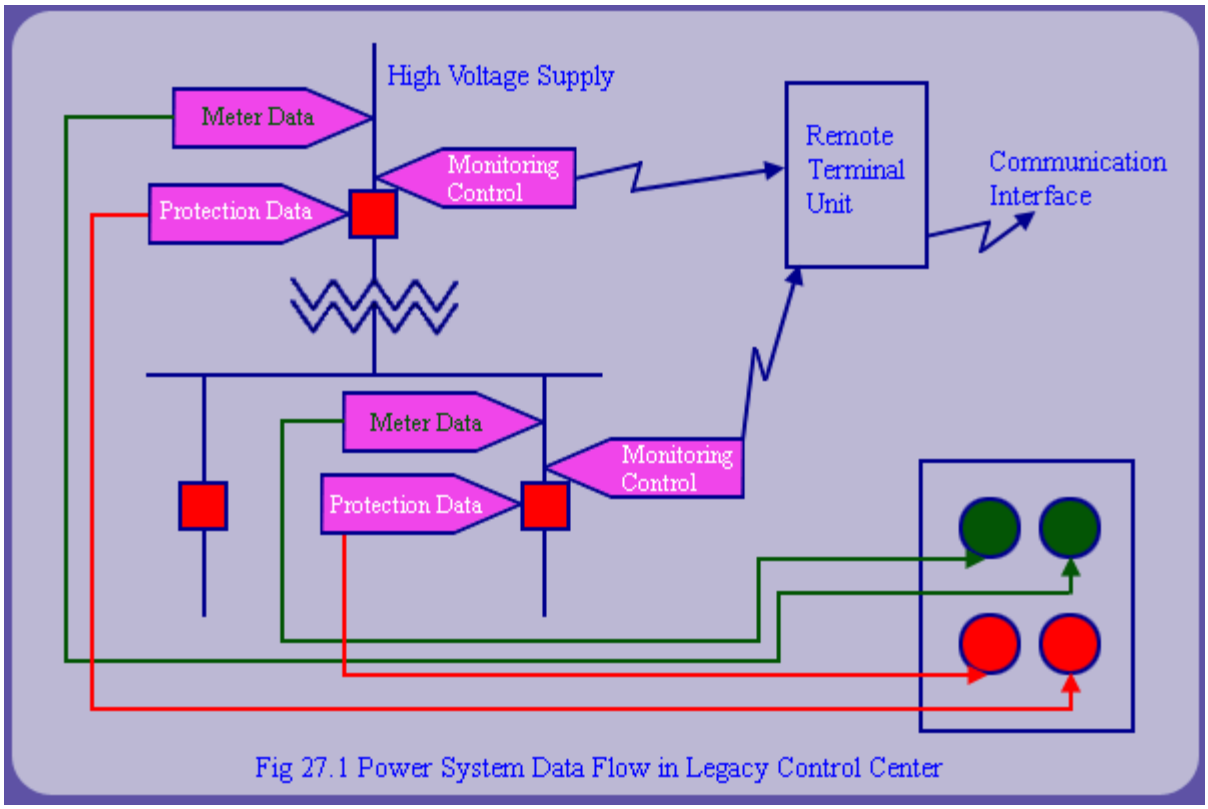

Fig 27.1 Power System Data Flow in Legacy Control Center

27.1 Why Numerical Relaying? (contd..)

Numerical relays permit much more flexibility than their electromechanical and solid state counterparts. In electromechanical relays, the constructional details like magnetic path, air gap etc., are used to design various operating characteristics. Since, solid state relays mainly use analog circuit, they permit more innovation than corresponding electromechanical relays which are no doubt robust. However, solid state relays can not have the kind of *flexibility* that computer aided relaying can have. For example, providing magnitude scaling and phase shift to a voltage signal to generate line to line voltage from phase to neutral voltage is much simpler with computer aided relaying because it can be handled by the program. A *computer relay can be programmed*. Further, due to the programming feature, it is possible to have generic hardware for multiple relays, which reduces the cost of inventory.

Numerical relaying along with developments in fiber optic communication have pioneered development of automated substations. Once, the analog signals from CTs and VTs are digitized, they can be converted to optical signals and transmitted on substation LAN using fiber optic network. With high level of EMI immunity offered by fiber optic cable, it has become the transmission medium by choice in substation environment. Numerical relays can be nicely interfaced with a substation LAN. This in turn should be contrasted with *legacy* substations (fig 27.1) where in lead wires have to run from each CT and VT to the control panel (fig 27.2).This not only reduces wiring complexity in the substation but also reduces burden on the CT as resistances of long lead wires are eliminated. Further, a single fiber optic LAN permits multiplexing of multiple analog signals which is not possible with legacy arrangement.

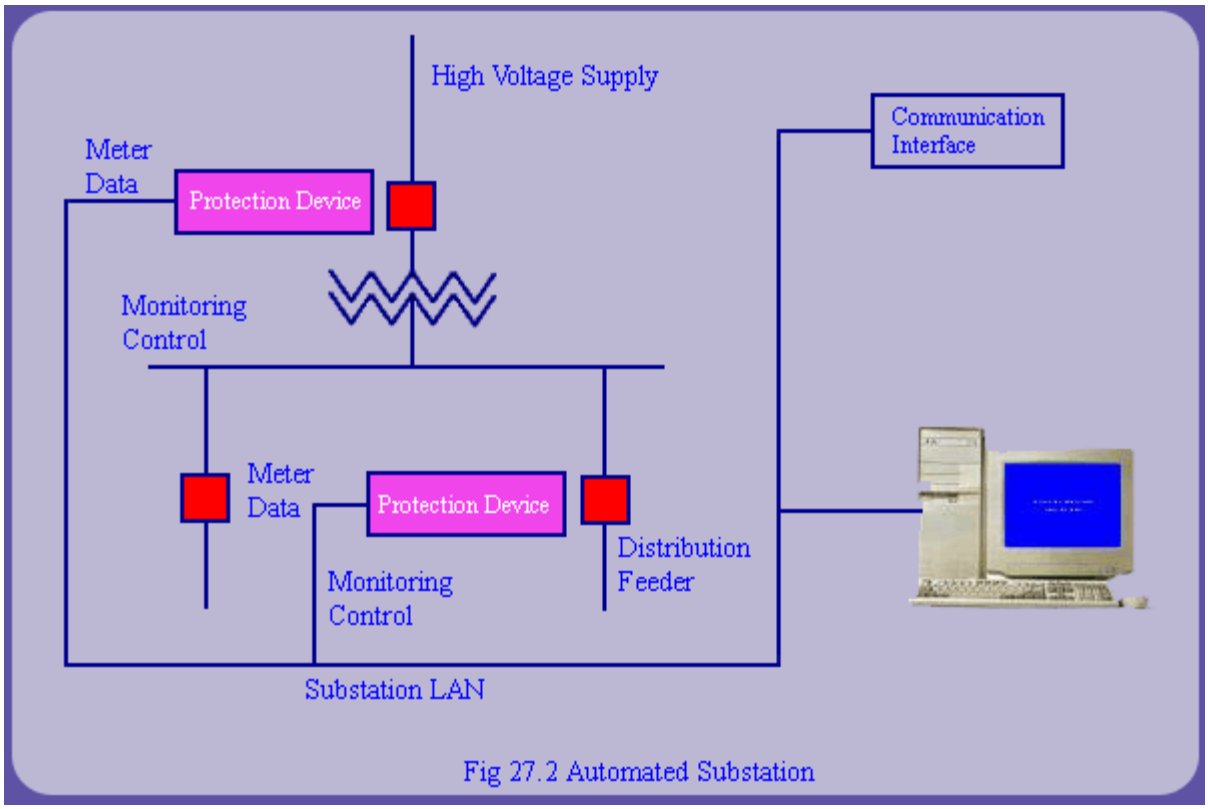

Fig 27.2 Automated Substation

27.1 Why Numerical Relaying? (contd..)

Numerical relays also permit development of new functions as well as development of *adaptive* relaying schemes. Traditionally, relaying systems are designed and set in a conservative manner. They represent compromise between:

- economy and performance
- dependability and security
- complexity and simplicity
- speed and accuracy
- credible and conceivable

Adaptive relaying is meant to minimize such compromises and also allow relays to fine-tune to existing system conditions. Specific adaptive relaying features will be discussed in the later lectures.

Numerical relays also permit storage of pre and post fault data (of the order of few cycles). This data can also be time stamped, now-a-days by Geographical Positioning System (GPS). GPS systems (a cluster of 24 satellites of pentagon, USA) not only provides positional information but also a time pulse every second for synchronization of sampling. Thus, in principle, every sample and every event like closing or opening of breakers can be time stamped. This helps in postmortem analysis which is used to determine whether (1) a relay operated correctly (or incorrectly) and (2) any other relaying system or device (like circuit breaker) has failed to operate. Time stamping of relay operation allows us to capture the sequence of relay operations. Thus, in a complex situation like catastrophic failure of the power system (brown out or black out), it is now possible to precisely determine the sequence of relay operations. This helps engineers to capture and simulate the disturbance using transient stability, (EMTP) programs.

Such simulation studies help in understanding shortcomings of the existing systems and thereby improvising them. In this role, a

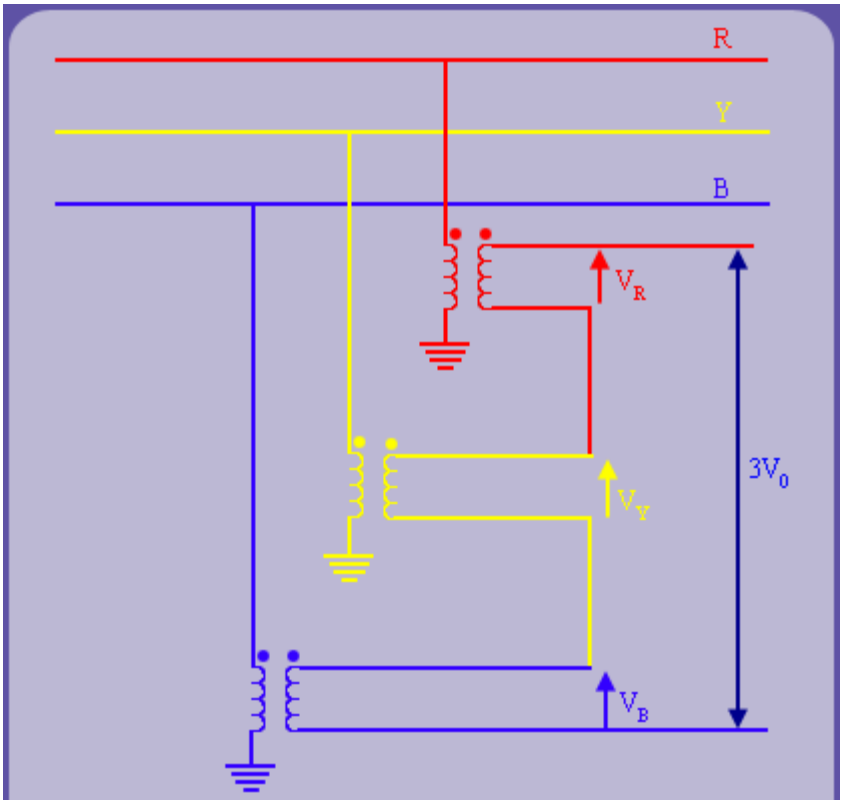

Fig 27.3 Open Delta VT connection

numerical relay is analogous to a fault data recorder (FDR).

Numerical relays also simplify interfacing with CTs and VTs. Consider a protective function which requires zero sequence voltage. Traditionally, it would be generated by open delta VT connection in fig 27.3 If zero sequence current is also required, it is obtained by using an additional CT in the ground wire. With numerical relays, zero sequence voltages and currents can be derived inside the processor from the phase voltage (V_a, V_b, V_c) and line currents (I_a, I_b and I_c).

In differential protection e.g., three phase transformer protection, traditional protection schemes also require additional care to handle polarity, scaling and phase shifting problems. This may even necessiate use of an auxiliary CT.

Such complications can be resolved with ease when numerical relays are used. This aspect will be discussed in more detail in the lectures on transformer protection.

27.2 Relay Hardware

27.2.1 Block Diagram

Fig 27.4 shows the functional block diagram of a digital relay. It can be seen that a digital relay consists of:

- Analog input subsystem
- Digital input subsystem
- Digital output subsystem
- A processor along with RAM (data scratch pad), main memory (historical data file) and power supply.

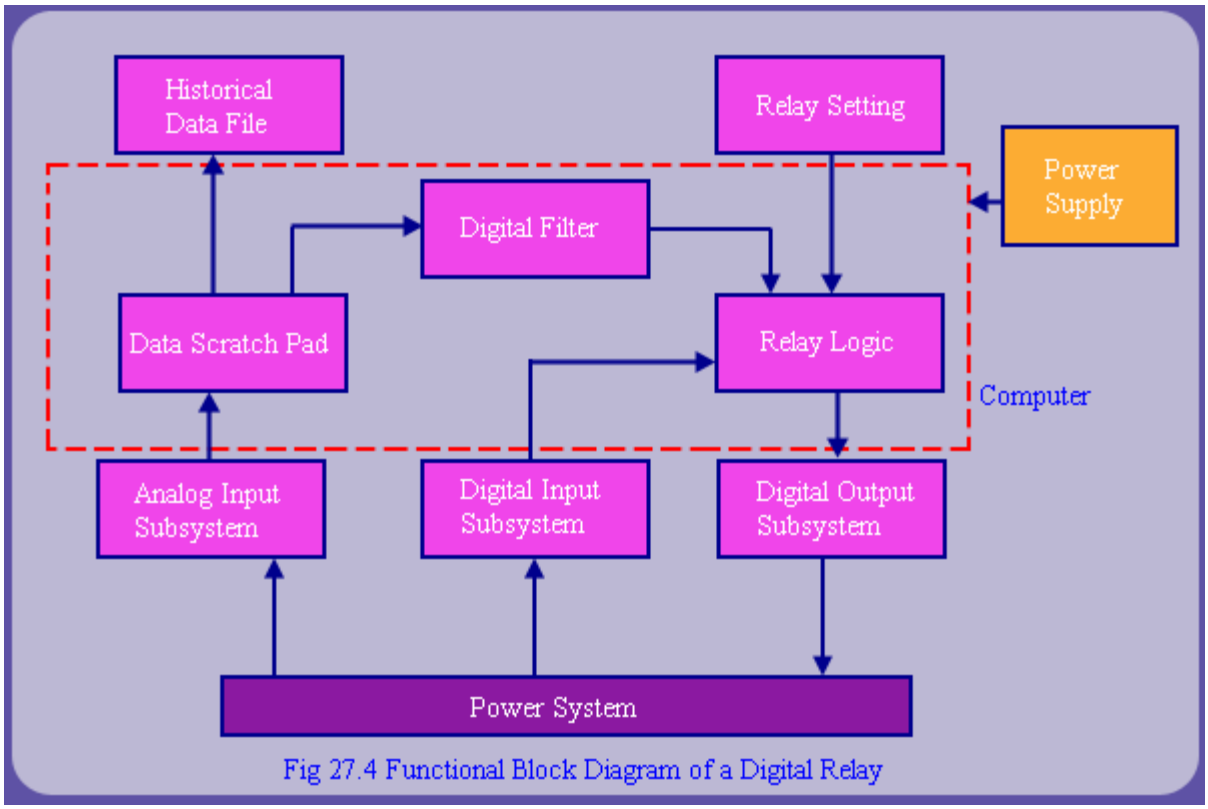

Fig 27.4 Functional Block Diagram of a Digital Relay

The 3-Ø voltage and current signals are analog in nature. Since, a computer works with digital data, analog signals have to be sampled and discretized. Additionally, signal scaling and isolation to protect the low voltage computer system and scale the voltage and current signals to proportionate voltage signal (e.g., within ± 5V) is necessary. This functionality is provided by the analog input subsystem. Typically, it consists of sample and hold circuit, Analog to Digital Converter (ADC) and multiplexer interfaced to the processor. The digital input data consists of Circuit Breaker (CB) status (open or close). The digital output is relay's operate / do not operate decision.

Once, the data is acquired within RAM, it is filtered by a digital filter and processed by the relay logic. The algorithms for extracting phasors and relay logic will be discussed in subsequent lectures.

TOP

27.2 Relay Hardware (contd..)

27.2.2 Analog Input Subsystem

There are two commonly used schemes for configuring the analog input subsystem. One is known as the 'simultaneous' & other 'non-simultaneous' scheme.

27.2.2.1 Non-Simultaneous Sampling Scheme

Fig 27.5 illustrates non-simultaneous sampling scheme. In this scheme, a multiplexer selects the analog channel sequentially. Typically, power system applications involve more than one analog input. To reduce the cost of the hardware, multiple channels are multiplexed through analog multiplexer to a single ADC. An analog multiplexer permits a single output line to mirror the signal at the selected input, say one of the 3 voltages/ 3 currents.

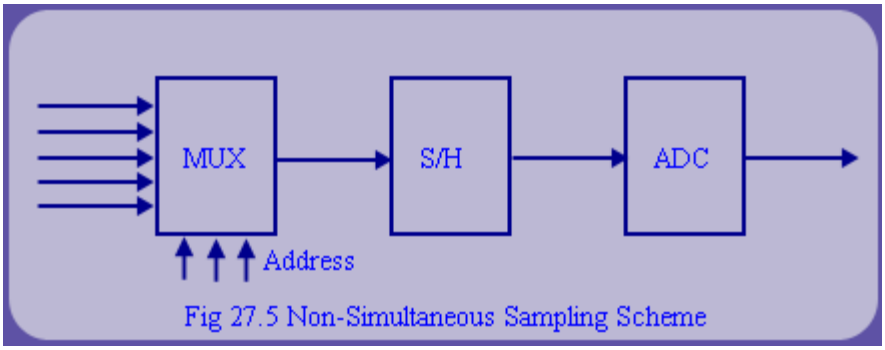

Fig 27.5 Non-Simultaneous Sampling Scheme

Thus, multiplexer is a collection of analog switches. Each channel can be selected by supplying appropriate binary code to the multiplexer e.g. for 8-channel multiplexer, 3 bit address space is required. A chip disable line permits parallel expansion if external logic is used to select desired multiplexer. A multiplexer has two inputs (terminals) for a single channel. It provides better noise immunity. Accuracy of the analog multiplexer depends on load impedance at the output terminal. Typical recommended value is 10^7 to $10^8 \Omega$. As Sample (S) and Hold (H) circuit has impedance in the range 10^8 - $10^{12} \Omega$, no problem is encountered.

27.2 Relay Hardware (contd..)

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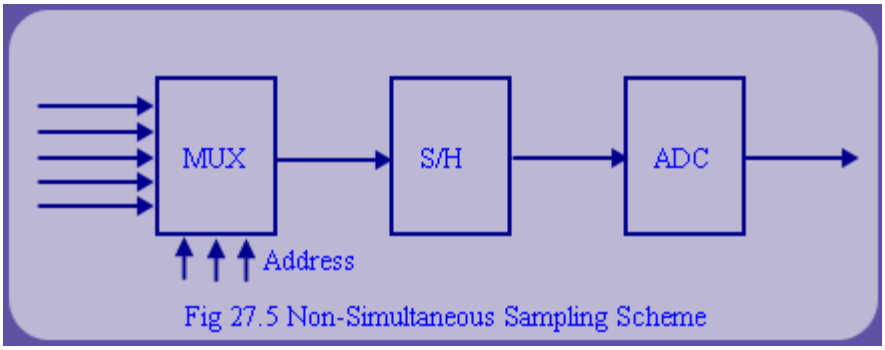

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27.2 Relay Hardware (contd..)

27.2.3 Sample and Hold Circuit

The analog information is held by a Sample and Hold circuit (fig 27.6). Any A/D converter requires a finite conversion time. A S & H circuit which conceptually is a shunt capacitor with a switch holds the information (in terms of voltage). While the conversion takes place, switch is in open position. This is known as the `hold' state. When the switch is closed, the V_{out} of S and H follows the V_{in}.

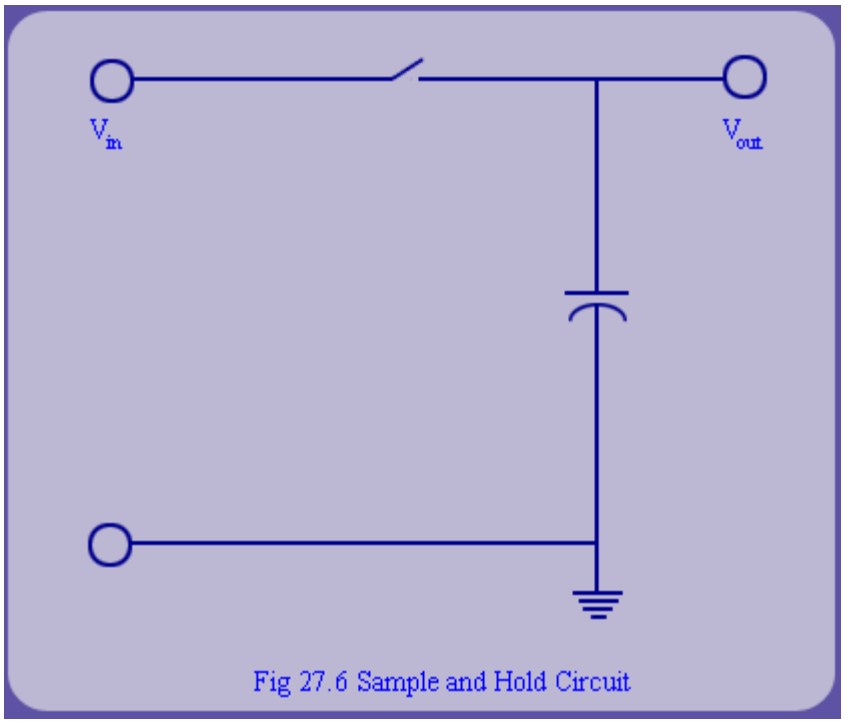

Fig 27.6 Sample and Hold Circuit

In the scheme illustrated in fig 27.5, it can be observed that the relative phasor information between two signals is not preserved.This is because the samples from different inputs are not obtained at same instant of time. One way to overcome, this hardware limitation is to interpolate the value of the sample from previous values.

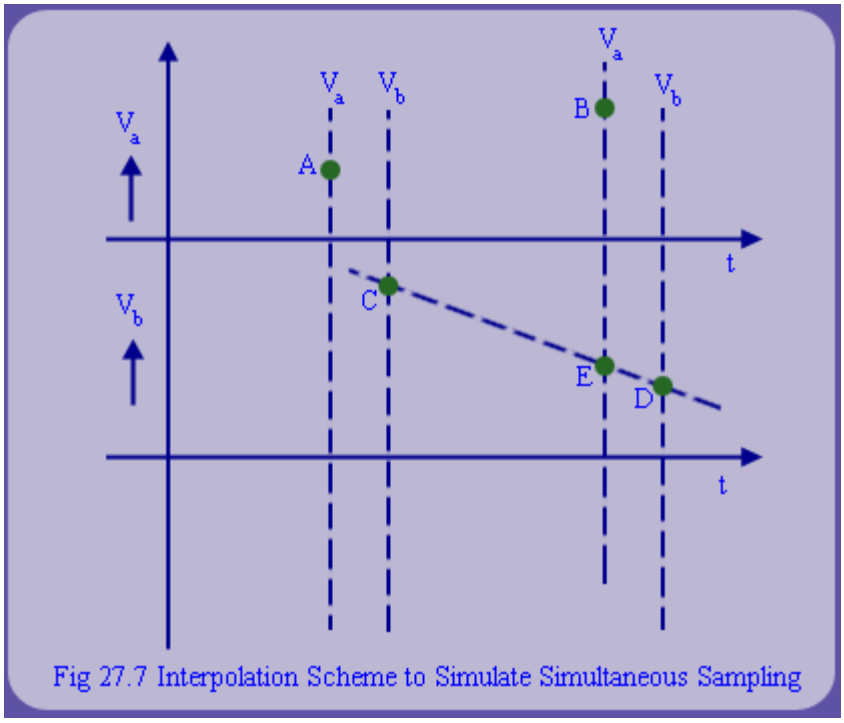

Fig 27.7 Interpolation Scheme to Simulate Simultaneous Sampling

Fig 27.7 illustrates the concept. Let $V_a(t)$ be sampled first and then $V_b(t)$ be sampled. The first two samples of 'a' & 'b' phases are given by points 'A' and 'C'. After one sampling interval, samples 'B' and 'D' are obtained, for phases 'a' and 'b' respectively. The problem is to estimate value of $V_b(t)$ at the sampling instant for 'a' i.e. say at sample 'B'. This can be obtained by linear interpolation for samples 'C' and 'D' and corresponding to point 'E'.

27.2 Relay Hardware

27.2.3Sample and Hold Circuit (contd..)

Simultaneous Sampling Scheme

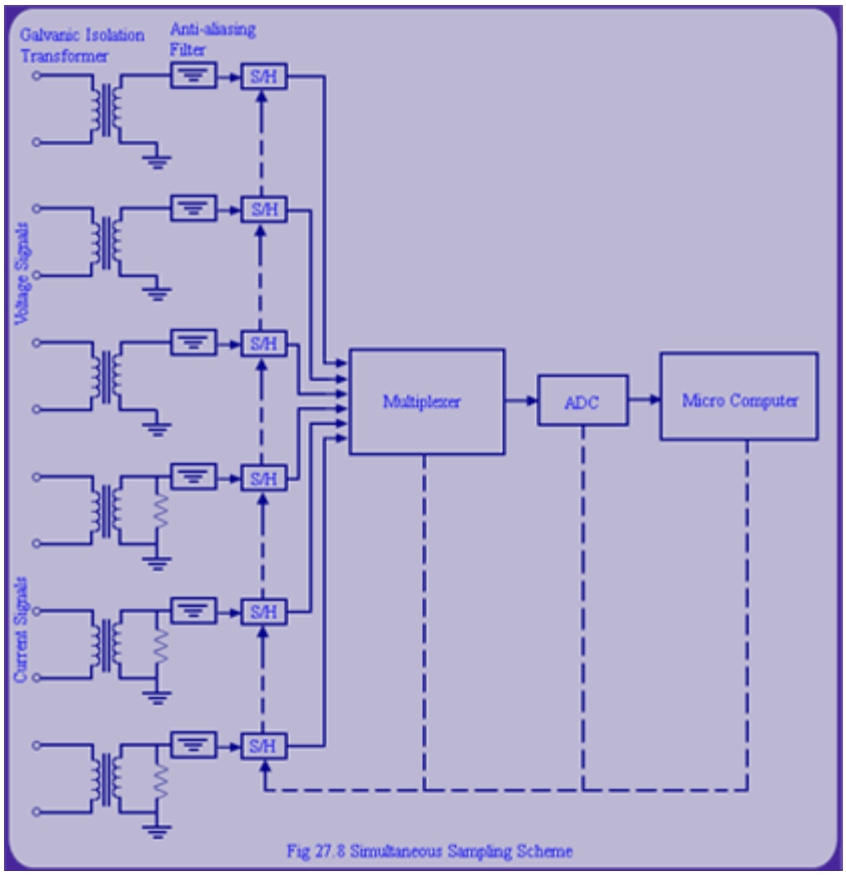

Fig 27.8 shows a simultaneous sampling scheme. In this scheme, all S&H amplifiers are set to hold state simultaneously. This preserves the relative phase information between multiple analog signals.Then, the multiplexer selects the channel sequentially. Typically, digital relays use successive ADC which have a conversion time of 15-30 µs. The sampling rate must satisfy Nyquist criteria. This issue will be discussed in the later lectures.

Finally, an antialiasing filter is used after signal conditioning hardware. Anti aliasing filter is a low pass filter (LPF) used to cut off the high frequency content (including noise) in the input signal. The cutoff frequency of LPF and the sampling rate have to be properly matched. This issue is addressed in later lectures.

27.2 Relay Hardware (contd..)

27.2.4Relaying hardware for Metering

In principle, the hardware setup shown in fig 27.8 can be used for both measurement and protection function. However, considering the order of difference between current magnitudes in case of fault and load, there can be loss of accuracy during metering applications. Consider a hypothetical case where in maximum load current is 100A and maximum fault current is 20 times this load current (2000A). Let a 12 bit unipolar ADC be used for sampling current signal. This implies that resolution of ADC is 2000/(2**12-1)=0.488 A. This resolution may be inadequate for metering purposes. One solution is to increase resolution i.e. the number of bits in ADC. For example, one may use 16 bit ADC in place of 12 bit ADC.

However, increasing the number of bits of ADC also affects the selection of processor. A good design guideline is to choose a processor with double the number of bits of ADC. This ensures that truncation and numerical precision problems associated with finite precsion arithematic do not cause significant loss of accuracy. For example, with 16 bit ADC, 32 bit processor is the natural choice. Alternatively, a variable gain amplifier can be used along with the ADC. At low currents, high gain setting is used and at high currents low gain setting is preferred. However, during the change from one setting to another, loss of information can take place. Therefore, a simple solution would be to keep metering and protection functionality separate.

27.2.5Open System Relaying

Open system relaying motivated by experiences from energy management field where in a plethora of manufacturers specific equipment has led to difficulty in expanding the system without changing the entire existing SCADA (system control and data aquisition) system. Open system movement encourages standard based development, thereby permitting incremental or evolutionary growth. This has to be contrasted with proprietary solutions that required either a complete changeover or force the utility to a vendor.

Consider a case of two vendors (A and B) supplying a Remote Terminal Units (RTUs) to a utility C. Let us consider that initially, the utility had procured the SCADA system from the manufacturer A. At a later date, the utility wants to add RTUs from the vendor B because it has cost and performance benefits. If the initial solution provided by vendor A was proprietory, it will not be possible for RTUs of vendor B to be interfaced with SCADA system supplied by vendor A. This restricts cross migration and hence it is unfair. On the otherhand, if the initial SCADA system was based on open standards, then the device of another vendor using the same standard could be interfaced with ease. This is the basic idea behind any open systems movement. An open relay conceptually consists of two separate 'boxes'. The first box is the well known standard computer. The second box encloses the scalable analog input subsystem. The processing board which may have multiple DSPs is plugged onto PC motherboard and once programmed can run independently of the PC. Such a relay may be interfaced with substaion LAN using standard protocol.

Recap

In this lecture, following important reasons for advocating numerical relays were identified:

- Cost: The processing power measured in Floating Point Operations Per Seconds (FLOPS) has been
- steadily increasing. This is because of the technological advances in VLSI. Today, general purpose as well as high speed Digital Signal Processors (DSP) are available at reasonable cost. As such, cost of numerical relays is competitive with traditional electromechanical and solid state relays.
- Self Checking and Reliability: A numerical relay just like a PC can check the health of its components periodically. In
- case of a failure, it can raise an alarm. No amount of periodic maintenance can provide this facility, which goes a long way in improving the reliability of digital relay.
- System Integration and Digital Environment: There is a trend towards automation in power systems. Transmission
- systems were automated first to improve the reliability of the overall transmission system by use of SCADA and setting up of energy control centers. Today digital electronics has permitted automation at substation level. Substation automation and distribution system automation have brought the digital technology of computation and communication at the lower voltage levels. Numerical relays fit appropriately in such an environment.
- Functional Flexibility and Adaptive Relaying: Numerical relays are programmable. A multi-purpose hardware can be
- programmed with many relaying schemes. The complexity of the relaying logic is limited by the imagination of the relay engineer and the processing capability of the processor. With the emergence of the DSP based numerical relays, it is possible to incorporate a number of features in a relay. Further, such relays can be equipped with communication facilities thereby, opening the possibility of adaptive relaying.

Congratulations, you have finished Lecture 27. To view the next lecture select it from the left hand side menu of the page