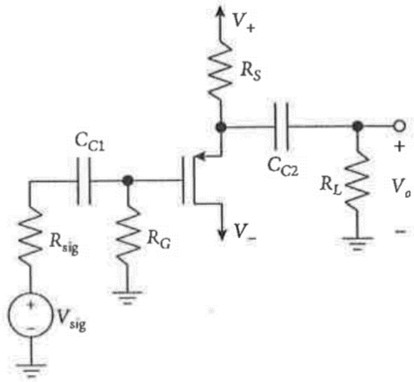
Lab 5.12 – A PMOS Source Follower

In this lab we are going to use a PMOS transistor (take care, the Multisim symbol for a PMOS device is confusing) and build a "Common Drain" amplifier (AKA a Source Follower). It is called a Source follower since that describes its behavior, the source (output) AC voltage is always approximately equal (there is a DC offset due to the Device threshold voltage) to the Gate AC voltage.



Notes:

- R_{sig} is the output impedance of the AC signal generator which is 50 ohms for the function generator on our lab bench so do not put a physical source resistor in your actual circuit.
- The capacitors are there to block DC and at audio frequencies should have a negligible reactance.
- V_+ and V_- (15 volts) are ideally at AC ground

As with any design, you first select the resistors to put the transistor at a reasonable operating point. Then draw the AC (small signal) version of the circuit (capacitors are short circuits and the power rails are AC grounds and replace the PMOS device by a small signal model (see your Text) to calculate the voltage gain (approximately 1), input impedance (approximately R_G, and output impedance (very low – ignore R_L).

The source follower is an effective "Buffer Amplifier" to isolate your signal source from the load.

- It will not "load" the signal source (high input impedance)
- The output "follows" the input (unity voltage gain)
- The output voltage is almost independent of the load resistance (low output impedance)

Most of these characteristics are due to a high degree of negative feedback in this circuit. Note that the input to the transistor is V_{gs} which is the input voltage minus the output voltage and the feedback gain is high due to the transistor gain.

LAB 5.12

PMOS Source Follower

(See Section 5.8.5, p. 321 of Sedra/Smith)

OBJECTIVES:

To study a PMOS-based source follower by:

- Completing the DC and small-signal analysis based on its theoretical behavior.
- Simulating it to compare the results with the paper analysis.
- Implementing it in an experimental setting, taking measurements, and comparing its performance with theoretical and simulated results.
- Qualitatively seeing the impact of transistor-to-transistor variations.

MATERIALS:

- Laboratory setup, including breadboard
- 1 enhancement-type PMOS transistor (e.g., MC14007)
- 3 large (e.g., 47-μF) capacitors
- Several resistors of varying sizes
- Wires

PART 1: DESIGN AND SIMULATION

Consider the circuit shown in Figure L5.12:

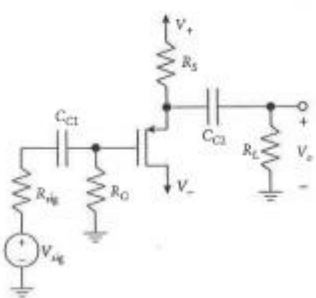


FIGURE L5.12: Source follower circuit, with coupling capacitors, and resistor R_G for DC-biasing purposes. Based on Fig. 5.60 p. 321 S&S.

Design the amplifier such that $I_D = 2$ mA. Use supplies of $V_+ = -V_- = 15$ V, $R_{sig} = 50\ \Omega$, and $R_G = 10\ \text{k}\Omega$. What is the minimum value of R_L that satisfies the requirements? Obtain the datasheet for the PMOS transistor that will be used. In your lab book, perform the following.

DC Operating Point Analysis

- Sketch a DC model of the circuit in your lab book, replacing the large-valued coupling capacitors C_{C1} and C_{C2} by open circuits (for simplicity you may also omit v_{sig}, R_{sig}, and R_L). What is the DC current through R_G?
- Based on the required value of I_D, what is $V_{OV} = V_{SG} - |V_{tp}|$? What value of R_S must you use?

AC Analysis

- Sketch a small-signal model of the circuit in your lab book, replacing the transistor with its small-signal model (try a T model, ignoring r_o), replacing the capacitors with short circuits, and replacing V_+ and V_- with an AC ground. Label the gate of the transistor as v_i, i.e., the small-signal voltage at the input.
- What is the ratio of v_i/v_{sig}? How would you approximate it in further calculations?
- Derive an expression for $A_v = v_o/v_i$.
- What is the value of g_m? What is A_v?
- What is the minimum value of R_L that satisfies the design requirements?
- Calculate the output resistance of your amplifier.

Simulation

- Simulate the performance of your circuit. Use capacitor values $C_{C1} = C_{C2} = 47\ \mu$F and the value of R_S based on your preceding calculations. Use a 10-$\text{mV}_{\text{pk-pk}}$, 1-kHz sinusoid with no DC component applied at v_{sig}.
- From your simulation, report the DC values of V_{SG}, V_{SD}, and I_D. How closely do they match your calculations? (Remember: The simulator has its own, more complex model of the real transistor, so there should be some small variations.)
- From your simulation, report A_v. How closely does it match your calculations?

PART 2: PROTOTYPING

- Assemble the circuit onto your breadboard using the specified component values and those just calculated. Note that R_{sig} represents the output resistance of the function generator, and therefore you should *not* include it in your circuit.

PART 3: MEASUREMENTS

- *DC bias point measurement*: Using a digital multimeter, measure the DC voltages of your circuit at the gate (V_G) and source (V_S) of your transistor.

- *AC measurement*: Using a function generator, apply a 10-mV_{pk-pk}, 1-kHz sinusoid with no DC component to your circuit. (*Note*: Some function generators only allow inputs as small as 50 mV_{pk-pk}. If this is the case, use that value instead.)
- Using an oscilloscope, generate plots of v_o and v_i vs. t.
- Using a digital multimeter, measure all resistors to three significant digits.

PART 4: POST-MEASUREMENT EXERCISE

- Calculate the values of V_{SG} and V_{SD} that you obtained in the lab. How do they compare to your pre-lab calculations? Explain any discrepancies.
- Based on the measured values of V_D and V_S, and your measured resistor values, what is the real value of I_D based on your lab measurements?
- What is the measured value of A_v? How does it compare to your pre-lab calculations? Explain any discrepancies.
- What would happen if you used the function generator with 50-Ω output resistance to directly drive your load resistor? What gain would you get? What would happen if the output resistance of the function generation was changed from 50 Ω to 5 kΩ? What do you conclude? Recall the value of output resistance you calculated earlier.
- *Hint*: The single biggest source of variations from your pre-lab simulation results will be due to variations in the transistor's threshold voltage V_{tp}. Remember: Its value will be somewhere within the range indicated on the transistor's datasheet.

PART 5 [OPTIONAL]: EXTRA EXPLORATION

- Add a 500-Ω resistor between the function generator output and capacitor C_{C1}. How does the gain of your circuit change? Can you explain this?