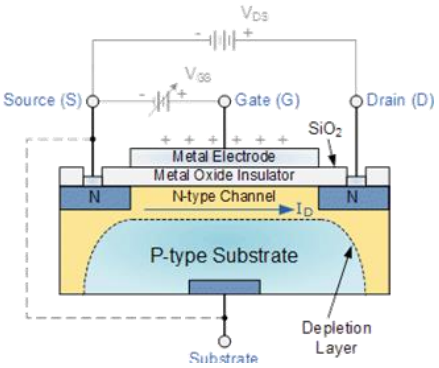
Lab 5.5 – NMOS Common Source Amplifier

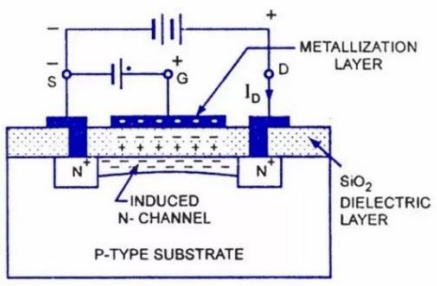
What is a MosFet?

A MosFet is a simple semiconductor device. Here is a "Depletion Mode" NMOS transistor.



As the Gate voltage goes negative with respect to the source, the carriers in the "Channel" get pushed away and the channel gets thinner which reduces the Drain to Source current. The substrate is kept at a low voltage so that the PN junction is reverse biased to isolate the device from the substrate.

Our NMOS transistors are "Enhancement Mode" Devices:



Operation of N-Channel E-MOSFET

Here the gate is raised positive with respect to the source. At some "threshold" voltage level enough carriers (electrons) are attracted to the region under the gate to create a conductive "Channel".

The Three Basic Configurations

There are three basic NMOS amplifier configurations (the word "common" relates to which terminal is maintained closest to AC ground):

1. Common Source where the input is the gate voltage and the output is the Drain voltage. This is the most often used analog NMOS amplifier configuration as it can have a high voltage gain and a reasonable output impedance.
2. Common Drain where the input is again the gate voltage and the output is the Source voltage. This circuit has a voltage gain that is close to unity, but the output impedance is very low.
3. Common Gate where the input is the source voltage and the output is the Drain voltage. This configuration is rarer than the other two but has an advantage at high frequencies since it isolates the input circuit from the output circuit better than the other two configurations.

Transistor Circuit analysis

Note that analyzing/designing a transistor circuit has two separate steps:

1. Biasing the transistor into a useful operating point (AKA the "Quiescent" or Q point) so that it is in an "active region". For a MosFet, this is where the characteristic curves are almost horizontal (AKA "Saturation")
2. Develop the "small signal" AC model of your circuit (this ignores the DC voltages and currents)
    a. Redraw the circuit shorting out all the bypass/coupling capacitors and treat the power supplies as AC ground. This is your AC model of the circuit.
    b. Now replace the transistor with a suitable small signal equivalent circuit and do some simplifications. You can now do a classical AC circuit analysis on your amplifier.

Some Things to Try in This Experiment

- Measure your amplifier distortion with a distortion analyzer (Elvis and Multisim each have one). The input signal has to be at 1000 Hz as the distortion analyzer filters out the 1000 Hz signal and looks at the remaining energy in the output to determine the (total signal)/(noise plus distortion) ratio.
- Make a point of splitting the source resistor into two resistors (one small, the other large) in series and only bypass the larger resistor. This provides some negative feedback in your circuit and should allow a higher output voltage with low distortion at the cost of lower gain. Note that the gain becomes approximately the reciprocal of the percentage of feedback provided.

Many of my patents involve the use of feedback to produce circuits that have very predictable performance despite large variation in component tolerances.

LAB 5.5

NMOS Common-Source Amplifier

(See Section 5.8.2, p. 316 of Sedra/Smith)

OBJECTIVES:

To study an NMOS-based common-source (CS) amplifier by:

- Completing the DC and small-signal analysis based on its theoretical behavior.
- Simulating it to compare the results with the paper analysis.
- Implementing it in an experimental setting, taking measurements, and comparing its performance with theoretical and simulated results.
- Measuring its output resistance.
- Qualitatively seeing the impact of transistor-to-transistor variations.

MATERIALS:

- Laboratory setup, including breadboard
- 1 enhancement-type NMOS transistor (e.g., MC14007)
- 3 large (e.g., 47-μF) capacitors
- Several resistors of varying sizes
- Wires

PART 1: DESIGN AND SIMULATION

Consider the circuit shown in Figure L5.5:

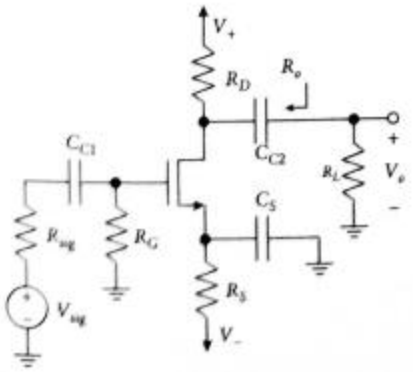


FIGURE L5.5: Common-source amplifier circuit, with coupling capacitors, and resistor R_G for DC-biasing purposes. Based on Fig. 5.57 p. 317 S&S.

Design the amplifier to achieve a small-signal gain of at least $A_v = -5$ V/V. Use supplies of $V_+ = -V_- = 15$ V, $R_{sig} = 50\ \Omega$, $R_L = 10\ k\Omega$, $R_G = 10\ k\Omega$, and design the circuit to have $I_D = 1$ mA. Obtain the datasheet for the NMOS transistor that will be used. In your lab book, perform the following:

DC Operating Point Analysis

- Sketch a DC model of the circuit in your lab book, replacing the three "large-valued" coupling capacitors C_{C1}, C_{C2}, C_S by open circuits (for simplicity you may also omit v_{sig}, R_{sig}, and R_L). What is the DC current through R_G?
- Based on the information just given, you have enough information to calculate $V_{OV} = V_{GS} - V_{tn}$. What is its value? What is the value of g_m? What is V_{GS}? Remember: Your actual transistor will have a value of V_{tn} that will vary from its nominal value, which will alter your measurement results slightly!
- Calculate r_o.
- You now have enough information to calculate R_S. Show your calculations. Is the value you calculate for R_S available in your kit? Can you achieve this value by combining several resistors? Comment.
- *Note*: At this stage we know neither V_{DS} nor R_D.

AC Analysis

- Sketch a small-signal model of the circuit in your lab book, replacing the transistor with its small-signal model, replacing the capacitors with short circuits (what happens to R_S?), and replacing V_+ with an AC ground. What happens to V_-? Label the gate of the transistor as v_i, i.e., the small-signal voltage at the input.
- What is the ratio of v_i/v_{sig}? How would you approximate it in further calculations?
- Derive an expression for $A_v = v_o/v_i$. What is the value of R_D that produces a small-signal voltage gain of *at least* $A_v = -5$ V/V? Is the value you calculated for R_D available in your kit? Can you achieve this value by combining several resistors? Comment.
- What is the DC voltage at the drain? Does this satisfy the assumption that the transistor should be operating in the saturation region? Explain.
- What is the output resistance, R_o?

Simulation

- Simulate your circuit. Use capacitor values $C_{C1} = C_{C2} = C_S = 47\ \mu$F, and the values of R_S and R_D based on your preceding calculations. Use a 10-mV_{pk-pk}, 1-kHz sinusoid with no DC component applied at v_{sig}.
- From your simulation, report the DC values of V_{GS}, V_{DS}, and I_D. How closely do they match your calculations? (Remember: The simulator has its own more-complex model of the real transistor, so there should be some small variations.)
- From your simulation, report A_v. How closely does it match your calculations?

PART 2: PROTOTYPING

- Assemble the circuit onto your breadboard using the specified component values and those just calculated. Note that R_{sig} represents the output

resistance of the function generator, and therefore you should *not* include it in your circuit.

PART 3: MEASUREMENTS

- *DC bias point measurement*: Using a digital multimeter, measure the DC voltages of your circuit at the gate (V_G), source (V_S), and drain (V_D) of your transistor.
- *AC measurement*: Using a function generator, apply to your circuit a 10-mV_{pk-pk}, 1-kHz sinusoid with no DC component. (*Note*: Some function generators allow only inputs as small as 50 mV_{pk-pk}. If this is the case, use that value instead.)
- Using an oscilloscope, generate plots of v_o and v_i vs. t.
- *Output resistance* R_o: Replace R_L with a 1-MΩ resistor and repeat the AC measurement. What is the amplitude of the output waveform? Adjust R_L until you find a value such that the amplitude of the output waveform is approximately 50% of what it was for the 1-MΩ load. This new value of R_L is the output resistance R_o. How does it compare to the value you calculated earlier in Step 2? *Hint*: It cannot be greater than the value of R_D.
- *Further exploration*: What happens to the shape of the output signal as you increase the amplitude of the input signal, e.g., to 1 V_{pk-pk}? At what input amplitude do you begin to see significant distortion? Can you explain this?
- Using a digital multimeter, measure all resistors to three significant digits.

PART 4: POST-MEASUREMENT EXERCISE

- Calculate the values of V_{GS} and V_{DS} that you obtained in the lab. How do they compare to your pre-lab calculations? Explain any discrepancies.
- Based on the measured values of V_D and V_S and your measured resistor values, what is the real value of I_D based on your lab measurements?
- What is the measured value of A_v? How does it compare to your pre-lab calculations? Explain any discrepancies.
- *Hint*: The single biggest source of variations from your pre-lab simulation results will be due to variations in the transistor threshold voltage V_{tn}. Remember: Its value will be somewhere within the range indicated on the transistor datasheet.

PART 5 [OPTIONAL]: EXTRA EXPLORATION

- Instead of tying R_G to ground, try tying it to the drain terminal of the transistor. Repeat the DC bias point measurement and the small-signal gain measurement. What has changed? Do R_D and R_S need to be altered to meet design specifications?