NMOS vs. NPN: Common-Source/ Common-Emitter Amplifier Comparison

OBJECTIVES:

To compare MOS- and BJT-based amplifiers by:

- Building and characterizing an NMOS-based common-source (CS) amplifier.
- Replacing the NMOS transistor with an NPN transistor and recharacterizing the new common-emitter (CE) circuit.

MATERIALS:

- Laboratory setup, including breadboard
- 1 enhancement-type NMOS transistor (e.g., MC14007)
- 1 NPN transistor (e.g., NTE2321)
- 3 large (e.g., 47-μF) capacitors
- Several resistors of varying sizes
- Wires

Consider the two circuits shown in Figure L6.13. Note the structural similarity between the two circuits.

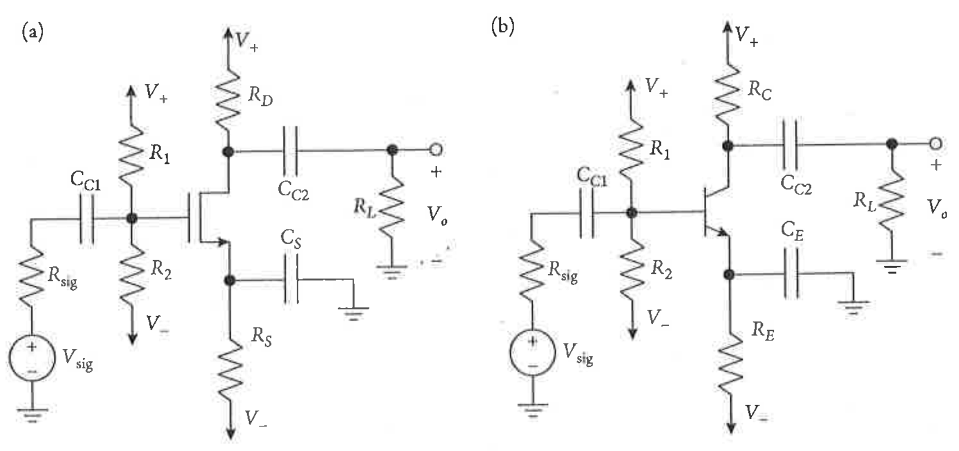

FIGURE L6.13: (a) NMOS common-source amplifier, and (b) NPN common-emitter amplifier.

PART 1: CS DESIGN AND MEASUREMENT

Hand calculations

Design the CS amplifier in Fig. L6.13(a) to achieve a small-signal gain of at least $A_v = -5$ V/V. Use supplies of $V_+ = -V_- = 15$ V, $R_{sig} = 50\ \Omega$, $R_L = 10\ k\Omega$, and $R_1 \| R_2 = 10\ k\Omega$, and design the circuit to have $I_D = 1$ mA and a DC voltage at the gate $V_G = 0$ V. Use $C_{C1} = C_{C2} = C_S = 47\ \mu F$. What is the expected DC voltage at the source of the NMOS?

Simulations

Simulate the performance of your circuit. Use a 10-mV_{pk-pk}, 1-kHz sinusoid with no DC component applied at v_{sig}. Report the DC value of V_S. What is A_v?

Prototyping

Assemble the circuit onto your breadboard using the specified component values and those just calculated. Once more, R_{sig} represents the output resistance of the function generator, and therefore you should *not* include it in your circuit.

Measurements

Using a digital multimeter, measure the DC voltages of your circuit at the gate (V_G), source (V_S), and drain (V_D) of your transistor. Then, using a function generator, apply a 50-mV_{pk-pk}, 1-kHz sinusoid with no DC component to your circuit. Using an oscilloscope, generate plots of v_i and v_i vs. t. What is A_v?

PART 2: CE DESIGN AND MEASUREMENT

Hand calculations

Consider the CE amplifier in Fig. L6.13(b). The main difference from the CS amplifier is that we have replaced the NMOS transistor by an NPN transistor (and changed some of the notation!).

Setting $R_E = R_S$, $R_C = R_D$, and $C_E = C_S$, and keeping $V_E = V_S$ (use your measured value) and $I_D = I_E$, what DC voltage V_B do you require at the base of the NPN transistor? (*Hint*: An active NPN transistor has a base-emitter voltage of approximately 0.7 V). What new values of R_1 and R_2 do you need to use to achieve this value of V_B while keeping $R_1 \| R_2 = 10\ k\Omega$? Since $I_B \neq 0$, you will need to derive the Thévenin equivalent circuit.

Simulation

Simulate the common-emitter circuit using the earlier values (including the new values of R_1 and R_2). What is the voltage gain of the new circuit? What are V_B, V_C, and V_E? How do they compare to V_G, V_D, and V_S in the CS circuit?

Prototyping

Assemble the new circuit onto your breadboard using the specified component values and those just calculated. You should be able just to replace the NMOS with an NPN transistor, and replace R_1 and R_2 with their new values.

Measurements

Using a digital multimeter, measure the DC voltages of your circuit at the base (V_B), emitter (V_E), and collector (V_C) of your transistor. Then, using a function generator, apply a 50-mV_{pk-pk}, 1-kHz sinusoid with no DC component to your circuit. Using an oscilloscope, generate plots of v_o and v_i vs. t. What is A_v?

PART 3: COMPARISON

List all the similarities and differences you can think of between the two amplifiers.