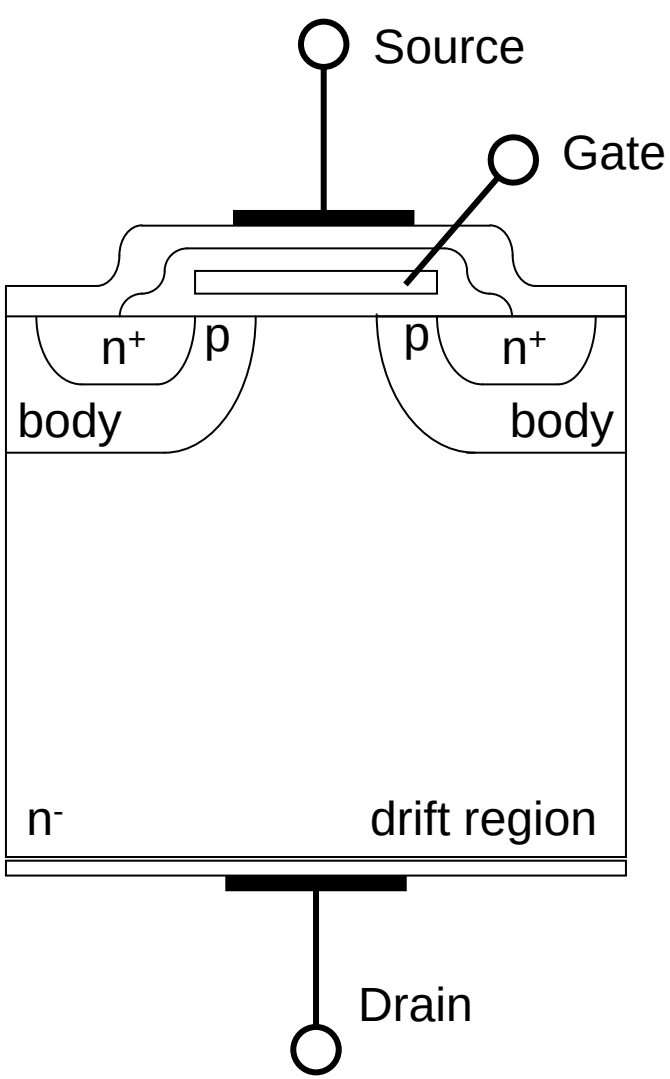
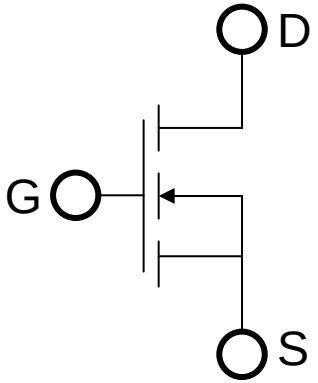
MOSFET

The MOSFET

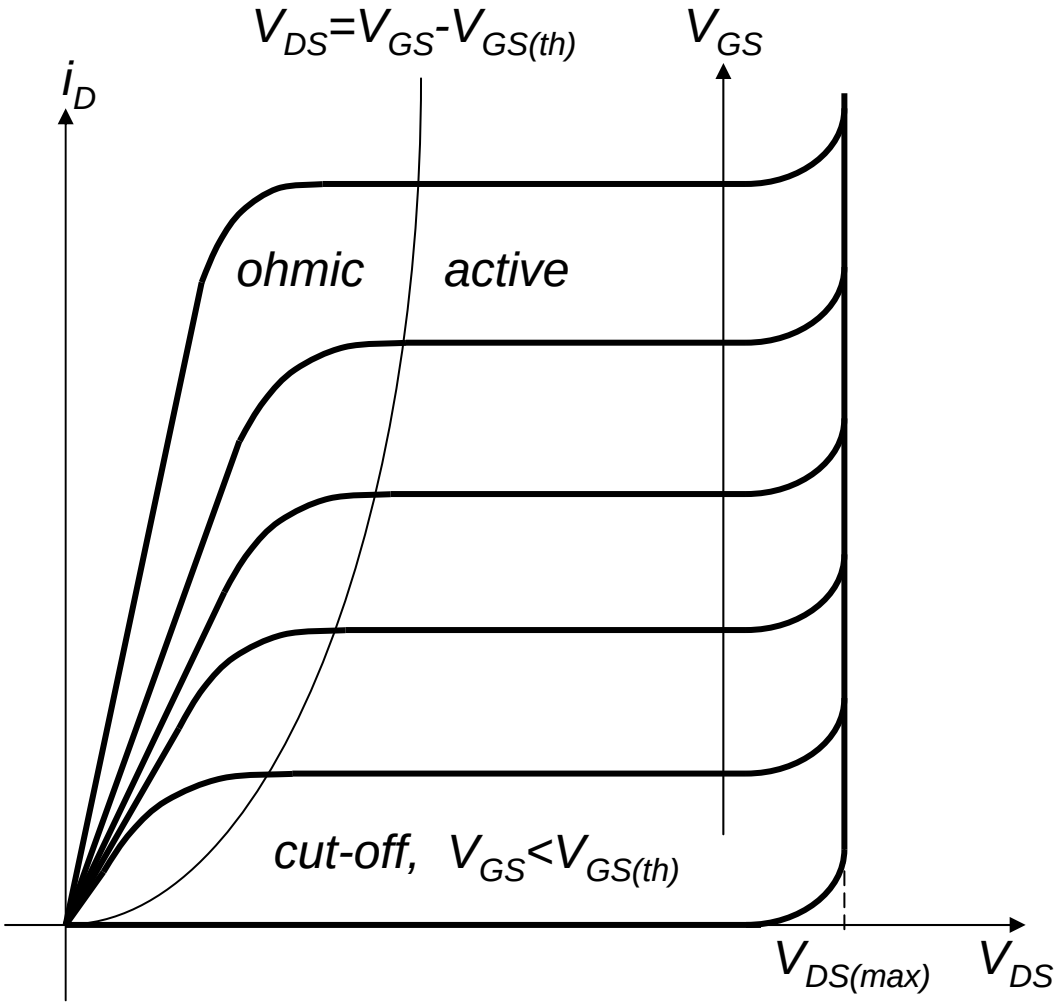




Diffusion structure

- A real power MOSFET consists of thousands of such cells
- It is in the p-doped region, the ”body”, where the channel is formed
- There is always one reversed biased pn-junction, so the conduction is not based on minority carrier injection
- A small signal MOSFET can either be operating in *normally on* or *normally off.* A power MOSFET operates in *normally off*

MOSFET output characteristic



Cut off region

- The gate source voltage is lower than the threshold voltage $V_{GS}<V_{GS(th)}$(3-5 V)

- The MOSFET must block the applied DRAIN-SOURCE voltage, which must be lower than the maximum, the breakdown, DRAIN-SOURCE voltage $V_{DS}<V_{DS(max)}$ to avoid avalanche

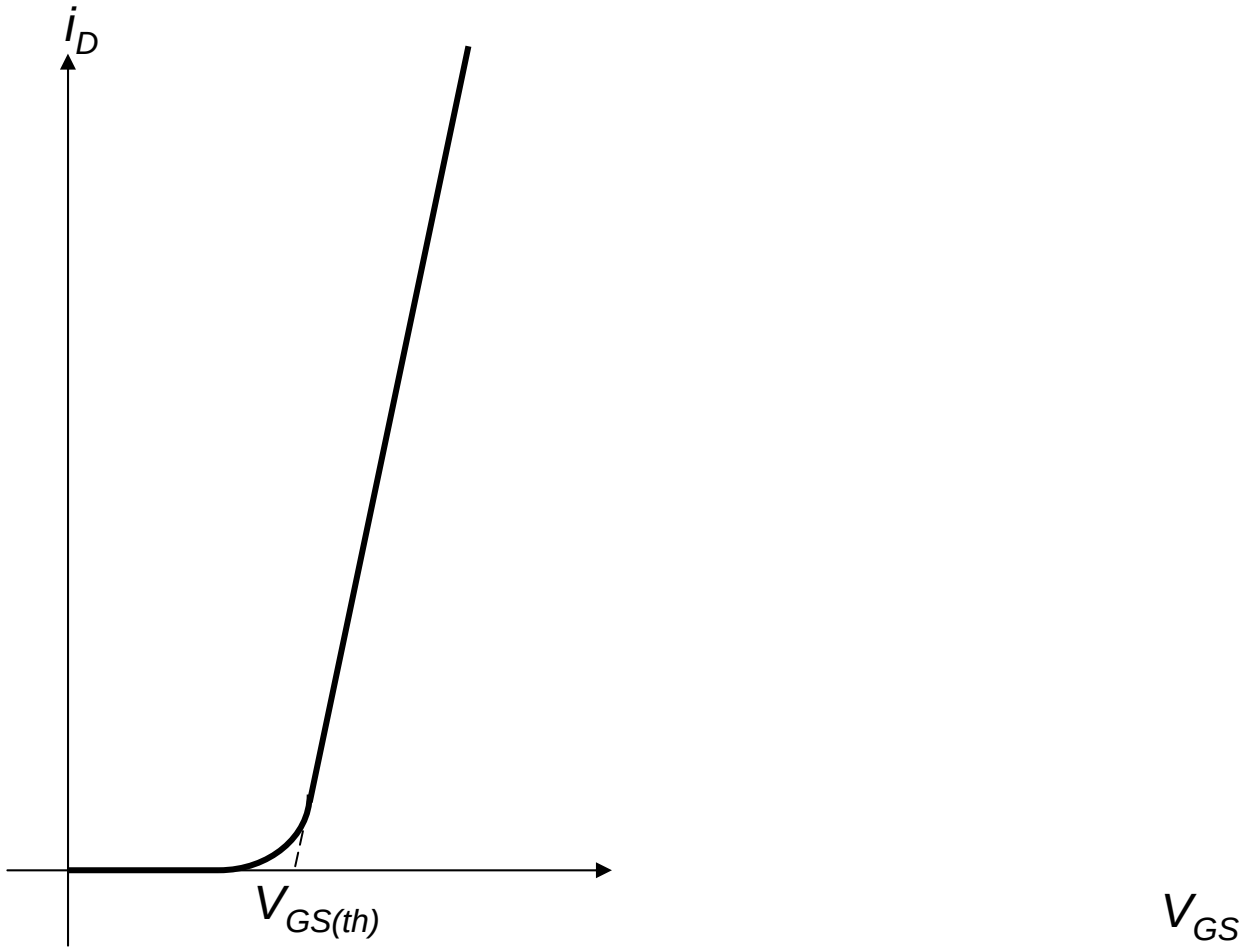
Active region

- The gate source voltage is higher than the threshold voltage $V_{GS}>V_{GS(th)}$
- The drain current is independant of the applied drain source voltage
  (sometimes called the saturation region)
- The drain current is determined by the applied gate-source voltage and is proportional to the squared difference between the applied gate source voltage and its threshold

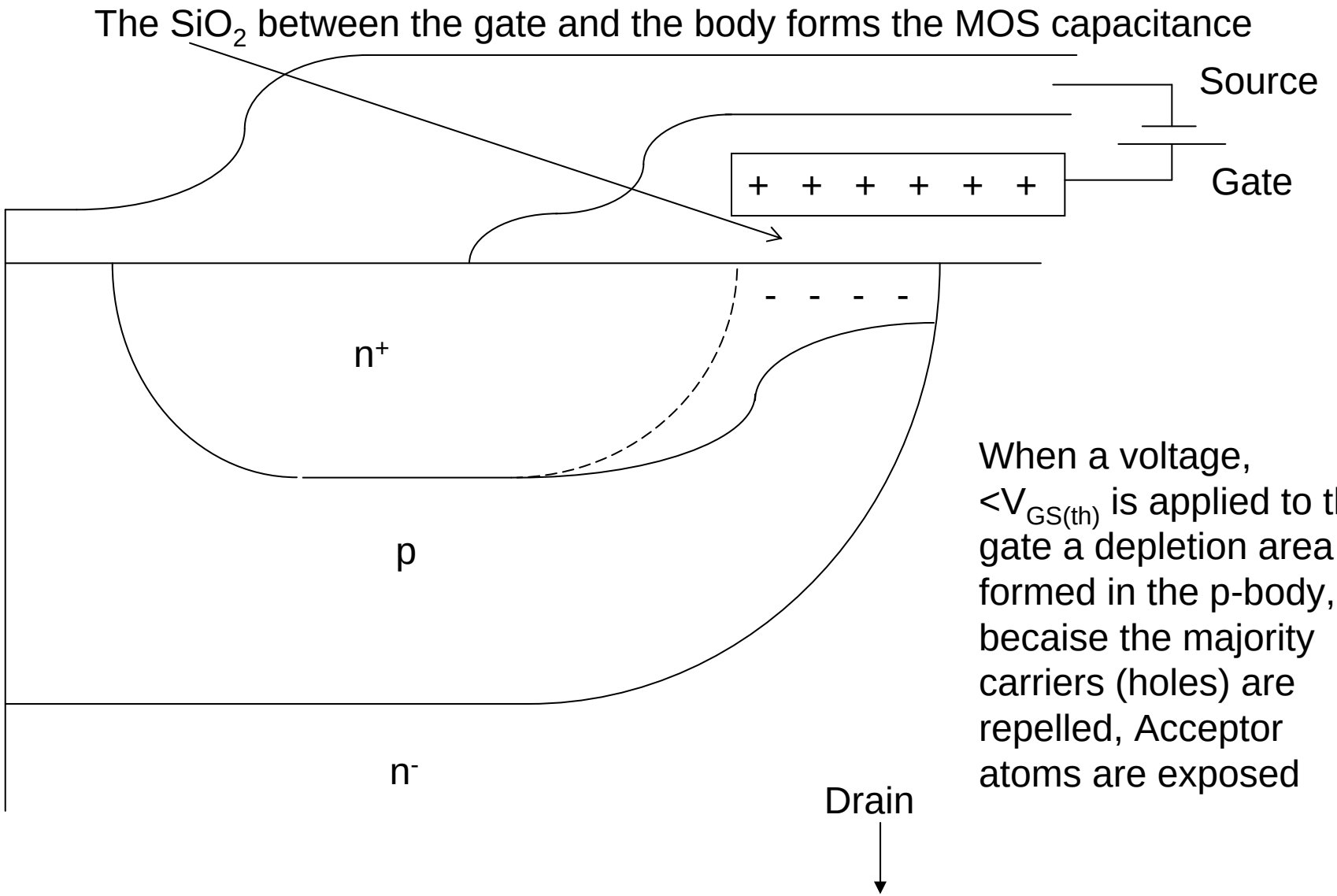
The ohmic region

- The drain current is proportional to and not independant the drain source voltage (resistive)
- This resistance is determined by the geometrical size and the conductivity of the drift region
- It can be compared with the saturation area in a bjt

MOSFET transfer characteristic

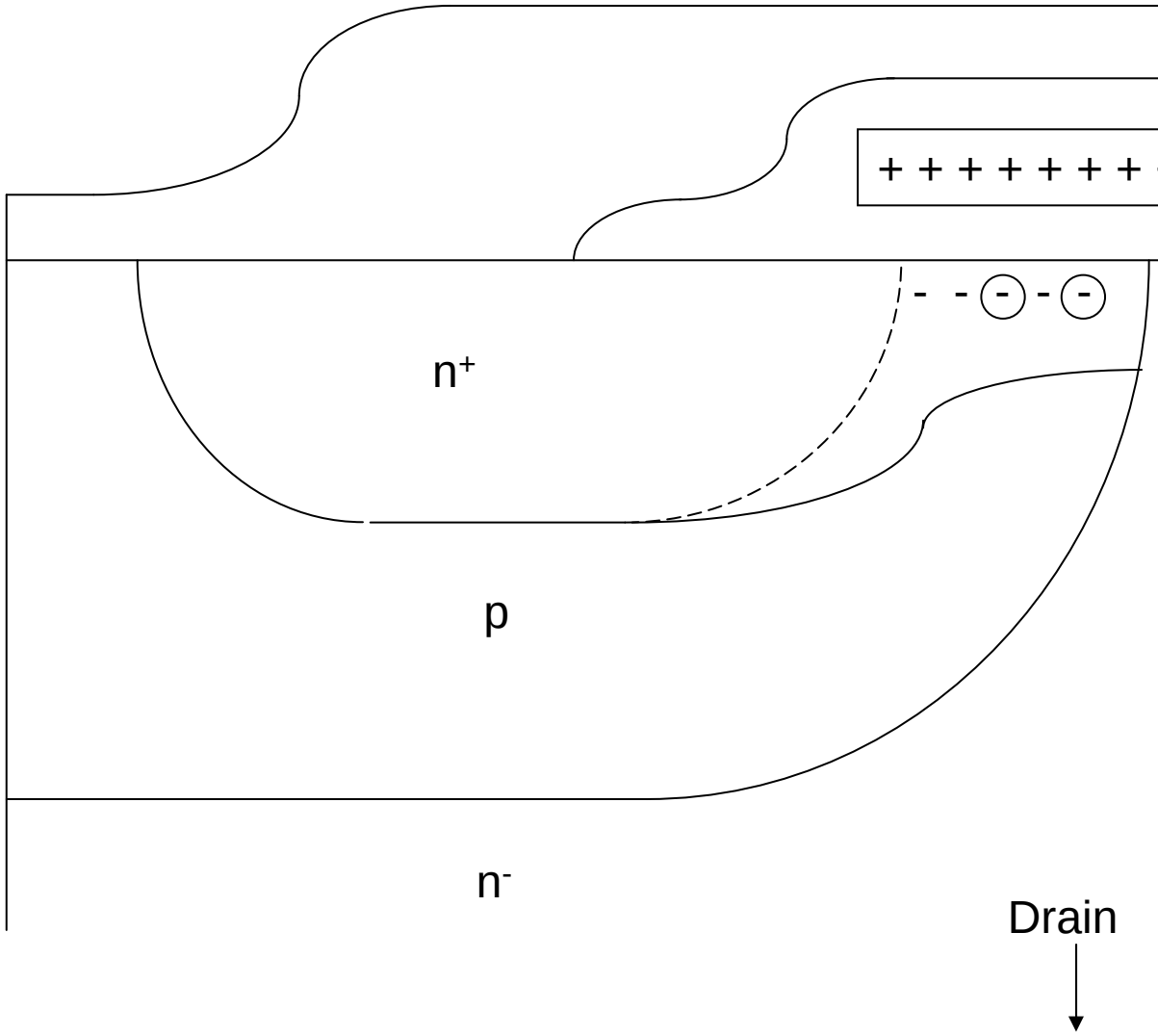


The conduction mechanism, $V_{GS}<V_{GS(th)}$



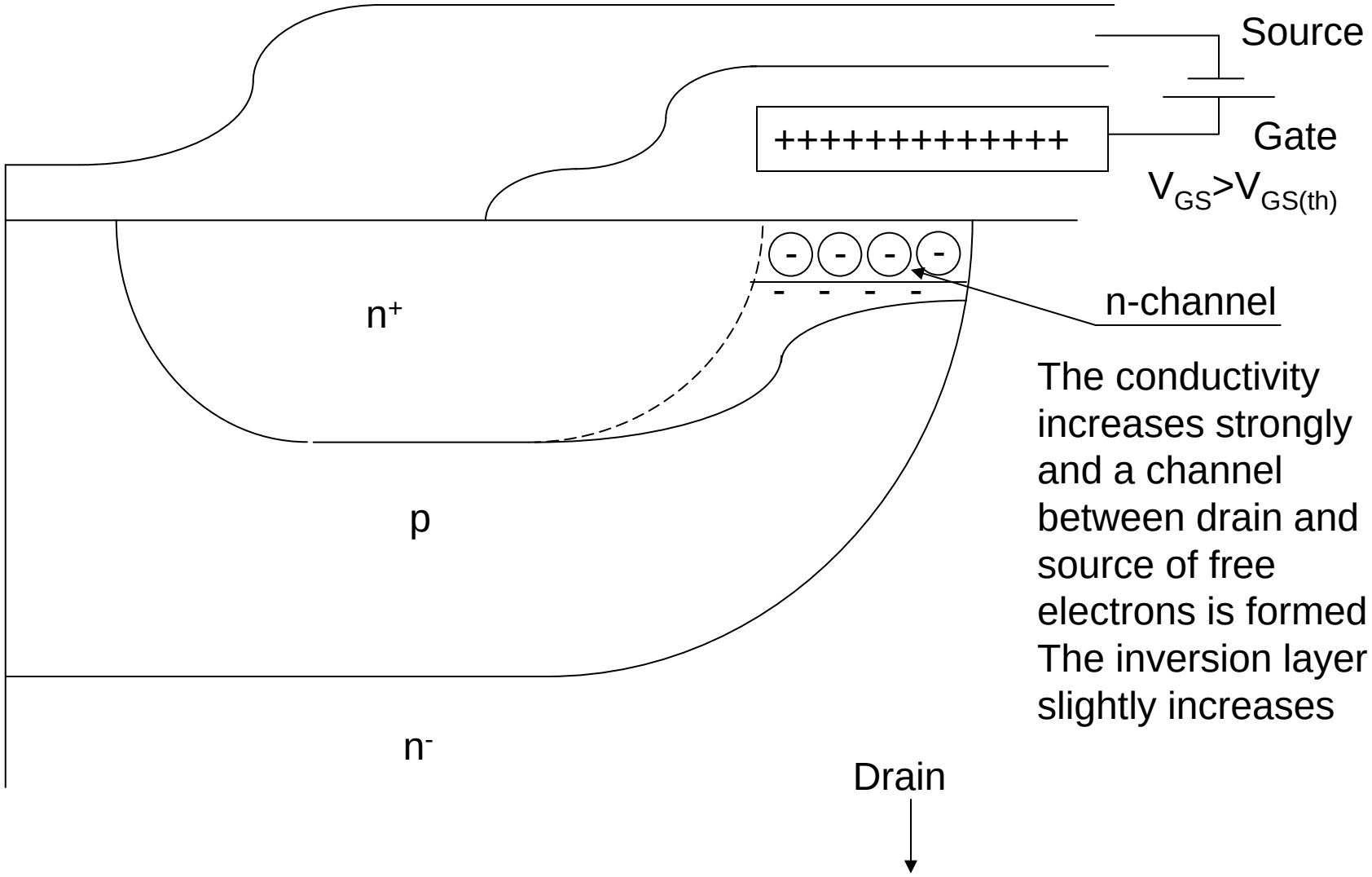
When a voltage, $<V_{GS(th)}$ is applied to the gate a depletion area is formed in the p-body, becaise the majority carriers (holes) are repelled, Acceptor atoms are exposed

The conduction mechanism, $V_{GS}<V_{GS(th)}$



With increased voltage free electrons, which are generated via thermal ionozation, are attracted
When the density of free electrons has grown to the atom doping density of the body the region of free electrons is termed an inversion layer

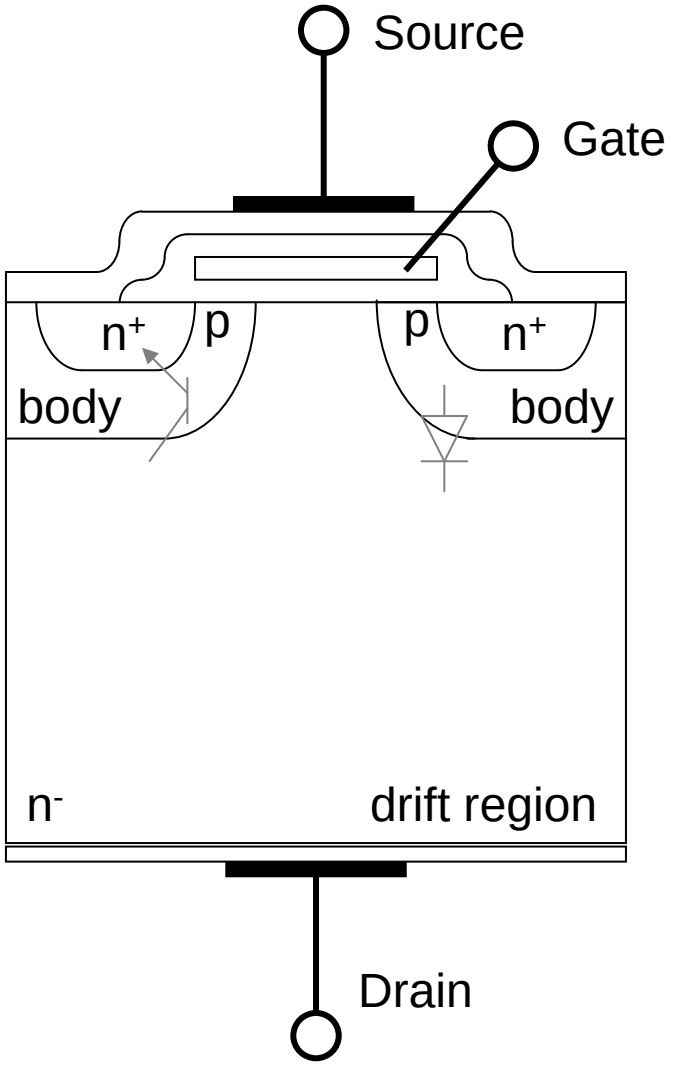
The conduction mechanism, $V_{GS}>V_{GS(th)}$



The conductivity increases strongly and a channel between drain and source of free electrons is formed
The inversion layer slightly increases

The MOSFET parasitic elements

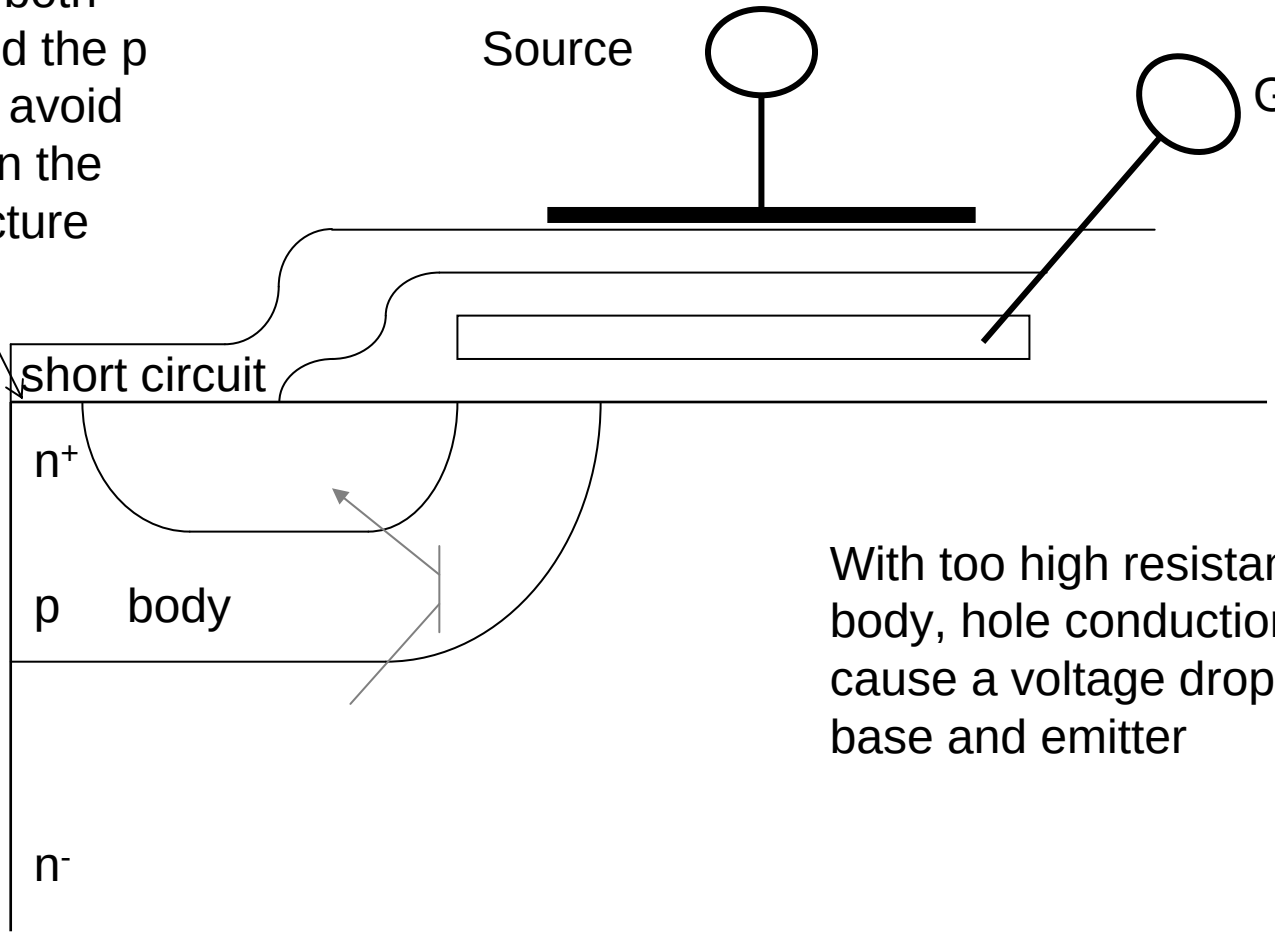
The npn structure must not be turned on as the bjt cannot be turned off, as there is no connection between the gate and the p (body) region.



The parasitic diode structure can be used as a freewheeling diode in bridge application

The MOSFET npn GE short circuit

The source metalisation is covering both the n^+ and the p region to avoid turning on the npn structure

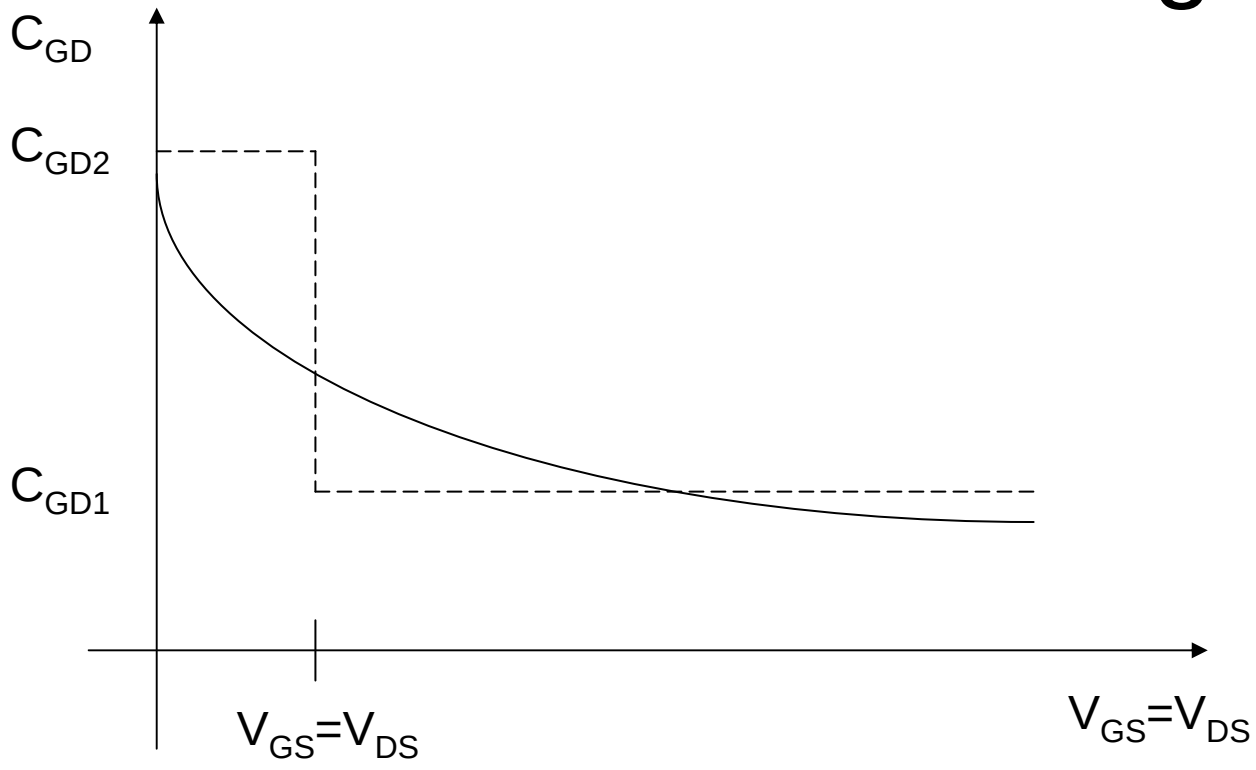


With too high resistance in the body, hole conduction can cause a voltage drop between base and emitter

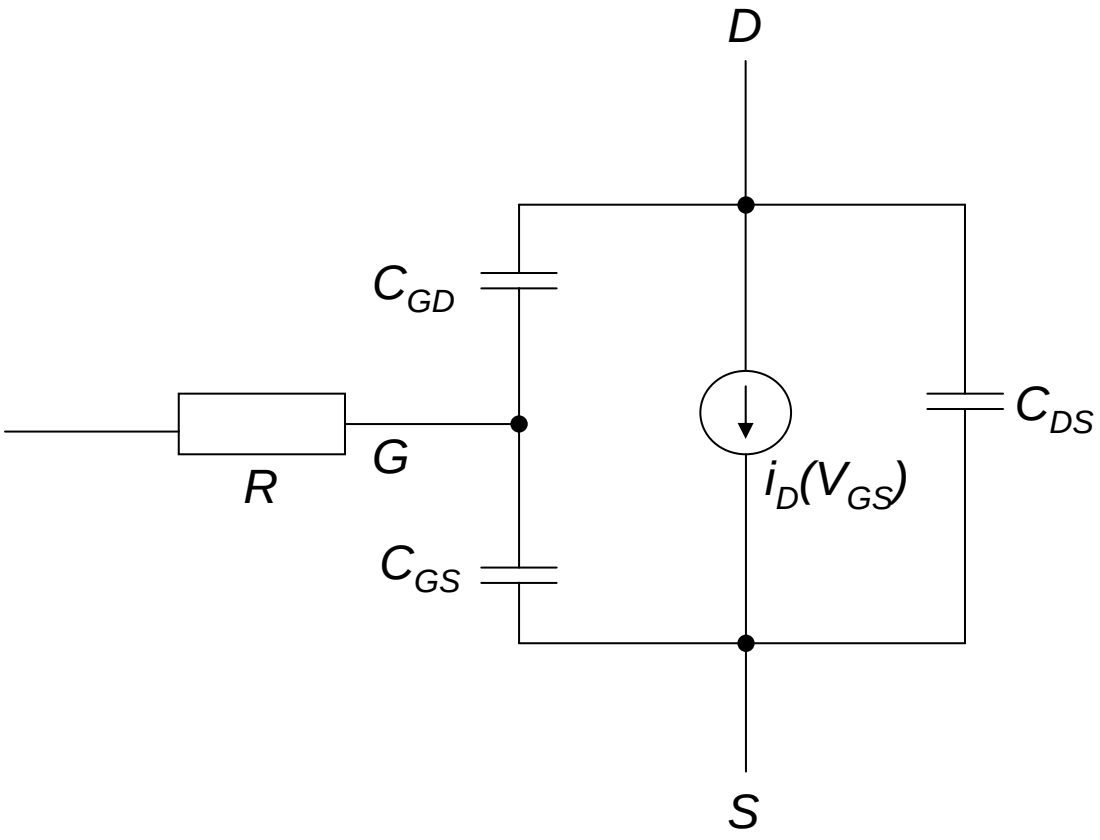
Switching

- A power MOSFET switches faster than the power BJT, since the excess carriers does not have to be established and removed at turn-on and turn-off
- Only the stray capacitance carriers have to be transported
- In most cases the MOSFET can be modelled as being capacitive between all three terminals
- The gate-drain capacitance is formed of the gate-oxide and the depleted part of the drift region. The latter increases with higher gate-drain voltage and thus the capacitance reduces

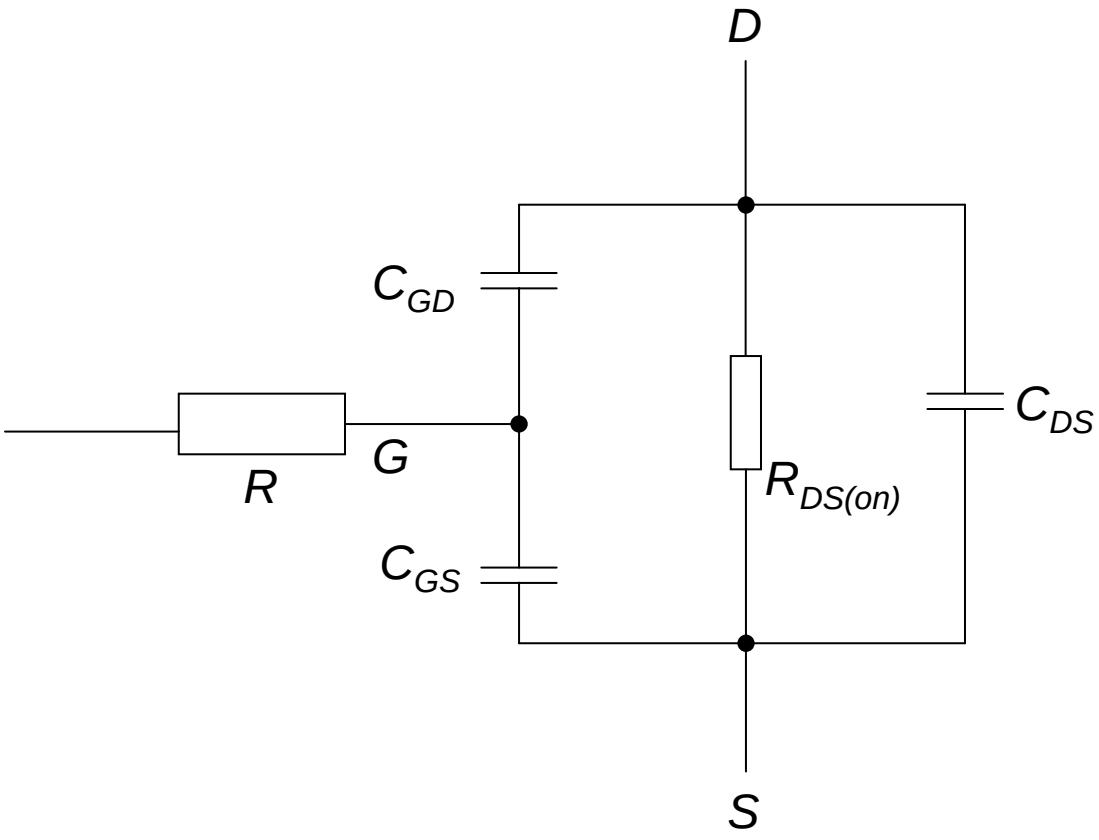
The MOSFET equivalent circuits The gate-drain capacitance versus the drain source voltage



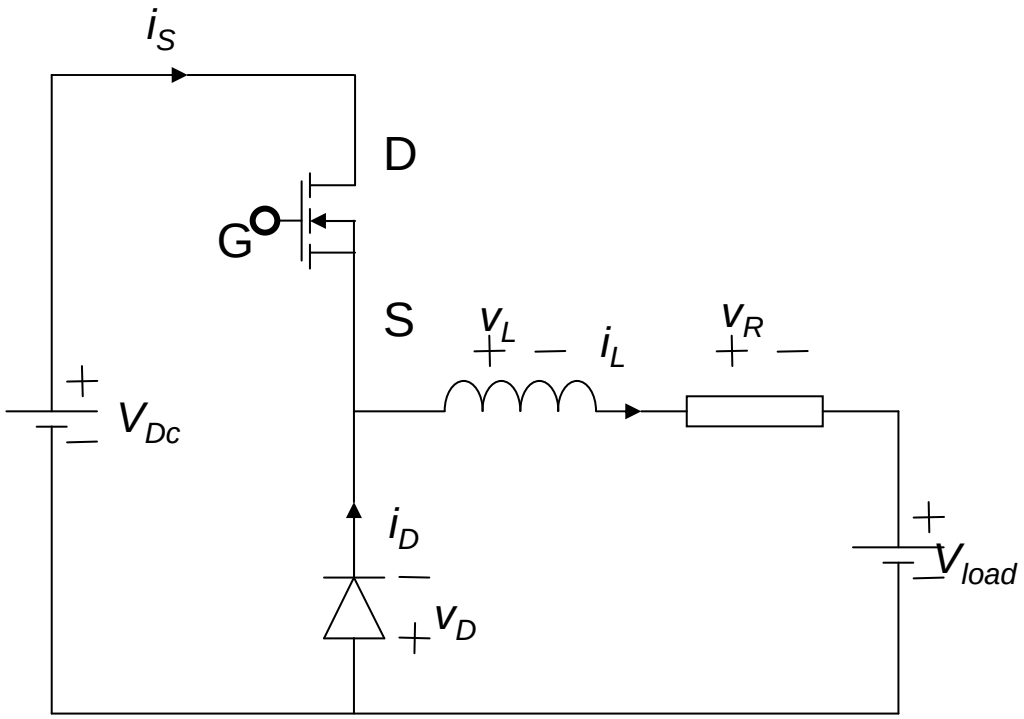
The MOSFET equivalent circuits in the cut-off and active region



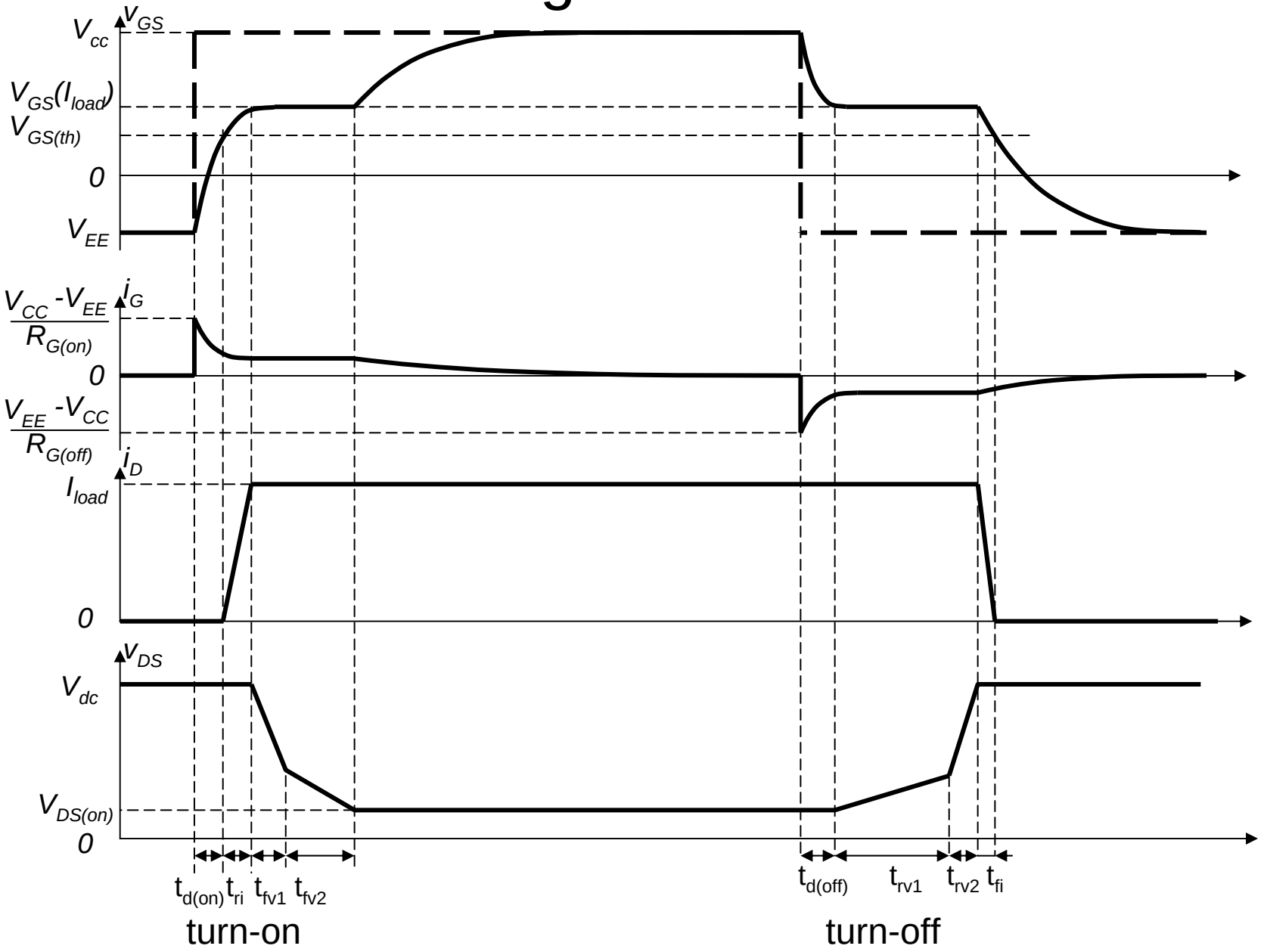
The MOSFET equivalent circuits in the ohmic region



The buck converter, ”step down chopper” with a MOSFET



MOSFET Time diagram at turn-on and turn-off



Turn on delay time

- The gate-source voltage $V_{GS}<V_{GS(th)}$
- The gate-source and the gate-drain capacitances are charged in parallel. The gate time constant is determined by these capacitances and the gate resistor

Current rise time

- When the gate-source voltage has become $V_{GS}>V_{GS(th)}$ the drain current starts to increase

- The gate-source voltage continues to increase with the same time constant

Voltage fall time

- After commutation from the free wheeling diode, the drain source voltage decreases
- The gate-drain capacitance is discharged
- This time is divided in two parts wheather the drain source voltage is higher or lower than the gate-source voltage threshold
- When the gate drain voltage has reached is final value, the gate source voltage clamping is lost and it can further increase

Turn-off delay time

- The gate-source voltage must decrease to a level determined by the transfer characteristic and the actual load current
- When this is reached the MOSFET operates in the active region
- The drain source voltage can rise

Voltage rise time

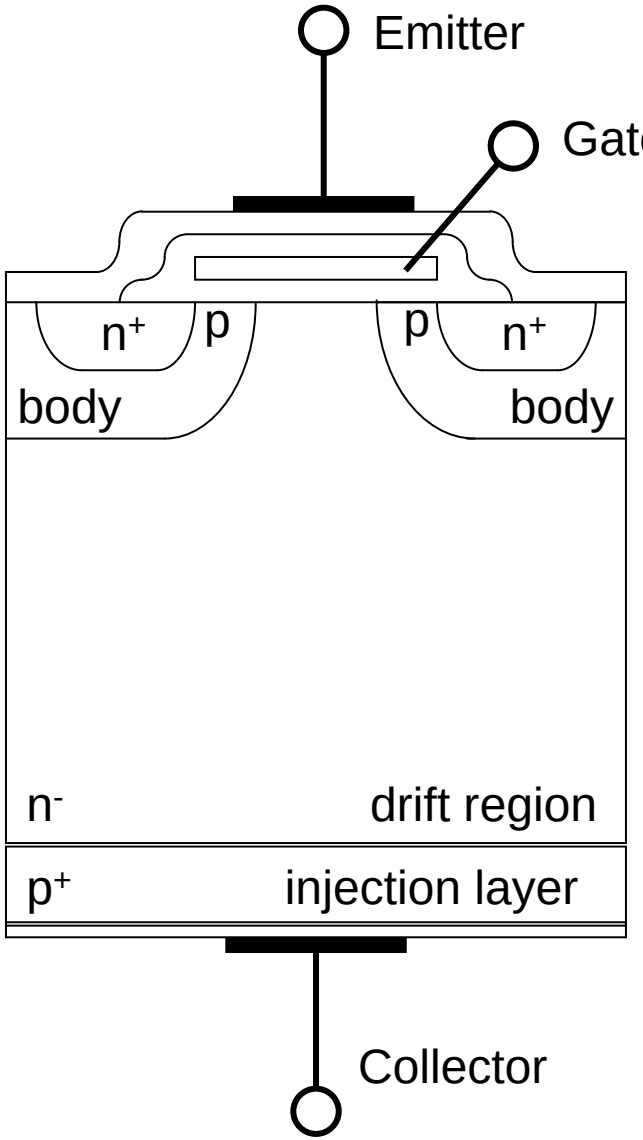
- As similar to turn-on, this part is divided in two parts

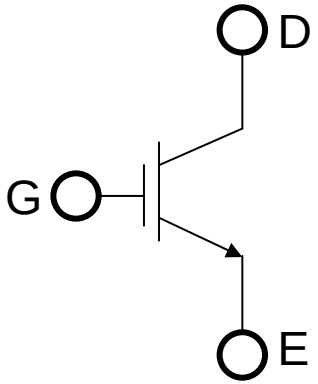
Current fall time

- The current fall time is determined by the transfer characteristic

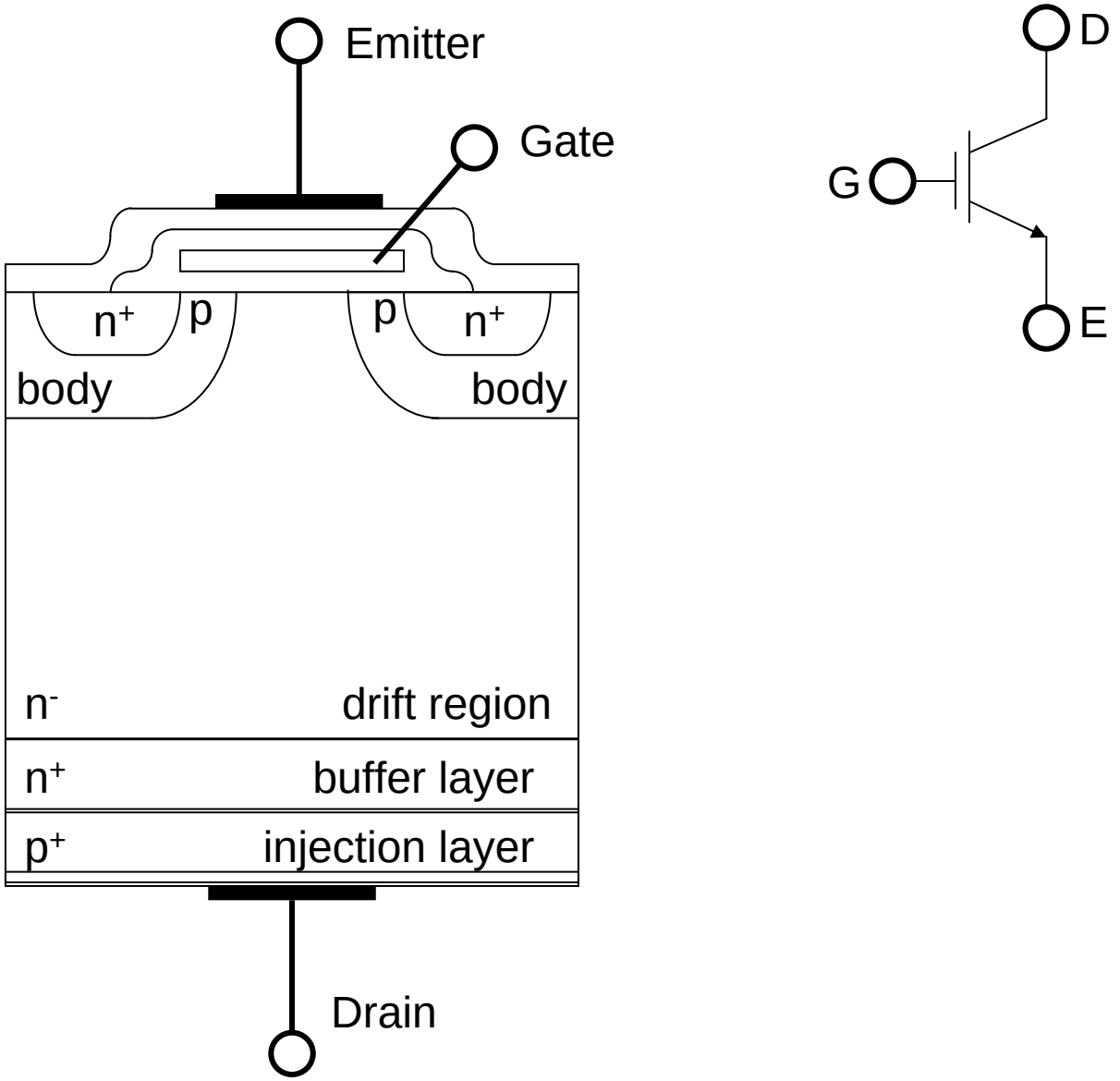
IGBT

The NPT-IGBT

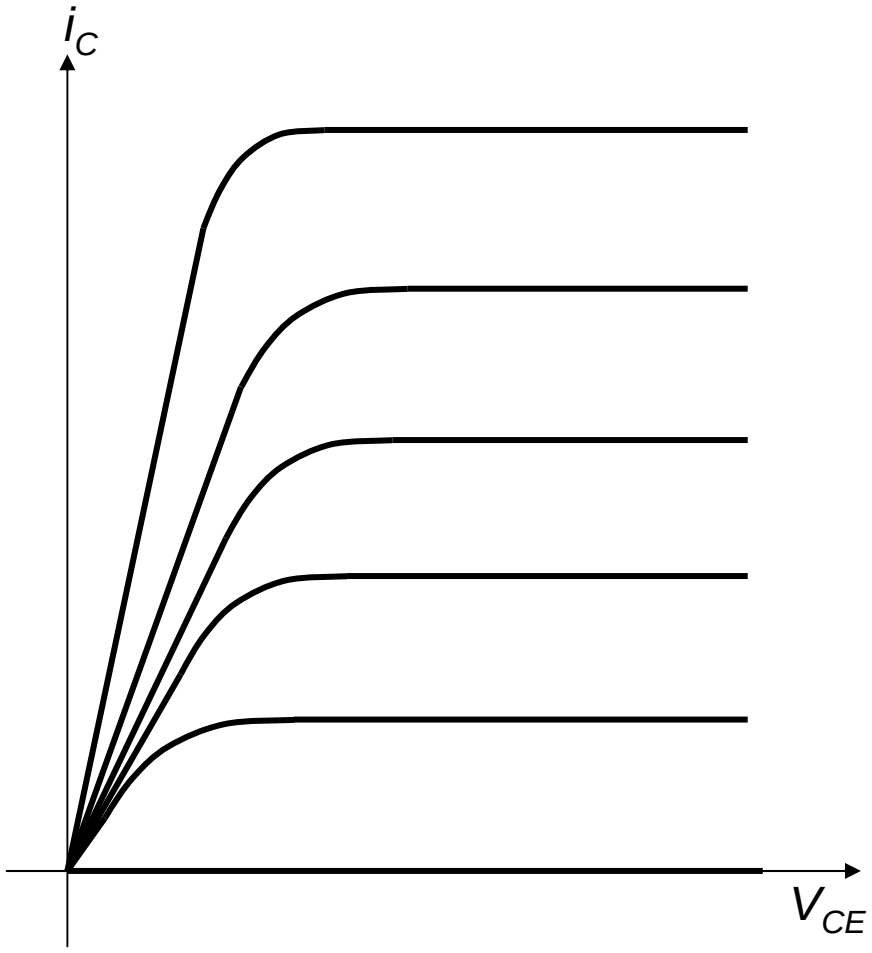

Emitter
Gate
n+
p
p
n+
body
body
n-
drift region
p+
injection layer
Collector


D
G
E

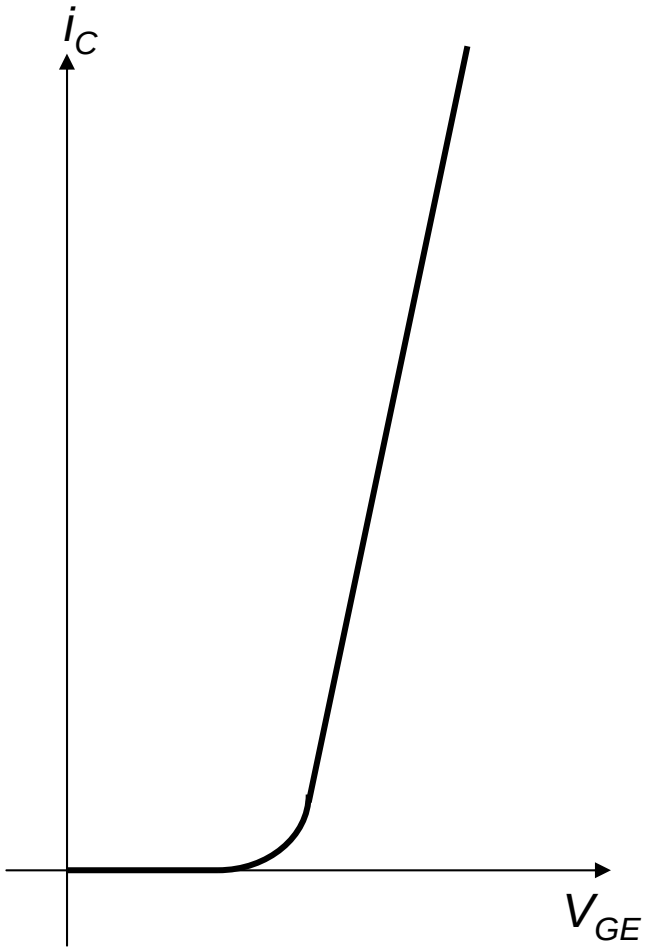
The PT-IGBT


Emitter
Gate
n+
p
p
n+
body
body
n-
drift region
n+
buffer layer
p+
injection layer
Drain
D
G
E

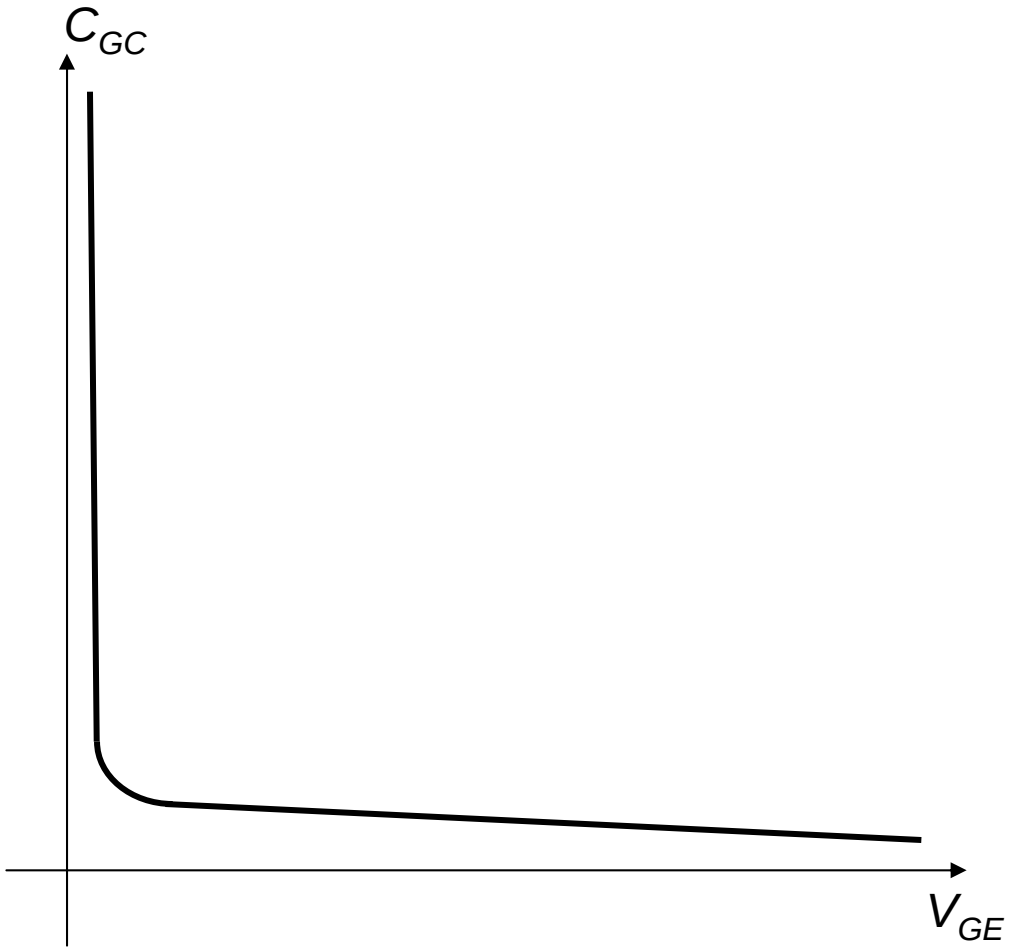
IGBT output characteristic



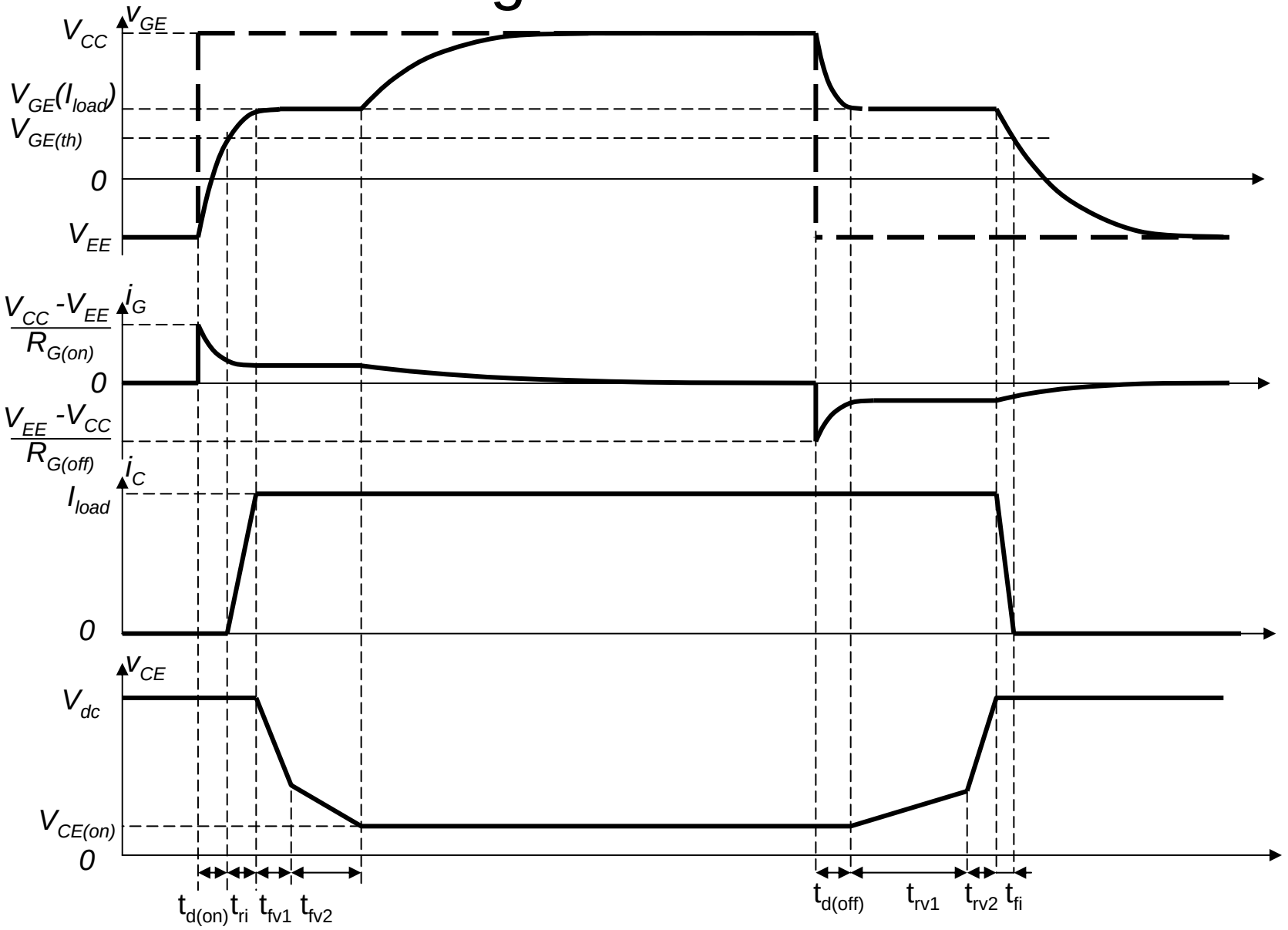
IGBT transfer characteristic



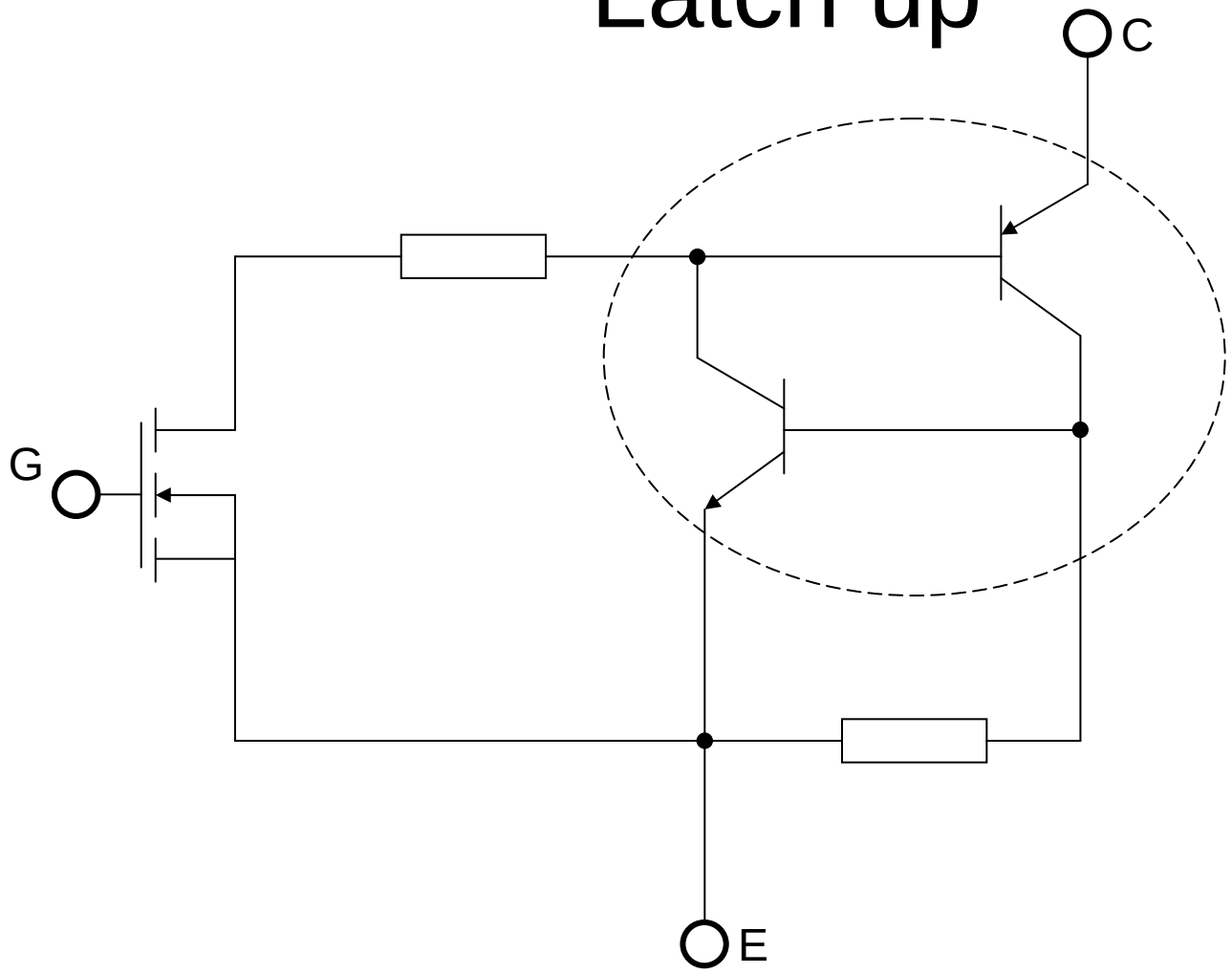
IGBT gate-collector capacitance versus gate-emitter voltage



IGBT Time diagram at turn-on and turn-off

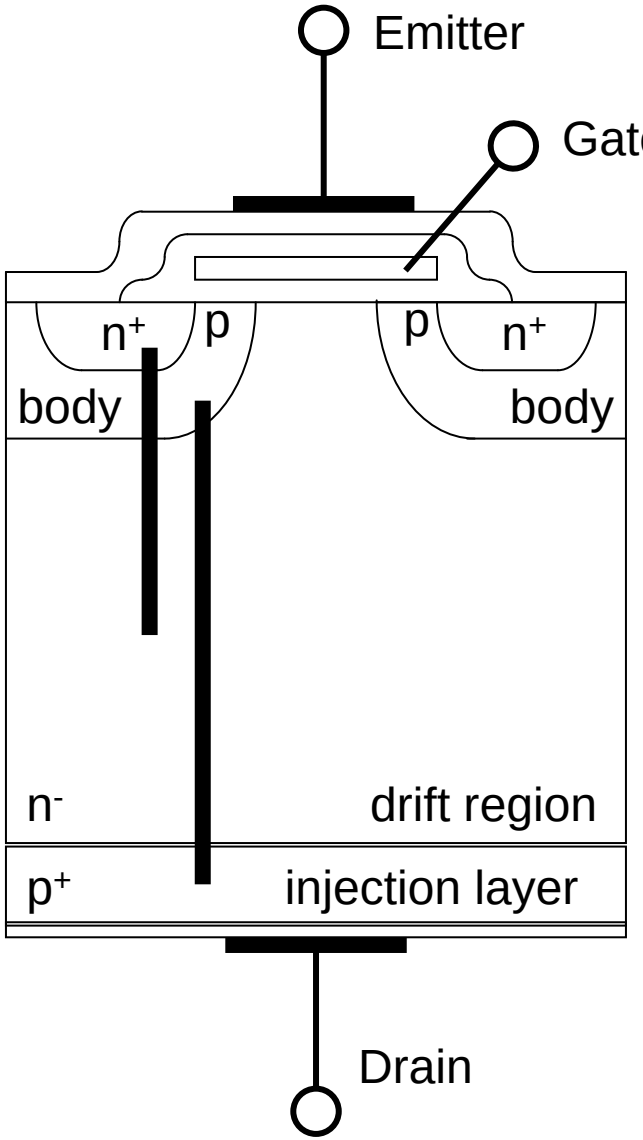


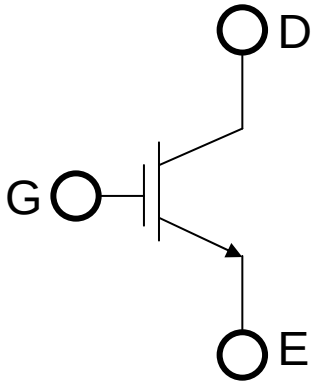
Darlington-thyristor Latch up



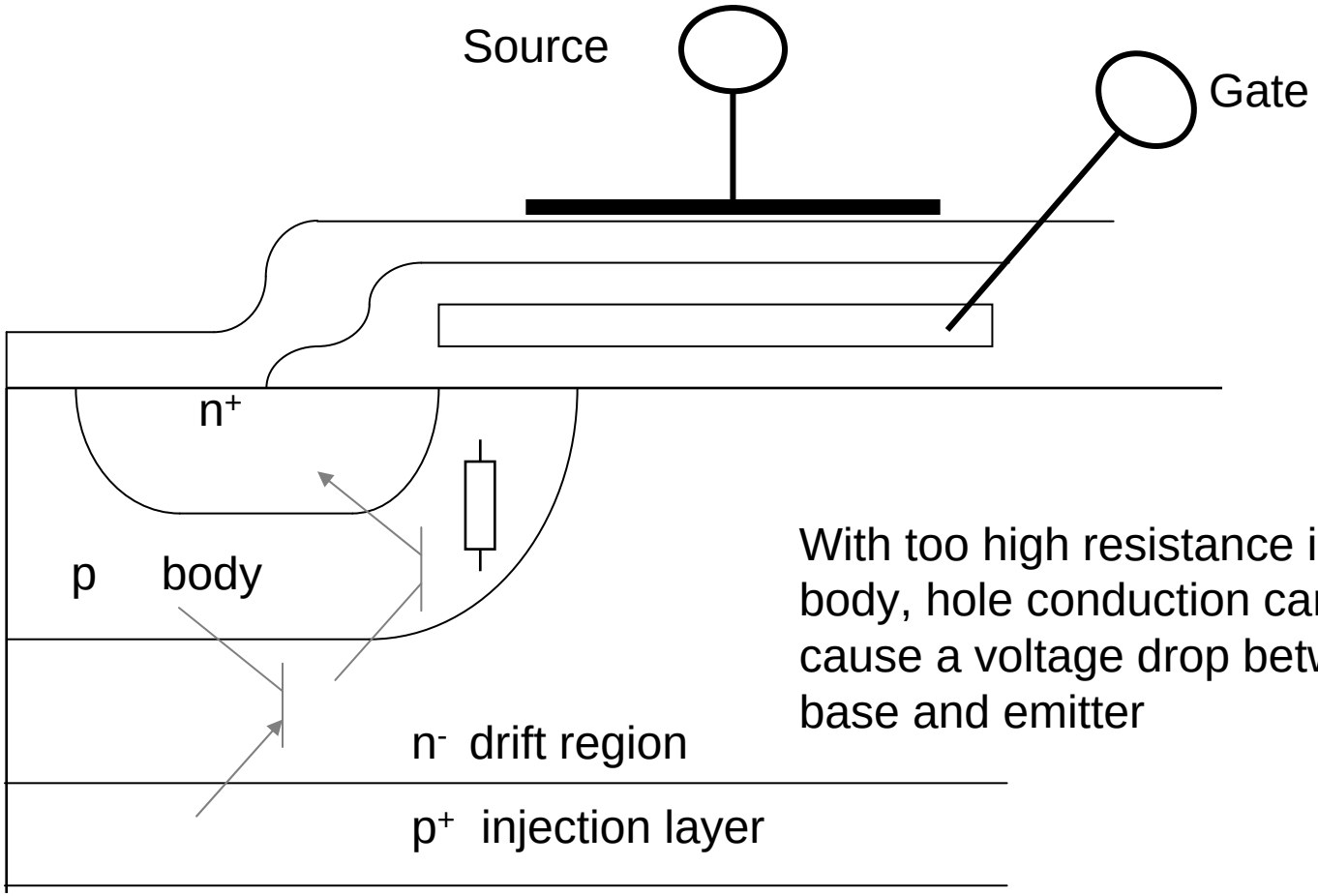
The thyristor structure must not be trigged

The NPT-IGBT


Emitter
Gate
n+
p
p
n+
body
body
n-
drift region
p+
injection layer
Drain


D
G
E

The IGBT latch up



With too high resistance in the body, hole conduction can cause a voltage drop between base and emitter

Safe operting area (SOA)
reverse blocking operating area (RBSOA)

Example 1600 V / 1700 V