Transistors as a switch

Session 6b for Electronics and Telecommunications
A Fairfield University E-Course
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Module: Semiconductor Electronics
(in two parts)

- Text: “Electronics,” Harry Kybett, Wiley, 1986, ISBN 0-471-00916-4
- References:
  - Electronics Tutorial (Thanks to Alex Pounds)
  - Electronics Tutorial (Thanks to Mark Sokos)
- 5 - Semiconductors, Diodes and Bipolar Transistors
  - 5 on-line sessions plus one lab
- 6 - FETs, SCRs, Other Devices and Amplifiers
  - 5 on-line sessions plus one lab
- Mastery Test part 3 follows this Module

Section 6: FETs, SCRs, Other Devices and Operational Amplifiers

- 0BJECTIVES: This section reviews additional important semiconductor devices and their applications. The Operational Amplifier is also studied.

Section 6 Schedule:

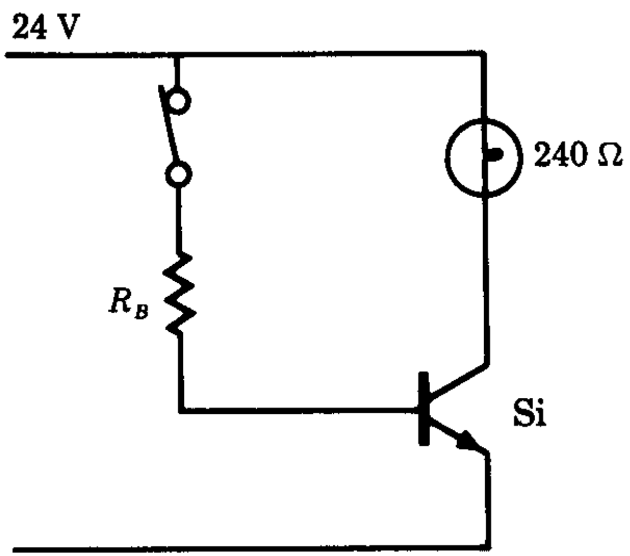
Session 6a	01/15	Field Effect Transistors	Kybett pp 70 – 77, pp 201-209
Session 6b	**01/20**	**Transistors as a switch**	**Kybett pp 78 –107**
Session 6c	01/22	SCR’s, Triacs and UJTs	
Session 6c (Lab - 02/01, Sat.)	01/27	Class “A”, “B”, and “C” Amplifiers	
Session 6e	02/05	Op-Amps	Kybett pp 209-215
Session 6f (Quiz 6 due 02/23)	02/10	Review for Quiz 6	
Session 6g	02/24	Discuss Quiz 6	
Session 6h	02/26	Review for MT3	
MT3	03/02	MT3 Exam	
Session 6i	03/10	Discuss MT3	

FET Summary

- A voltage-controlled resistor
- Channel material
  - N-channel FET
  - P-channel FET
- FET types
  - Junction FET (JFET)
  - Metal Oxide Gate FET (MOSFET)
  - Complementary Symmetry MOSFET (CMOS)
- Simple high input impedance amplifiers
- Very effective as switches (Session 6b)

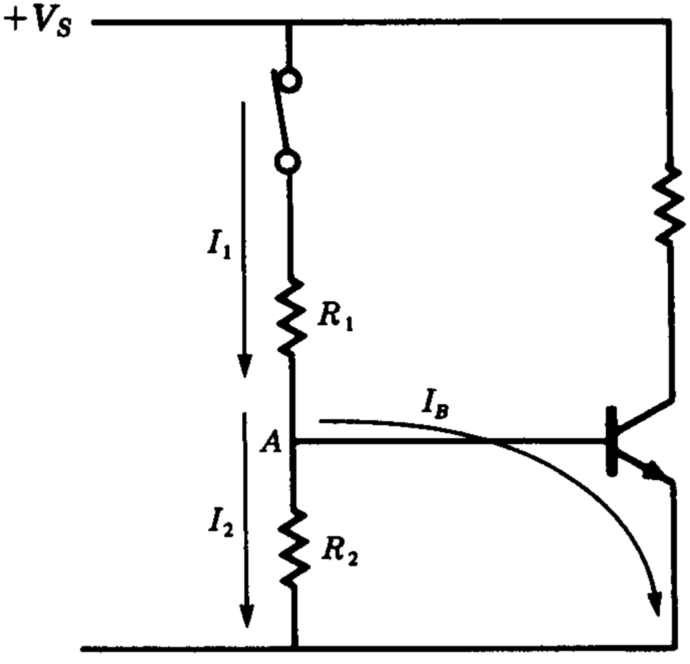
An NPN Switch

- Open switch – no current
- Closed switch – base current flows
  - For saturation (fully on) $I_c \sim 0.1$ amp
  - If $\beta = 100$, $I_b \sim 1$ milliamp



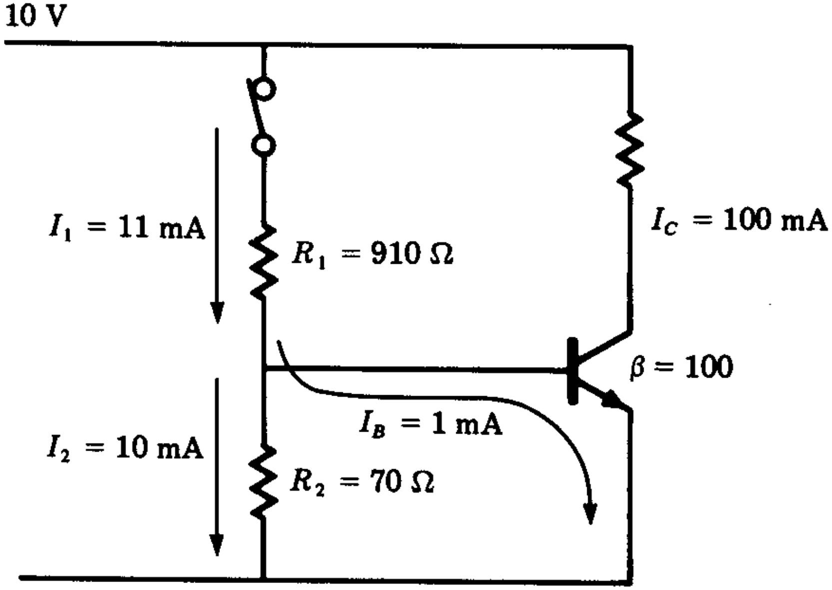
Better Biasing

- **Never** leave transistor (or IC) inputs dangling
  - Noise sensitivity
  - Static discharge failures
- Reduced leakage current sensitivity
  - I_{cb}: reverse leakage current
  - R_2 conducts leakage current t ground



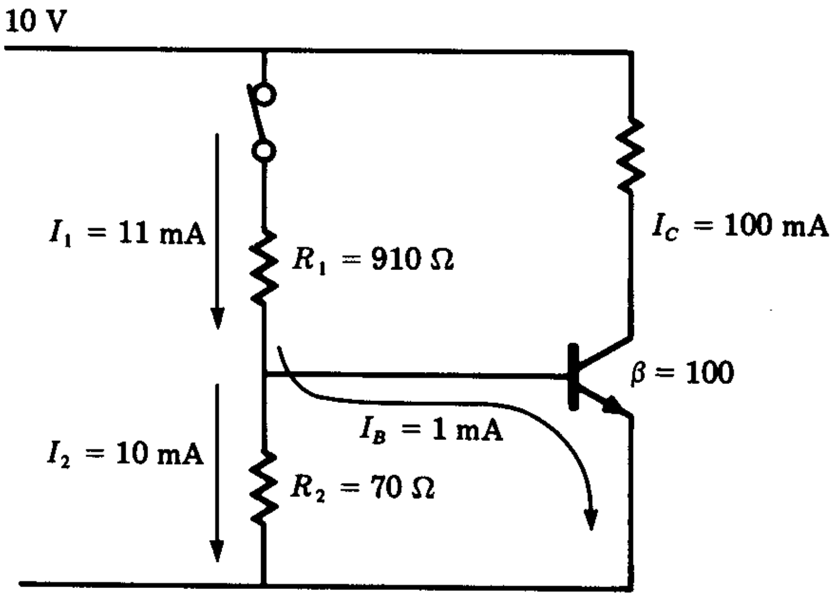
Biasing Analysis

- Desire 100 ma load current



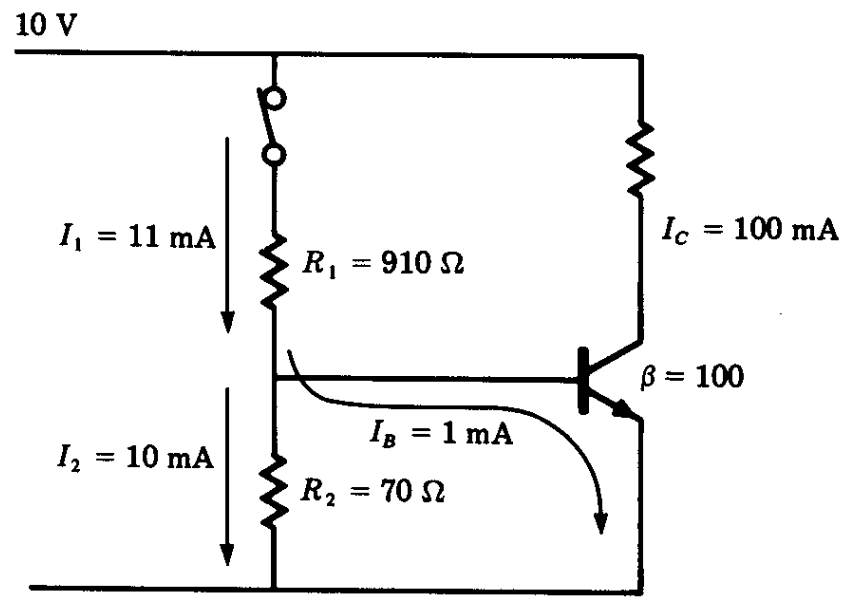
Biasing Analysis

- Desire 100 ma load current
- Base current >1 ma for saturation (β=100)



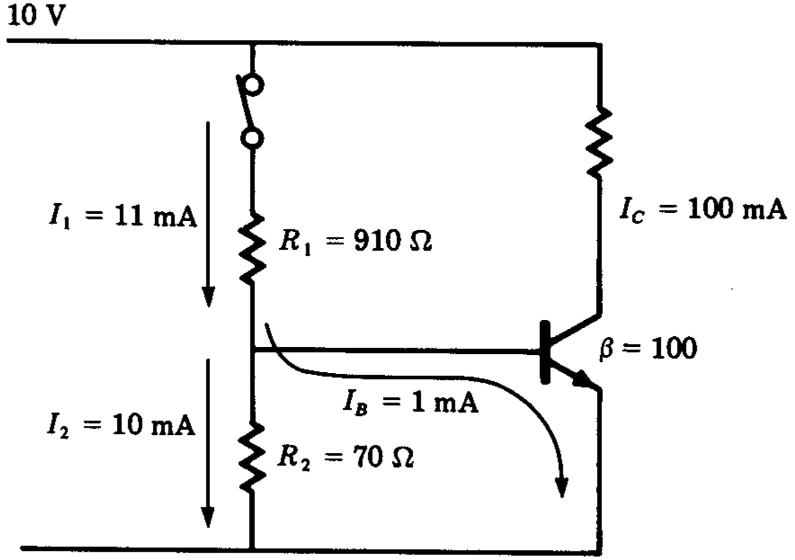
Biasing Analysis

- Desire 100 ma load current
- Base current >1 ma for saturation (β=100)
- Set I_2 = 10 ma
  - Low impedance biasing for reduced leakage sensitivity



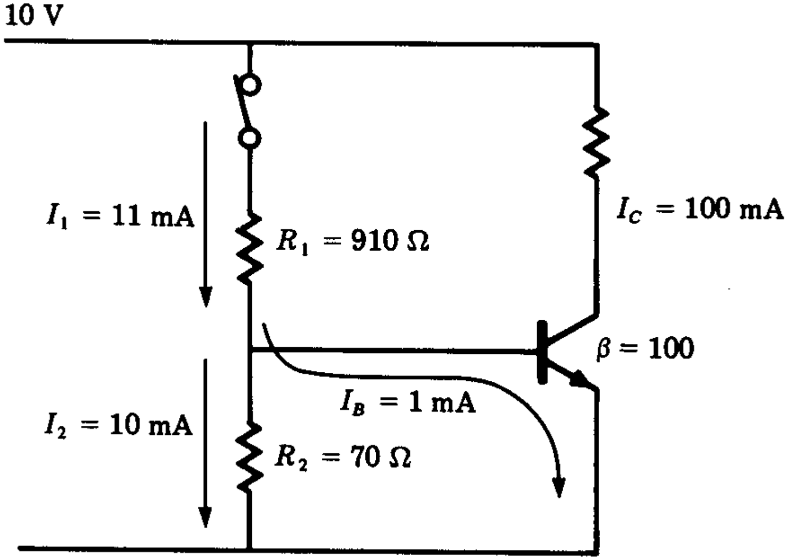
Biasing Analysis

- Desire 100 ma load current
- Base current >1 ma for saturation (β=100)
- Set I_2 = 10 ma
- R_2 = 70 Ω (68 Ω)
  (Low impedance biasing;
  reduced leakage sensitivity)



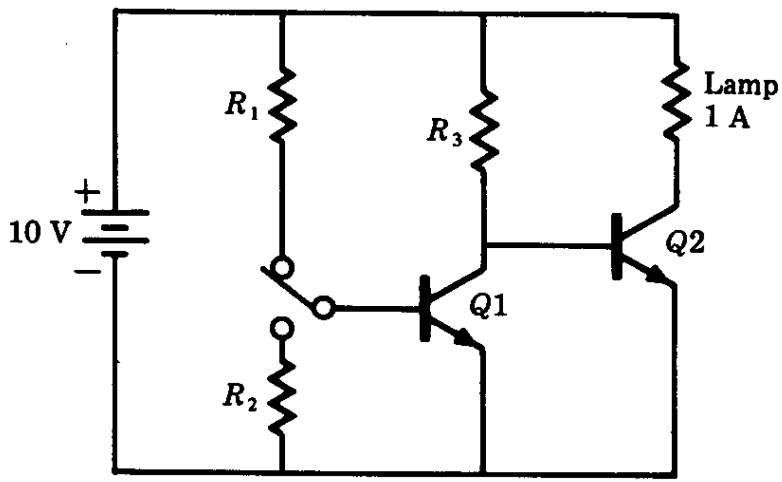
Biasing Analysis

- Desire 100 ma load current
- Base current >1 ma for saturation (β=100)
- Set I_2 = 10 ma
- R_2 = 70 Ω (68 Ω)
  (Low impedance biasing; reduced leakage sensitivity)
- R_1 = 846 Ω (820 Ω)
- Note reduced current gain and higher power use



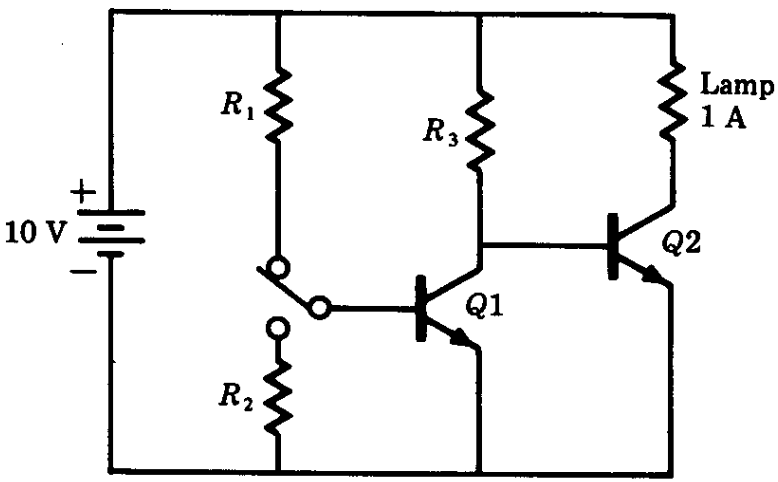
More Current Gain

- Cascade two transistors
- Bias the first transistor for a smaller load current
- The second transistor provides the higher current
- Is the lamp on or off here?



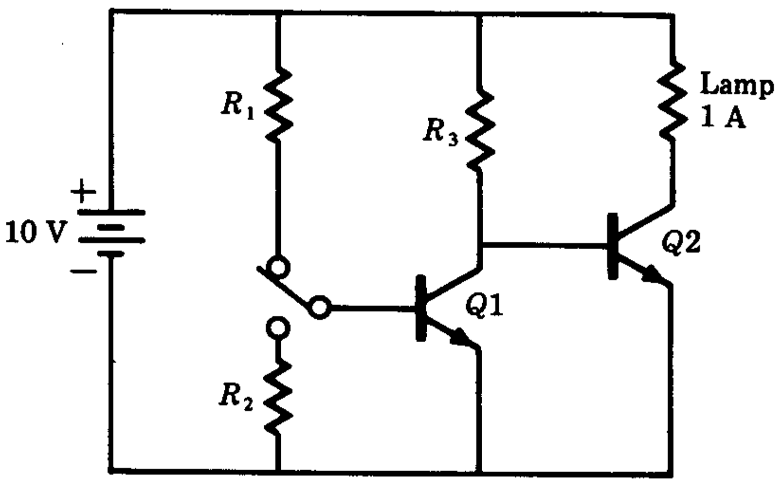
More Current Gain

- Cascade two transistors
- Bias the first transistor for a smaller load current
- The second transistor provides the higher current
- Is the lamp on or off here?
  - Q1 is on



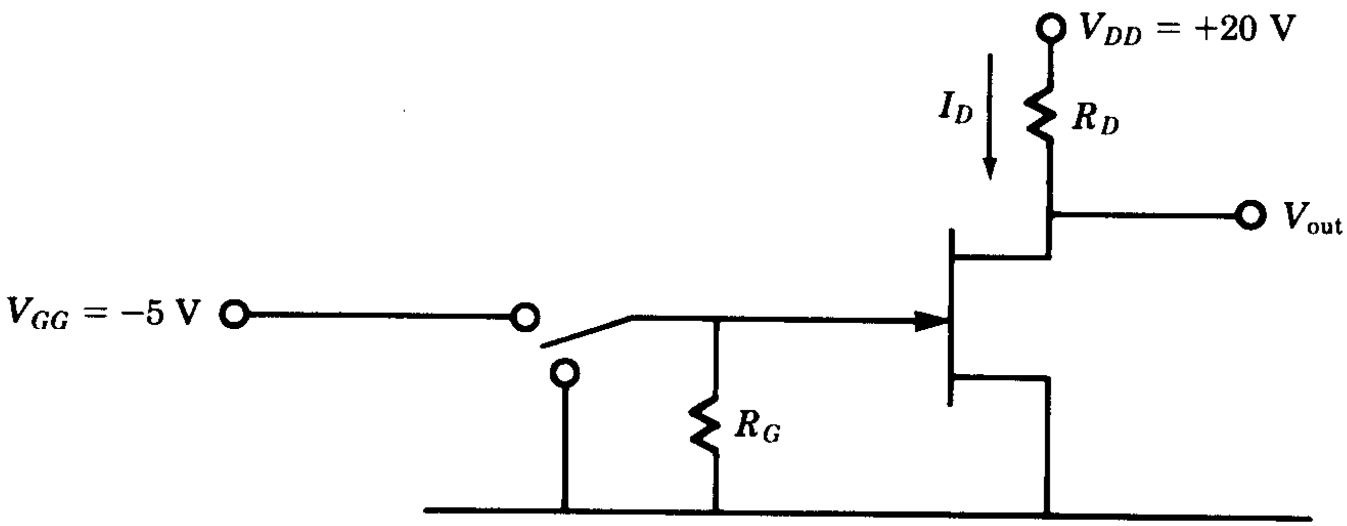
More Current Gain

- Cascade two transistors
- Bias the first transistor for a smaller load current
- The second transistor provides the higher current
- Is the lamp on or off here?
  - Q1 is on
  - Q2 is off



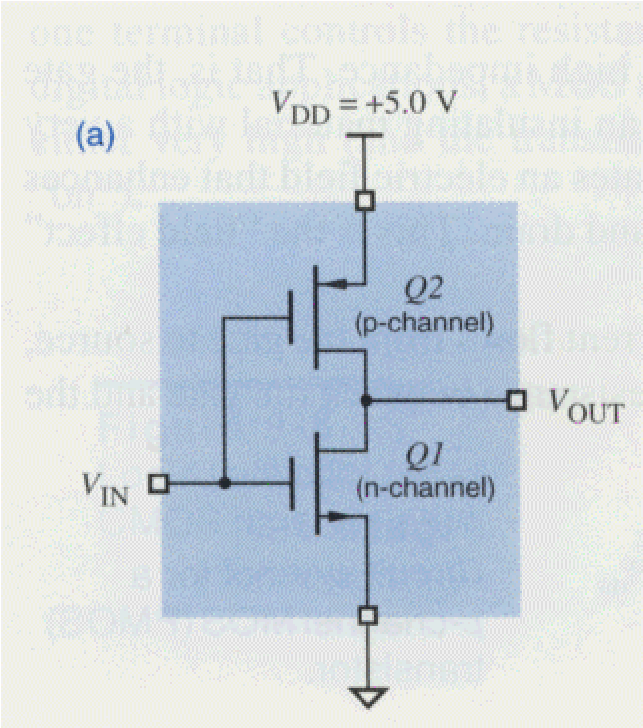
An N-Channel JFET Switch

- V_{gg} = 0; the JFET is on
- V_{gg} = -5; the JFET is off



A CMOS Inverter

- Q1: N-channel MOSFET, Q2: P-channel MOSFET
- If V_{in} is grounded
  - Q1 is off and Q2 is on
  - V_{out} is +5v
- If V_{in} is +5 volts
  - Q2 is off and Q1 is on
  - V_{out} is 0 volts
- Q1 and Q2 are FET switches (always opposite condition)



Note: these MOSFETs are designed to be off for Vgs < 1 volt

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