(a) Conventional symbol (b) Array logic symbol

Fig. 7-1 Conventional and Array Logic Diagrams for OR Gate

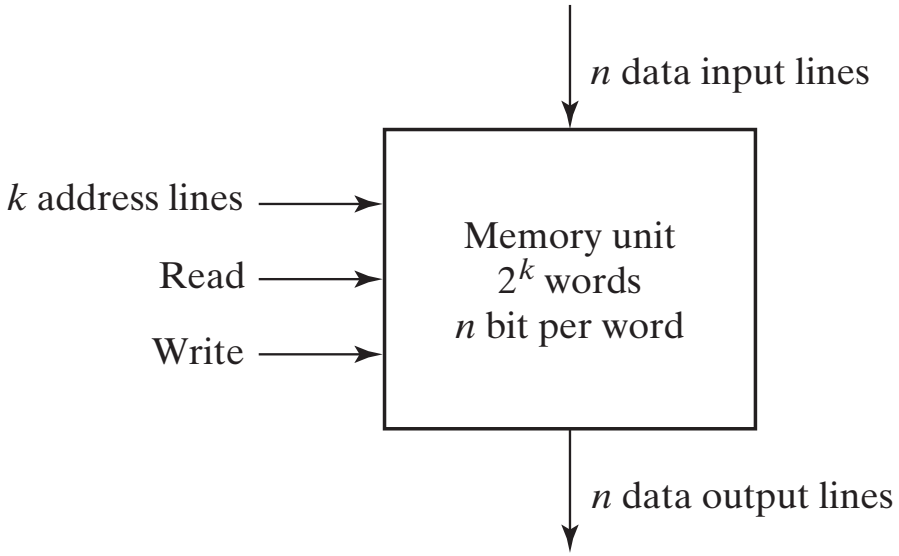
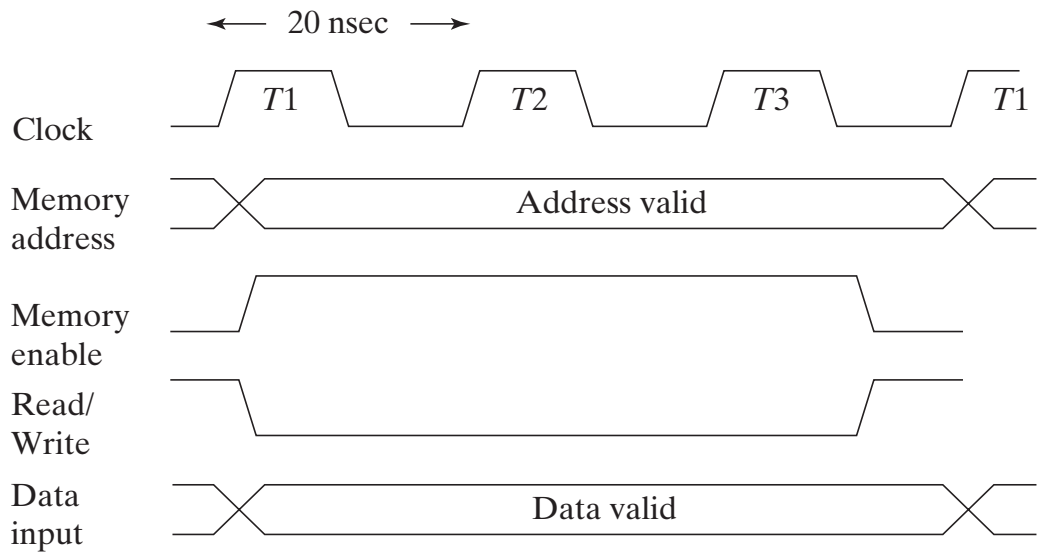


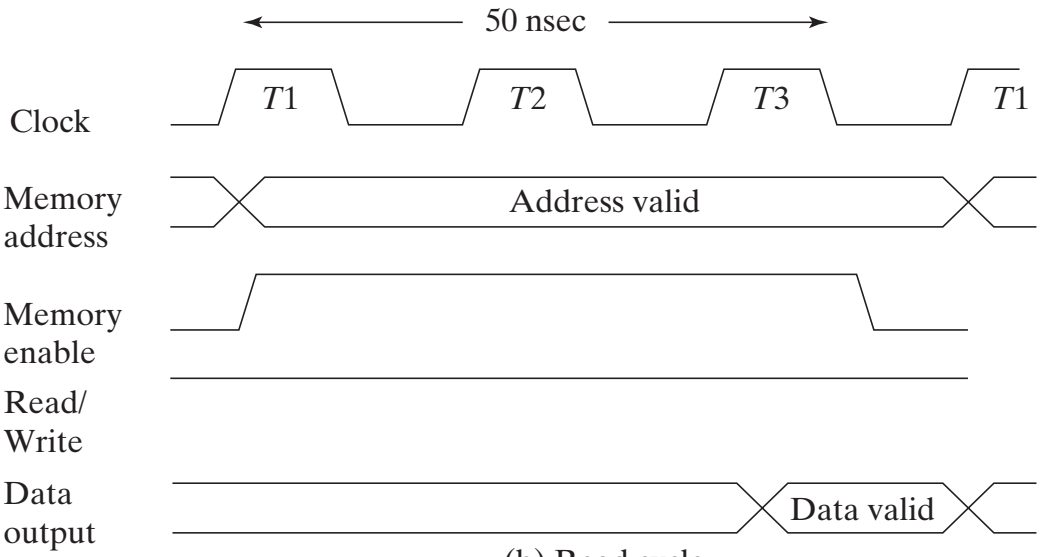
Fig. 7-2 Block Diagram of a Memory Unit

Memory address		
Binary	decimal	Memory contest
0000000000	0	1011010101011101
0000000001	1	1010101110001001
0000000010	2	0000110101000110
	⋮	⋮
1111111101	1021	1001110100010100
1111111110	1022	0000110100011110
1111111111	1023	1101111000100101

Fig. 7-3 Content of a 1024 × 16 Memory

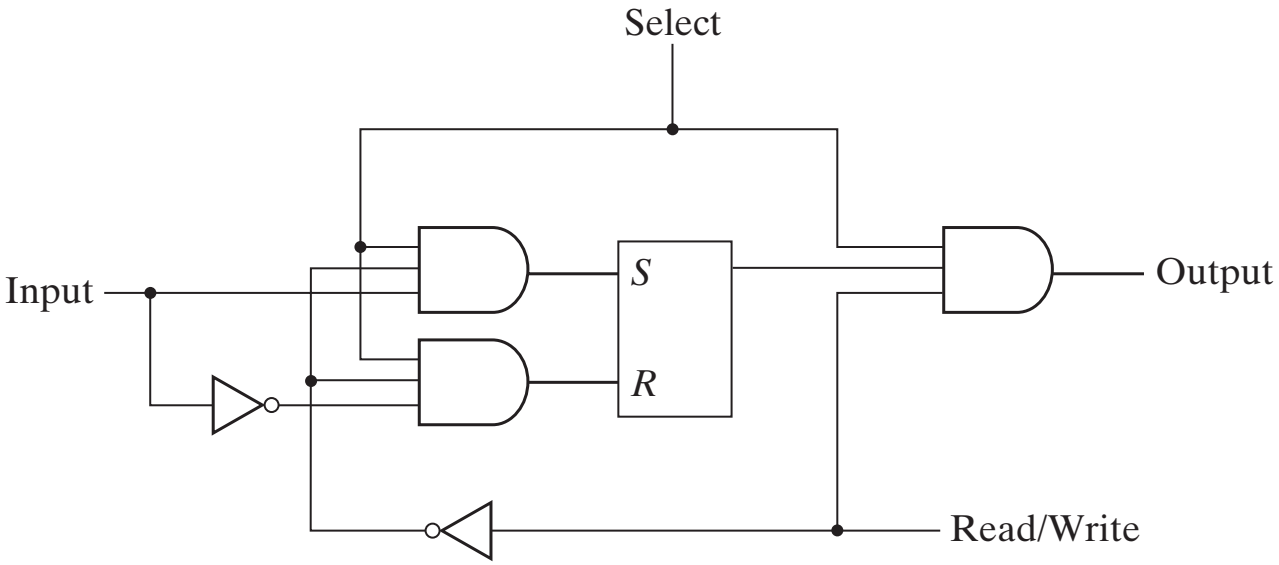


(a) Write cycle

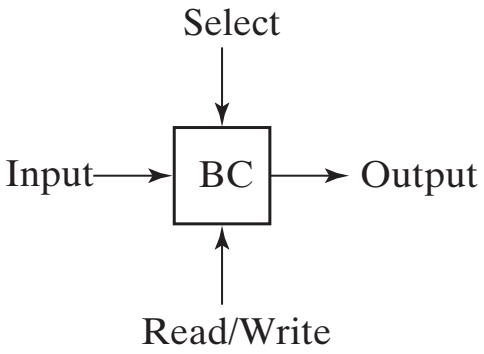


(b) Read cycle

Fig. 7-4 Memory Cycle Timing Waveforms



(a) Logic diagram



(b) Block diagram

Fig. 7-5 Memory Cell

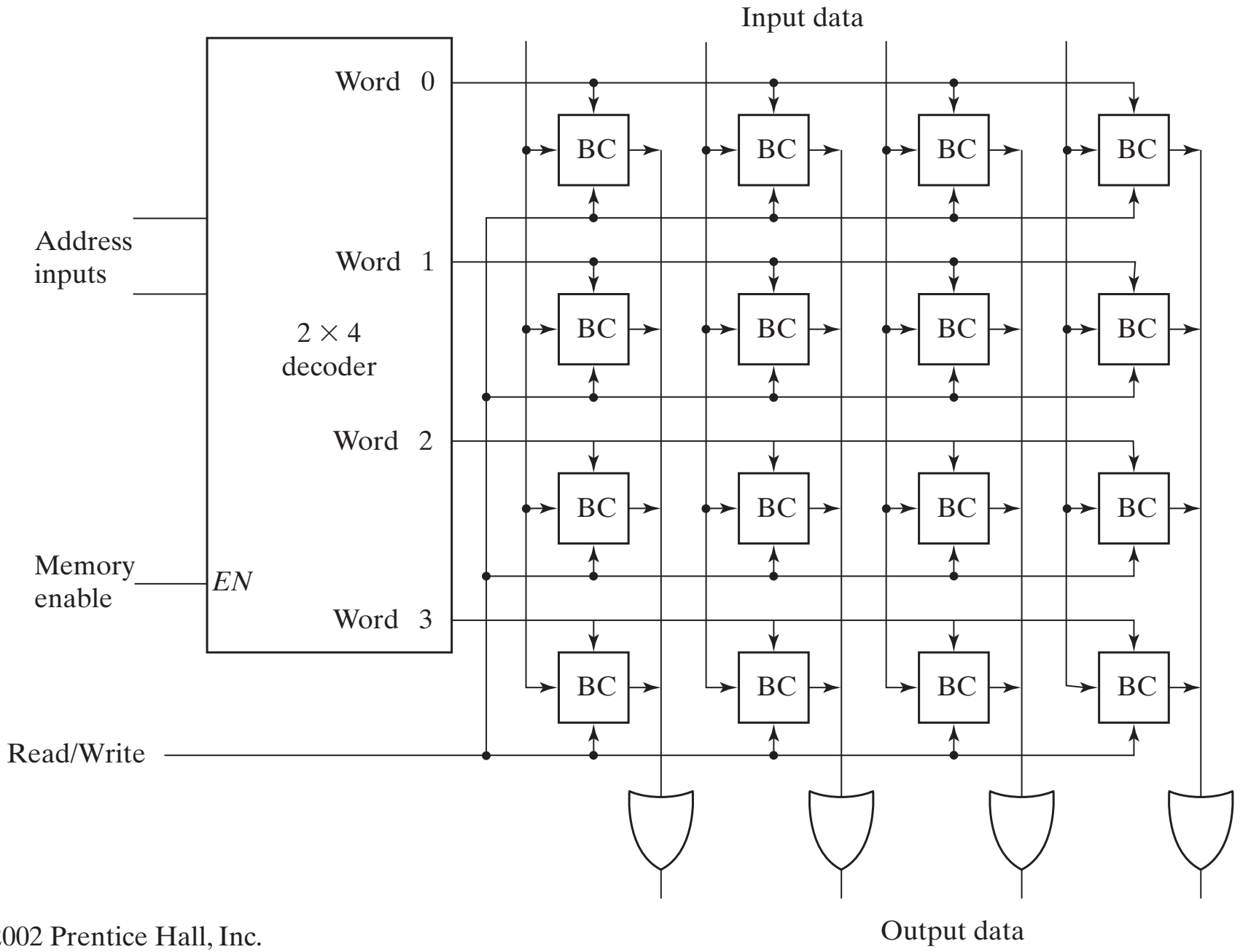


Fig. 7-6 Diagram of a 4 × 4 RAM

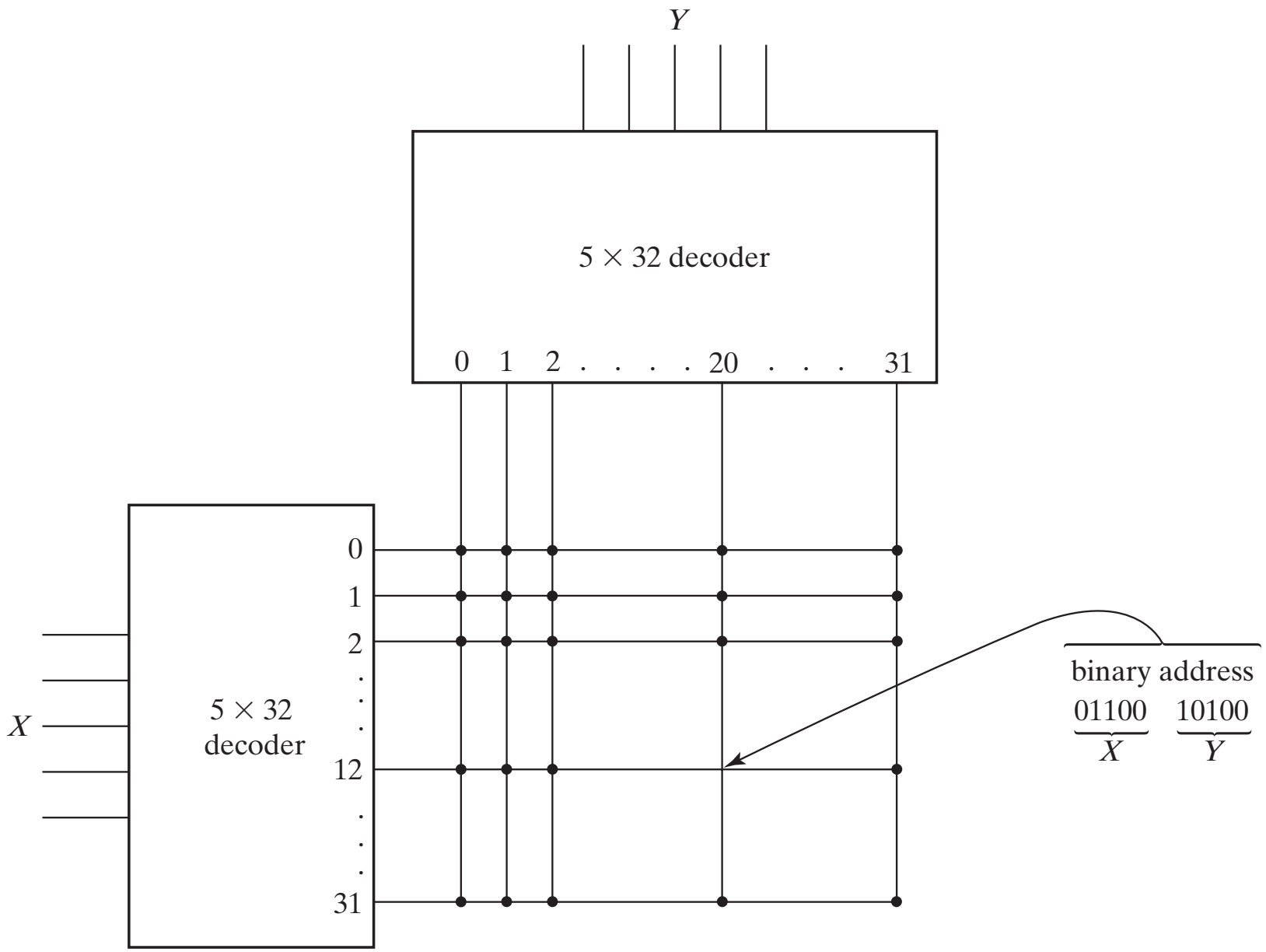


Fig. 7-7 Two-Dimensional Decoding Structure for a 1K-Word Memory

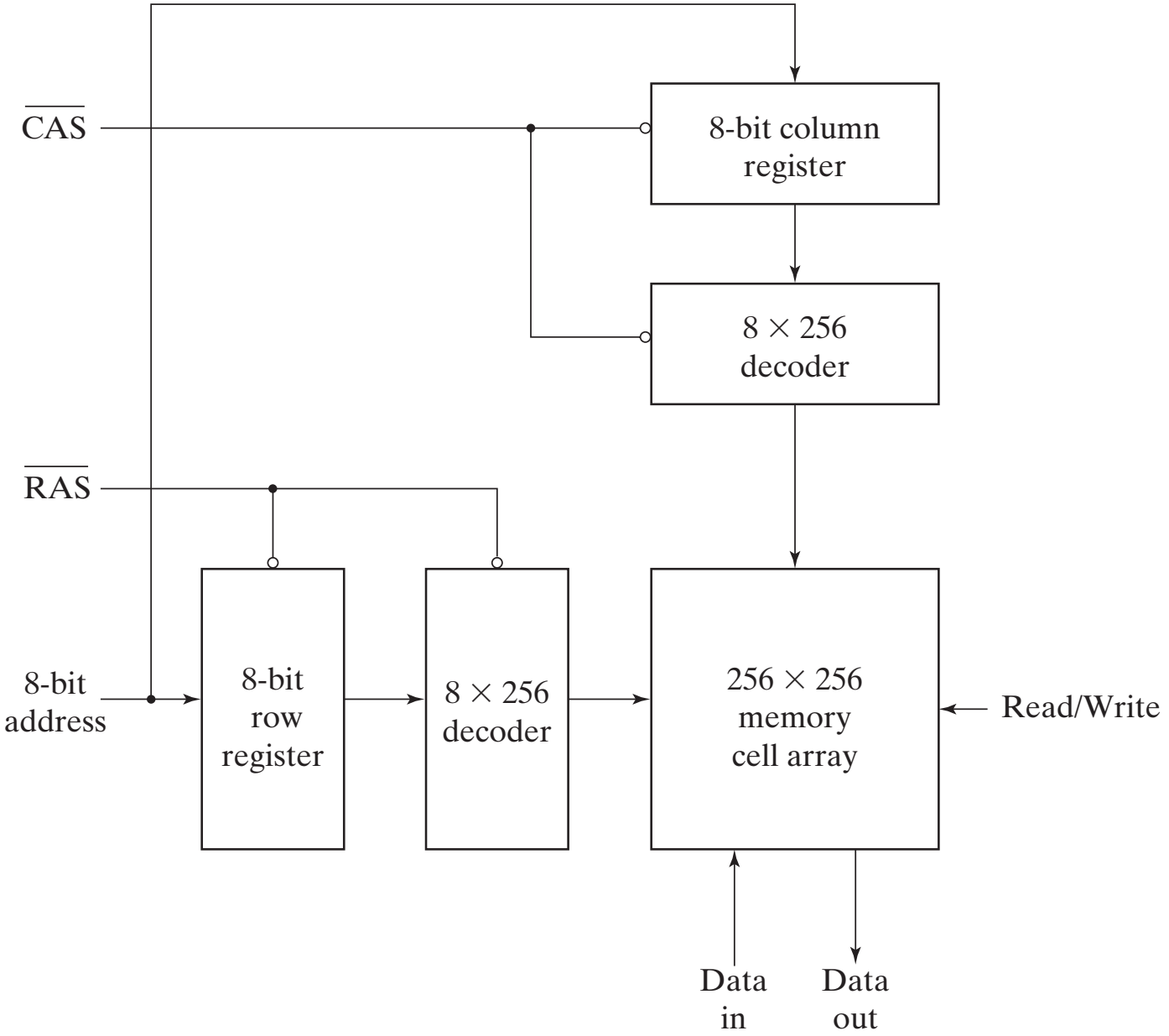


Fig. 7-8 Address Multiplexing for a 64K DRAM

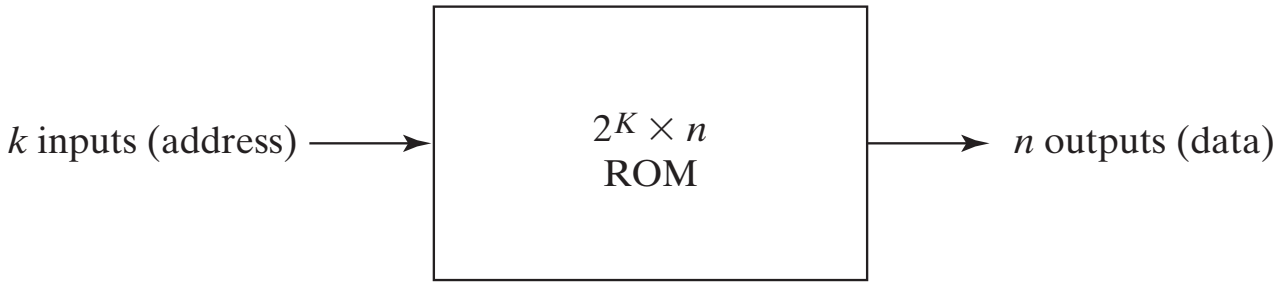


Fig. 7-9 ROM Block Diagram

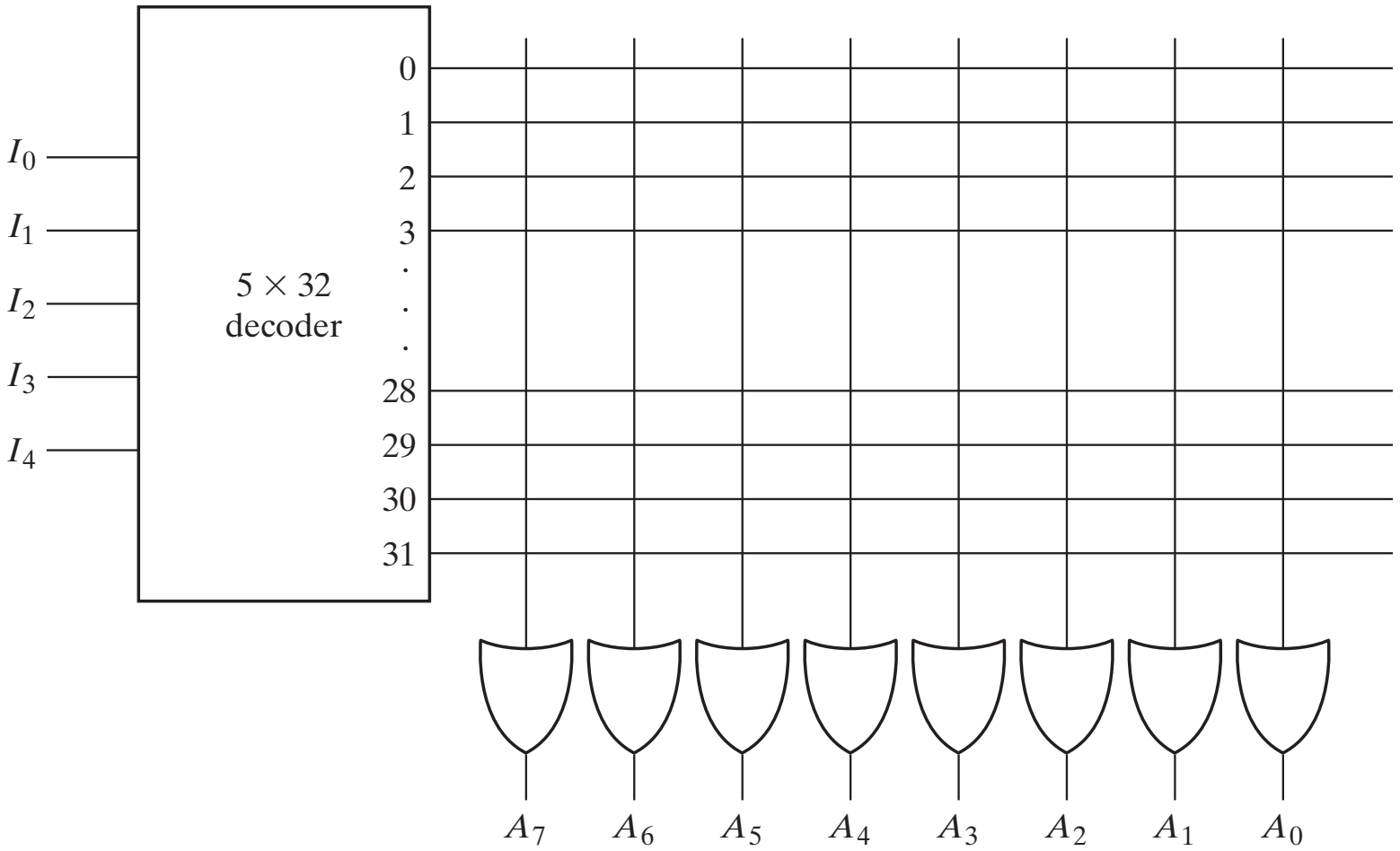


Fig. 7-10 Internal Logic of a 32 × 8 ROM

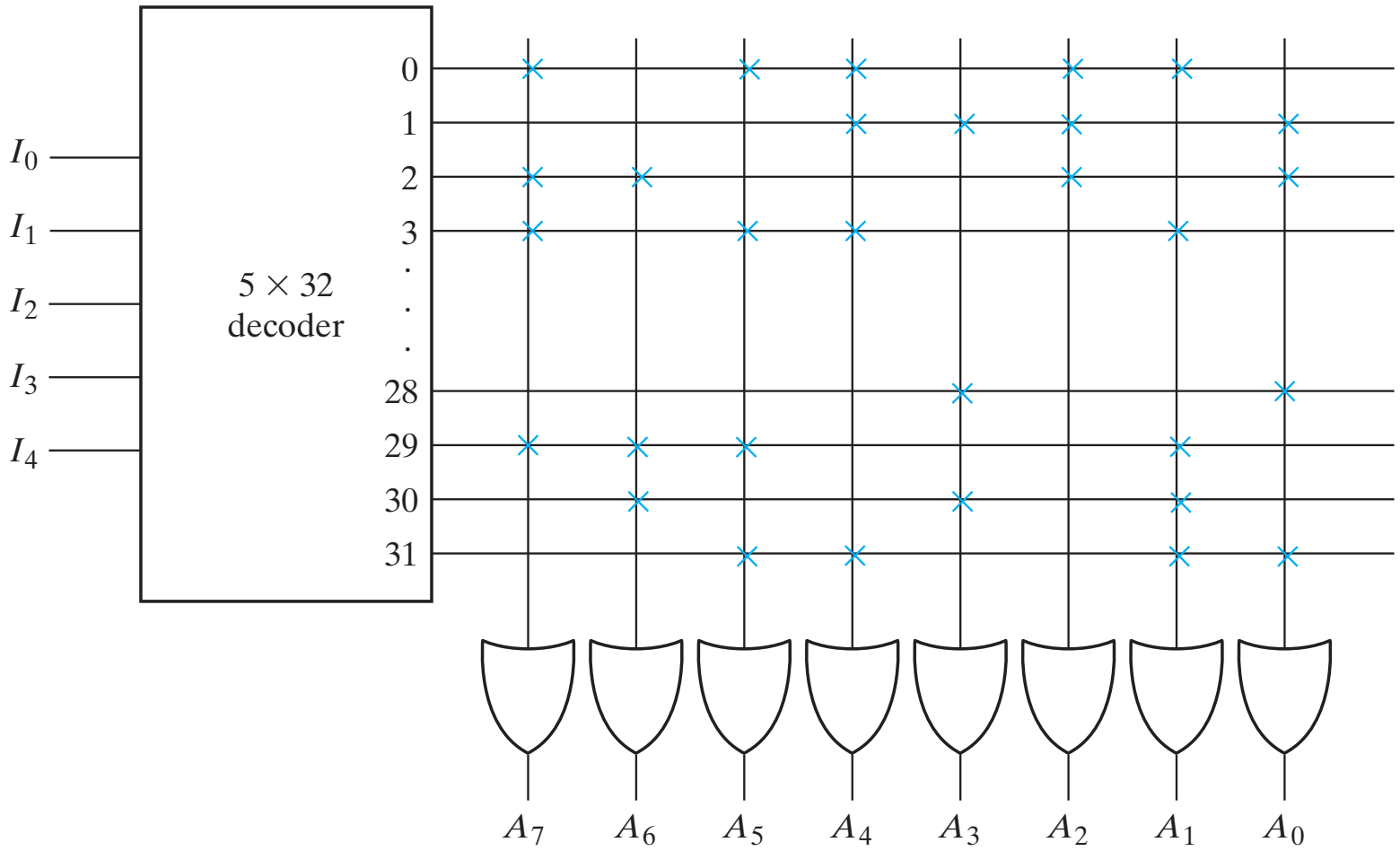
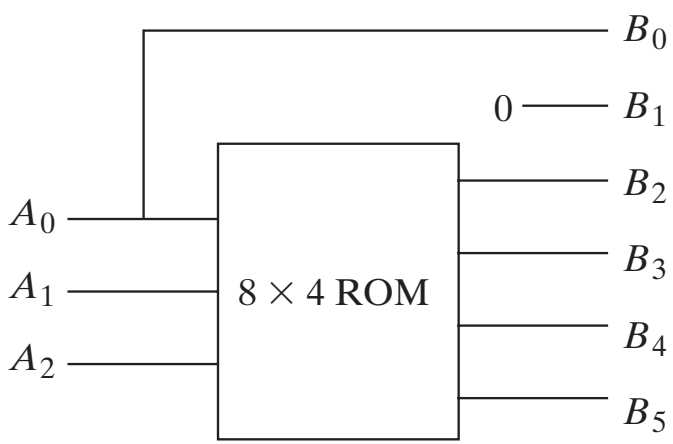


Fig. 7-11 Programming the ROM According to Table 7-3

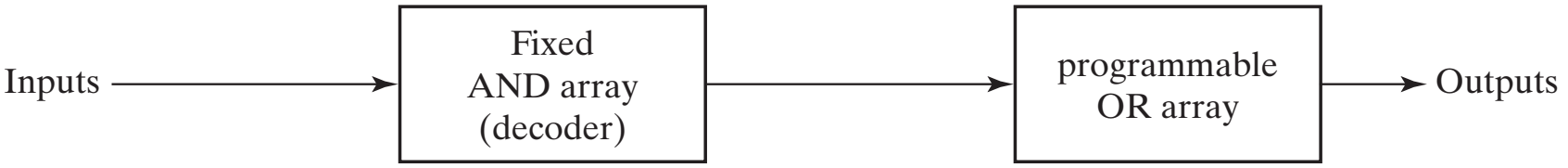


(a) Block diagram

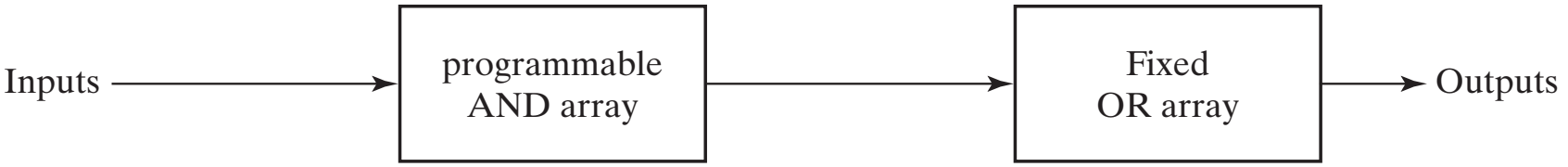
A_2	A_1	A_0	B_5	B_4	B_3	B_2
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	1
0	1	1	0	0	1	0
1	0	0	0	1	0	0
1	0	1	0	1	1	0
1	1	0	1	0	0	1
1	1	1	1	1	0	0

(b) ROM truth table

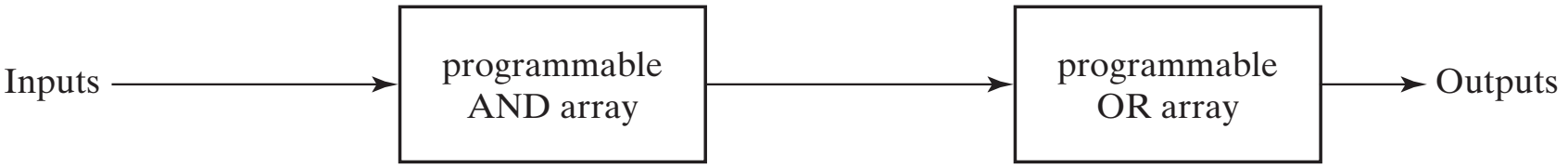
Fig. 7-12 ROM Implementation of Example 7-1



(a) Programmable read-only memory (PROM)



(b) Programmable array logic (PAL)



(c) Programmable logic array (PLA)

Fig. 7-13 Basic Configuration of Three PLDs

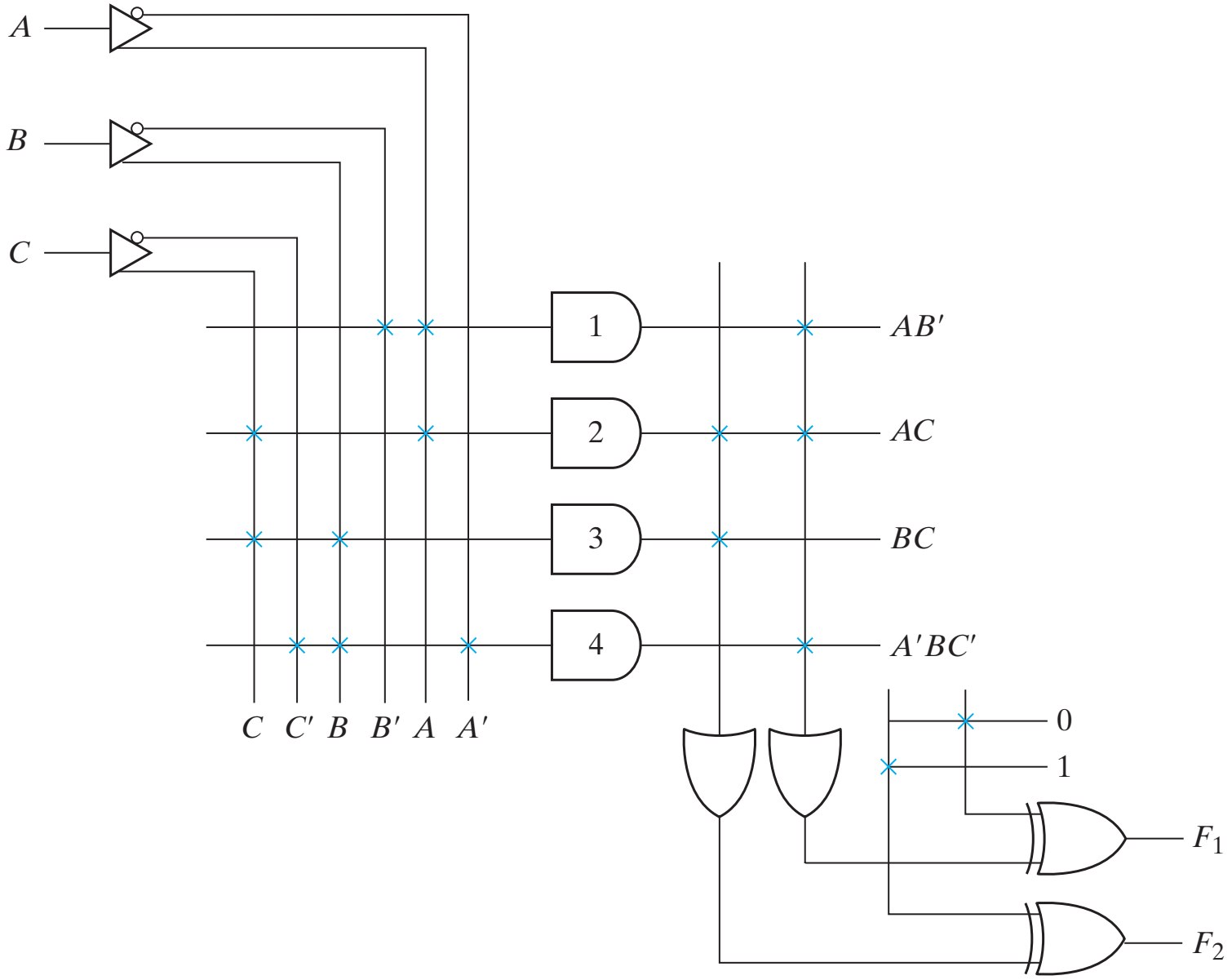


Fig. 7-14 PLA with 3 Inputs, 4 Product Terms, and 2 Outputs

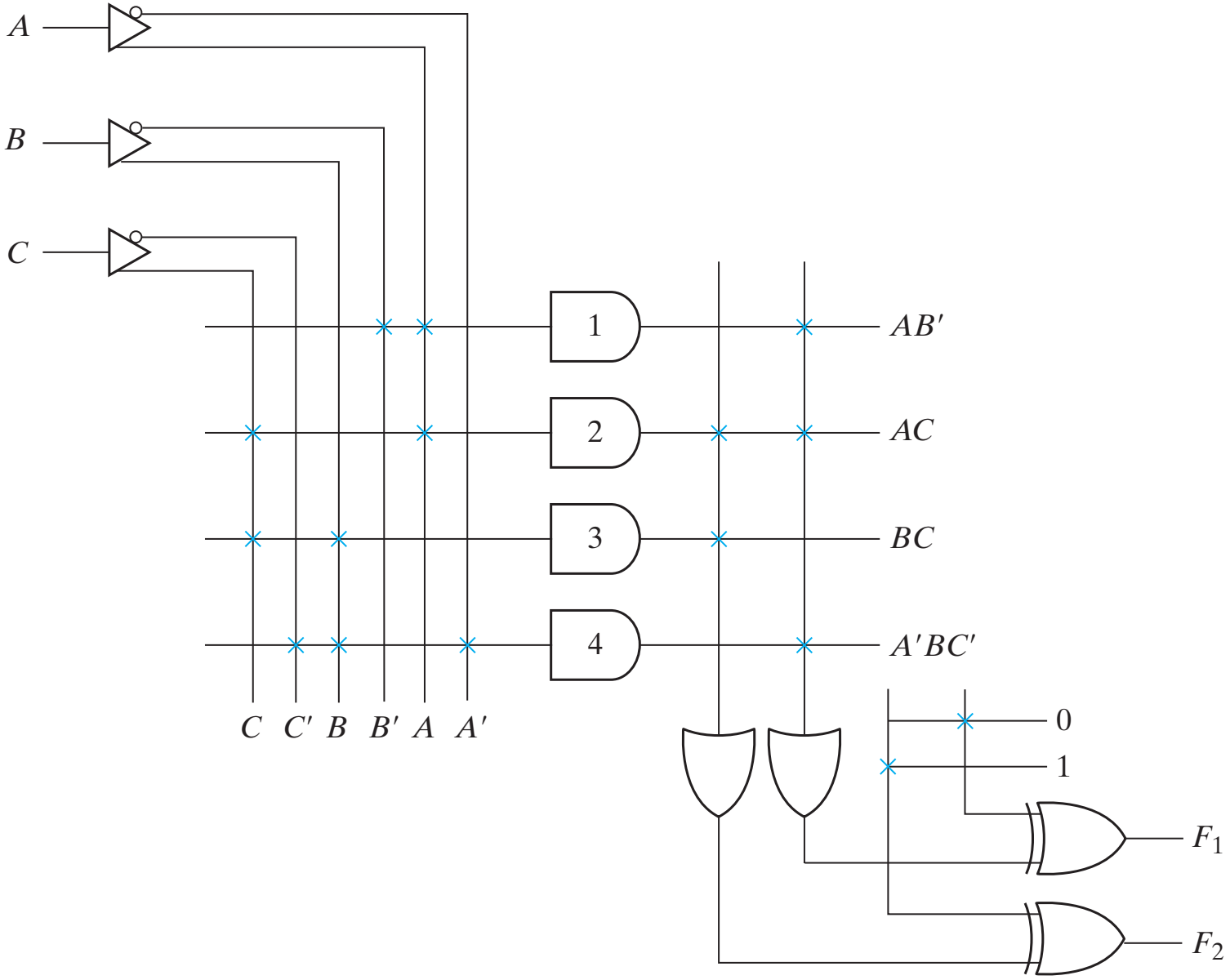
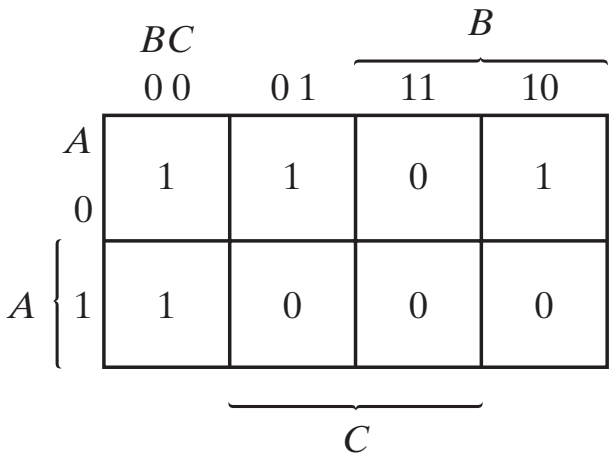
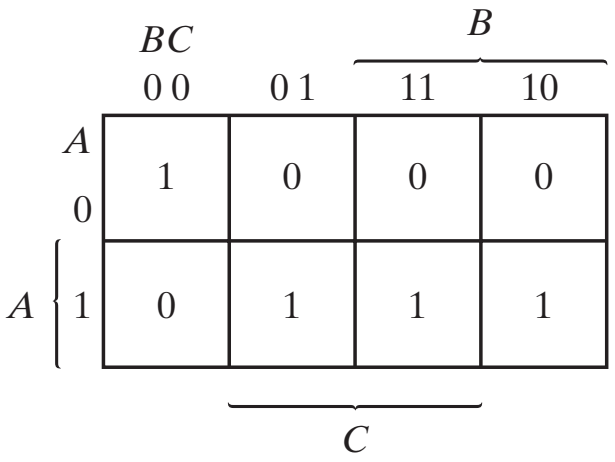


Fig. 7-14 PLA with 3 Inputs, 4 Product Terms, and 2 Outputs



$F_1 = A'B' + A'C' + B'C'$

$F_1 = (AB + AC + BC)'$



$F_2 = AB + AC + A'B'C'$

$F_2 = (A'C + A'B + AB'C')'$

PLA programming table

	Product term	Inputs A	B	C	Outputs (C) F_1	(T) F_2
AB	1	1	1	–	1	1
AC	2	1	–	1	1	1
BC	3	–	1	1	1	–
$A'B'C'$	4	0	0	0	–	1

Fig. 7-15 Solution to Example 7-2

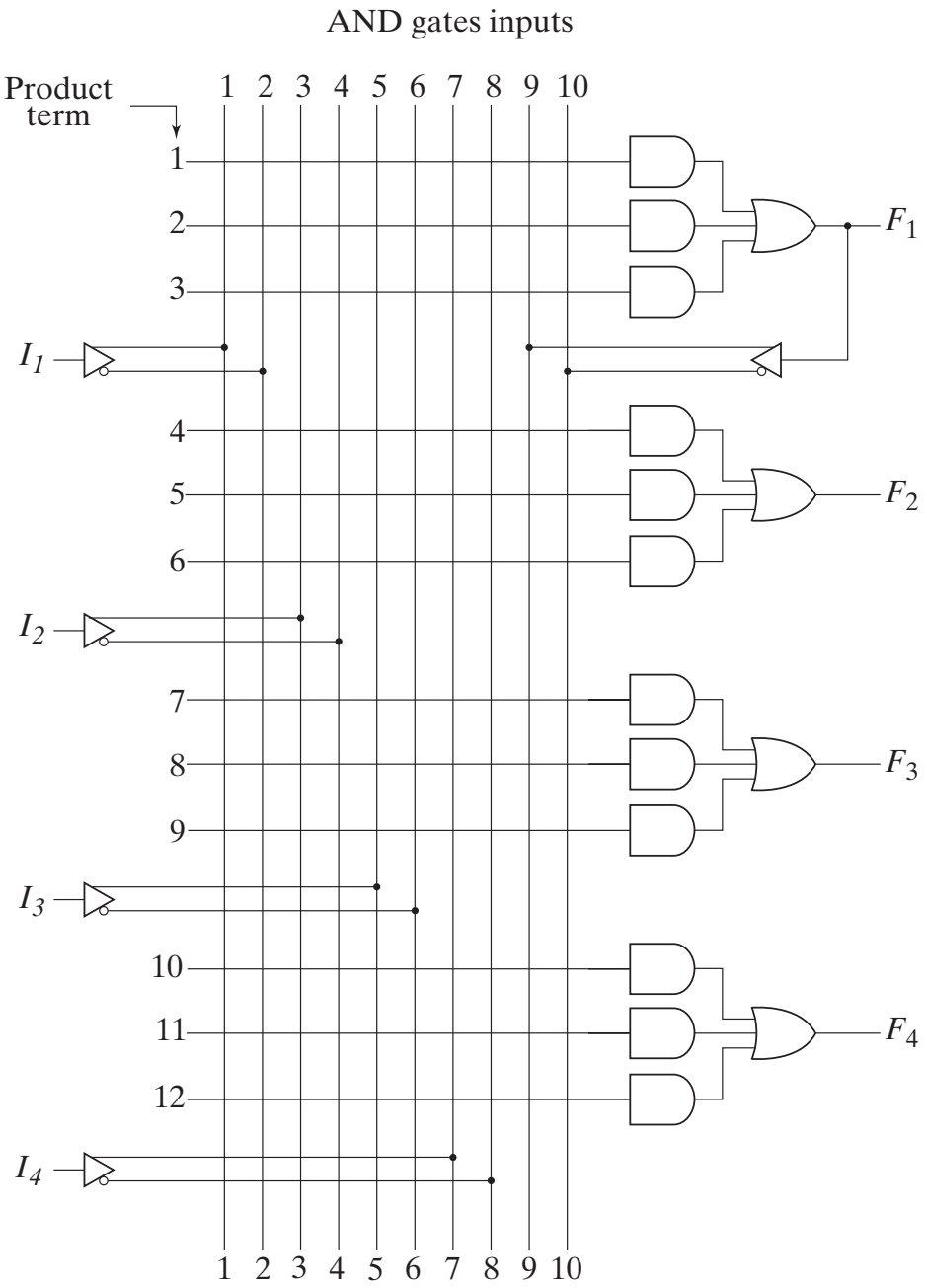


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Fig. 7-16 PAL with Four Inputs, Four Outputs, and Three-Wide AND-OR Structure

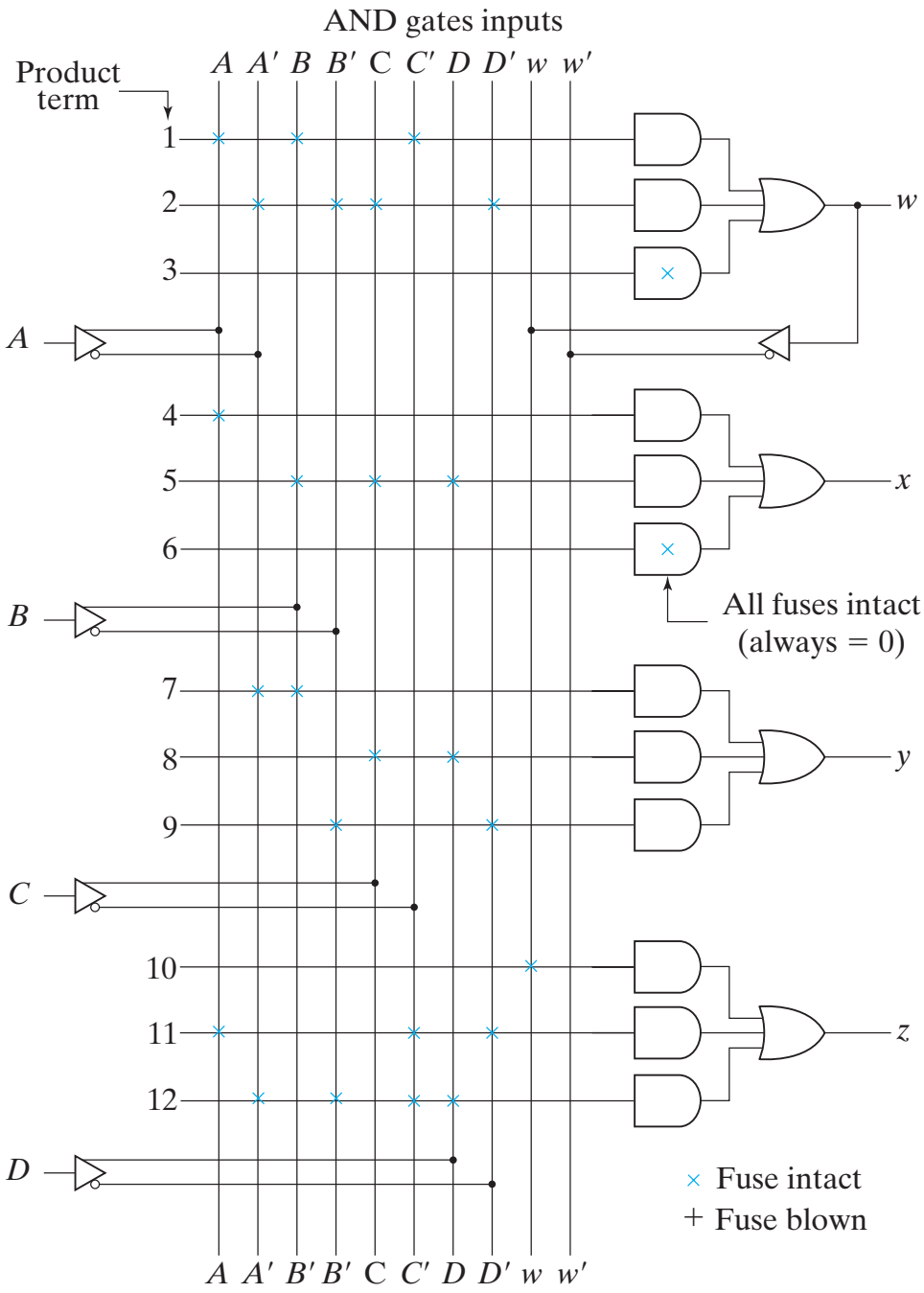

Fig. 7-17 Fuse Map for PAL as Specified in Table 7-6

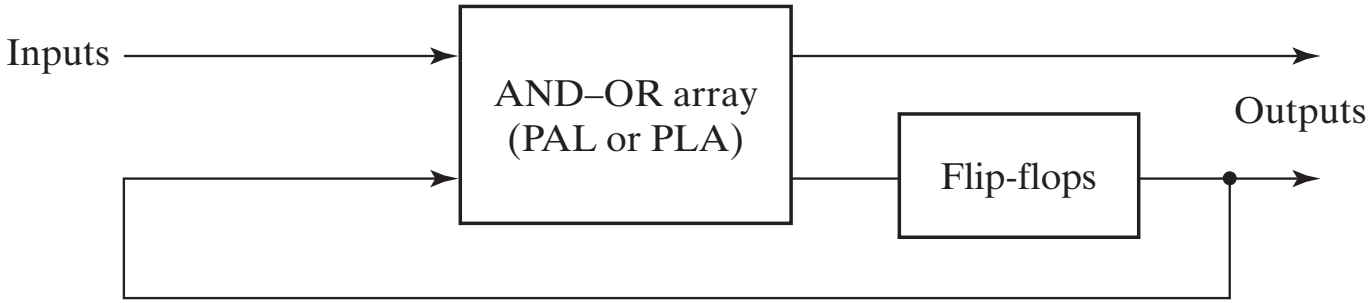

Fig. 7-18 Sequential Programmable Logic Device

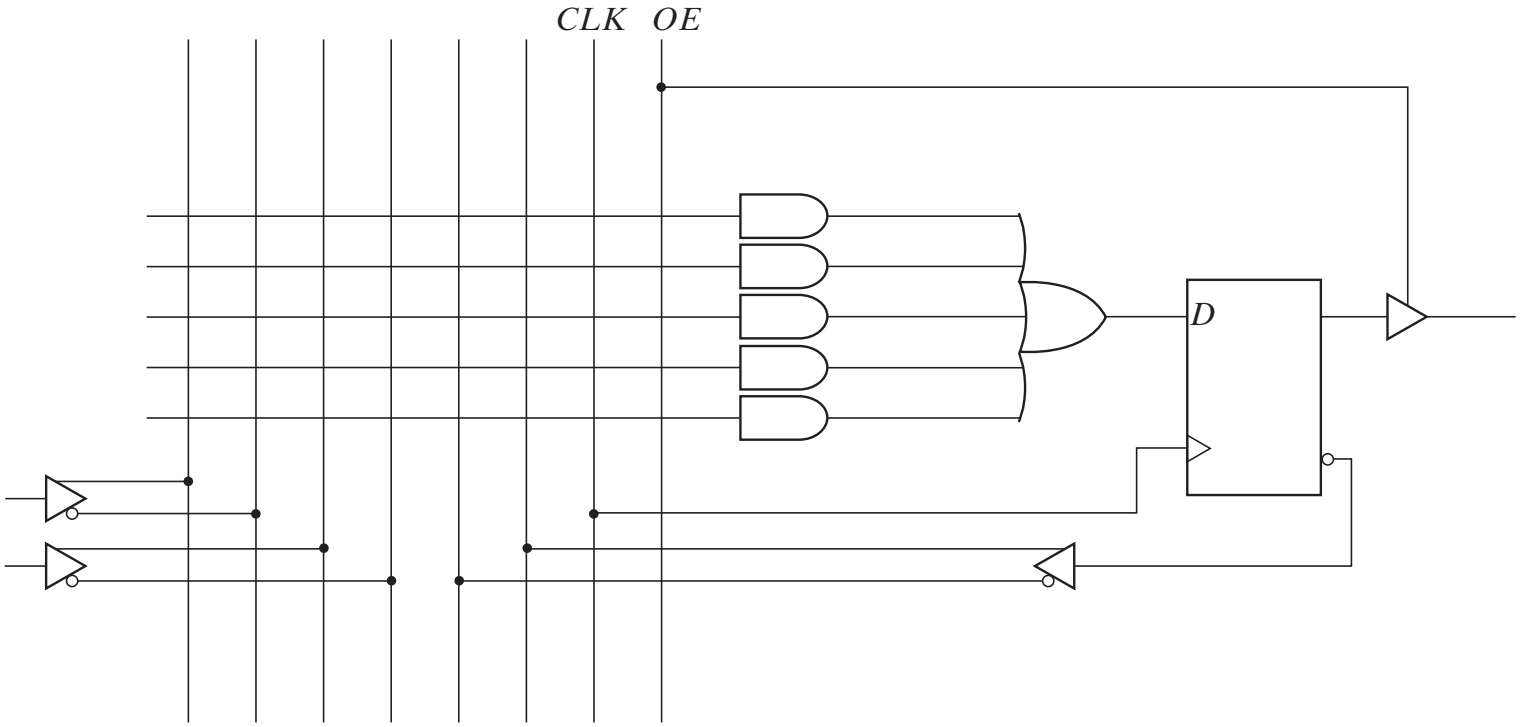

Fig. 7-19 Basic Macrocell Logic

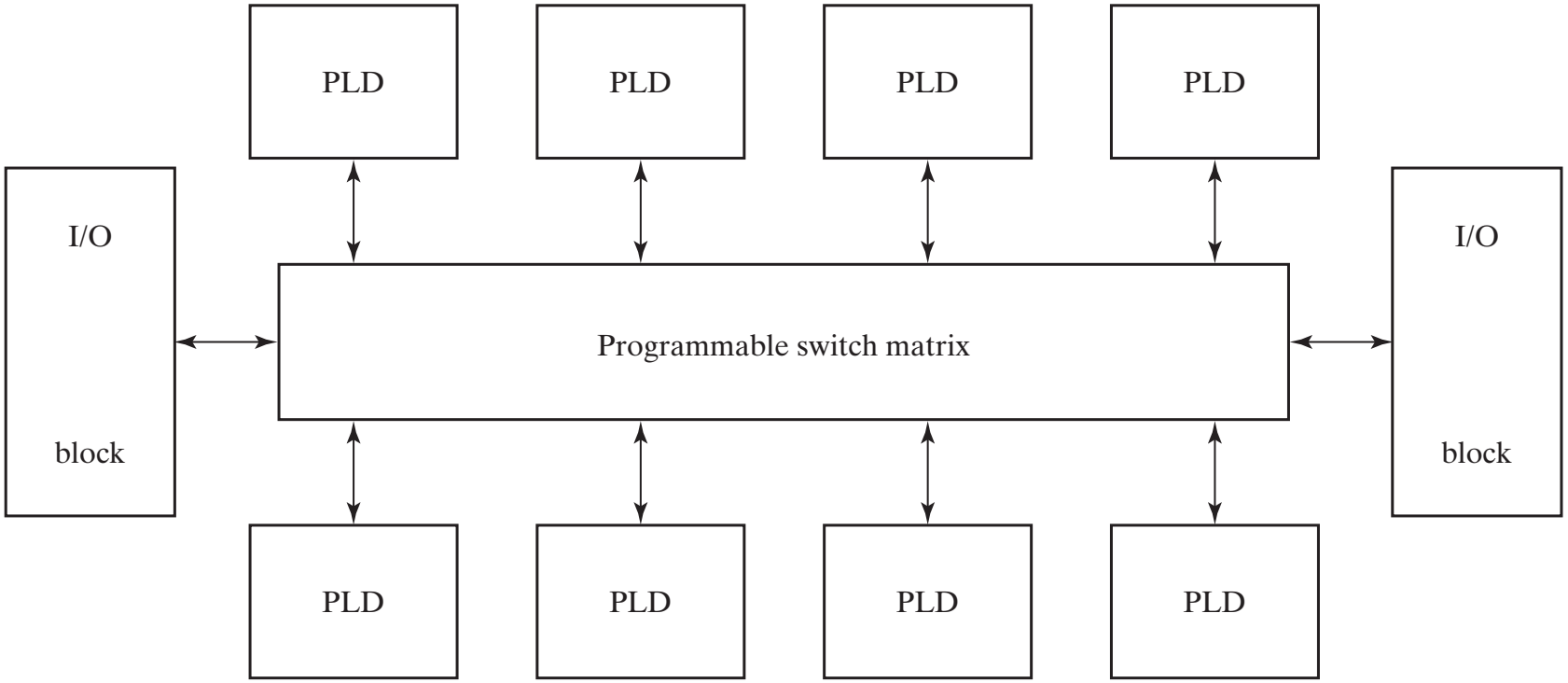

Fig. 7-20 General CPLD Configuration

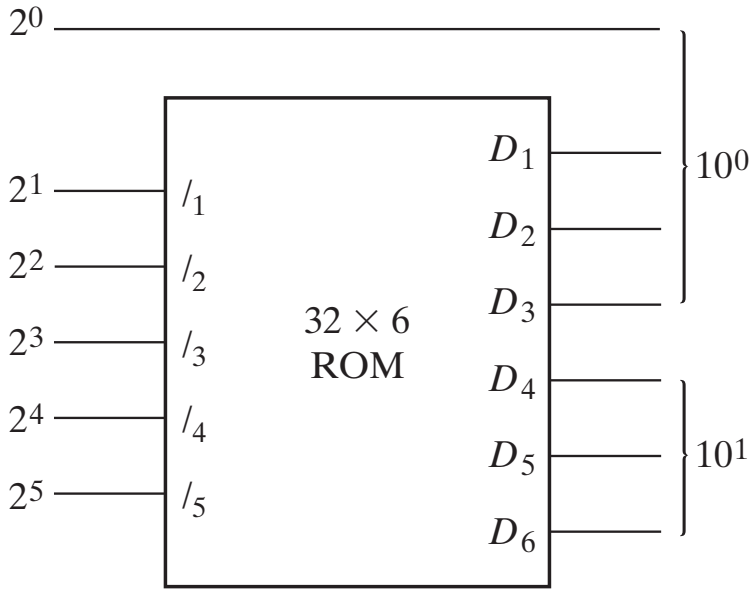

Fig. P7-17