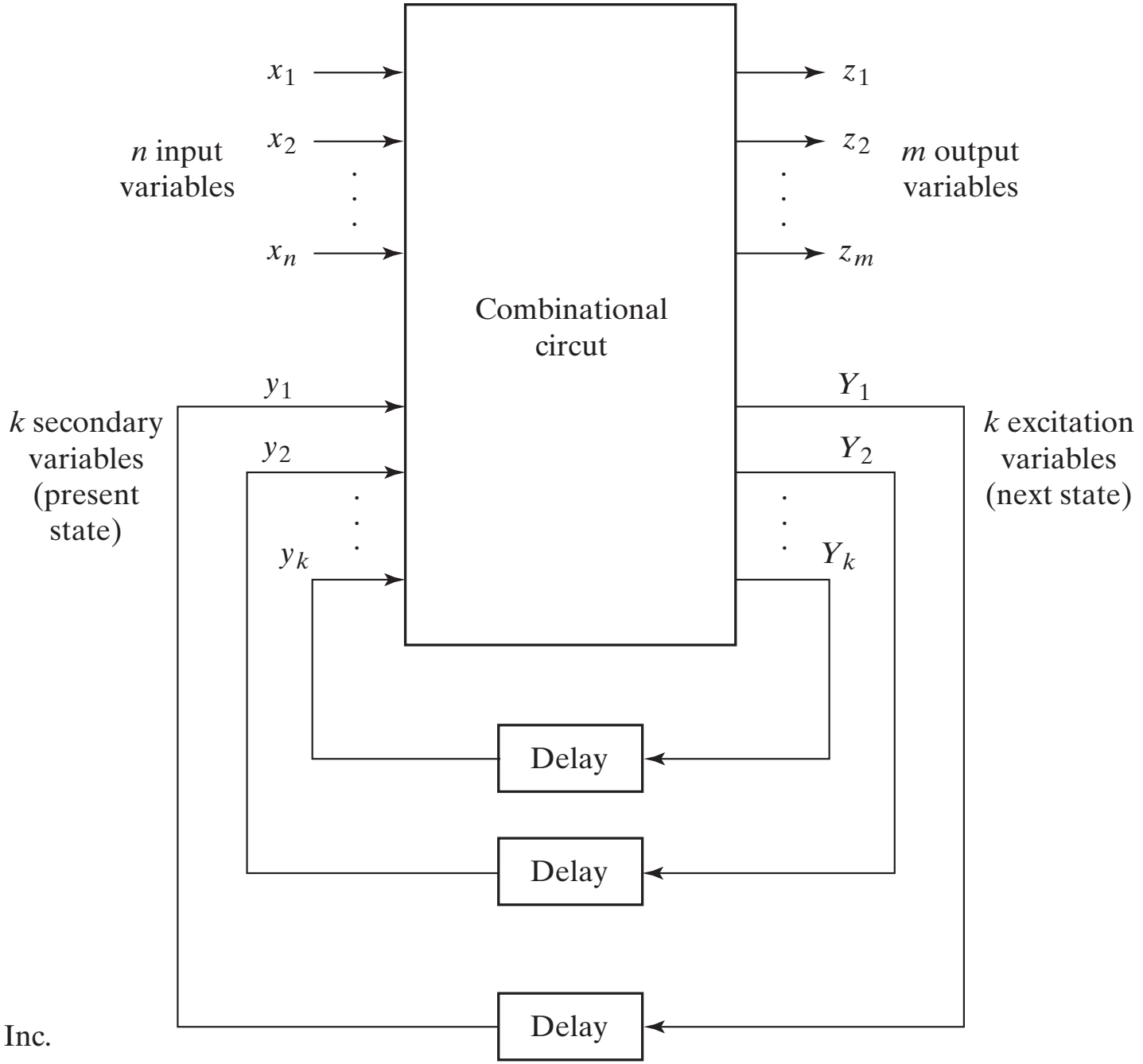


Fig. 9-1 Block Diagram of an Asynchronous Sequential Circuit

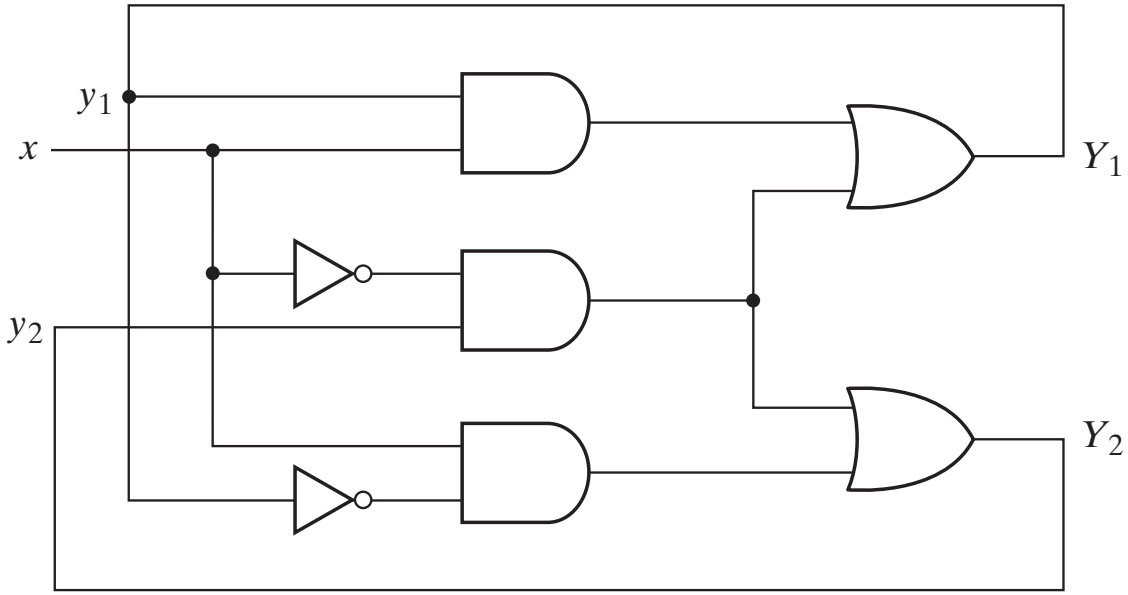
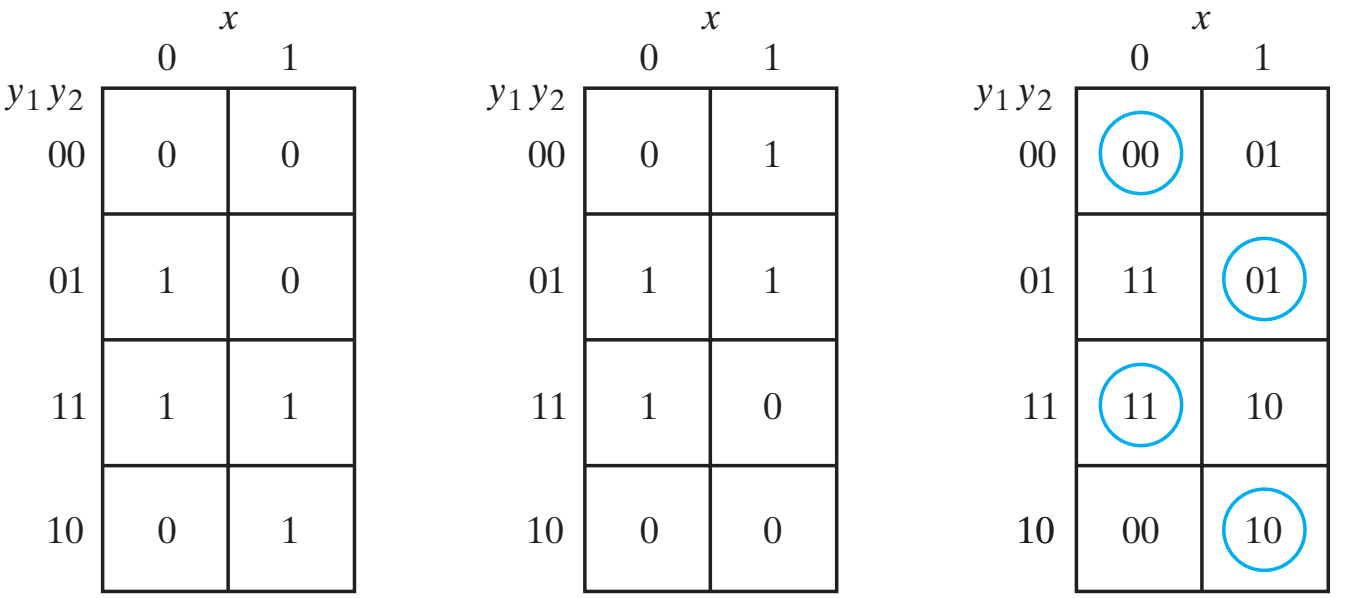


Fig. 9-2 Example of an Asynchronous Sequential Circuit

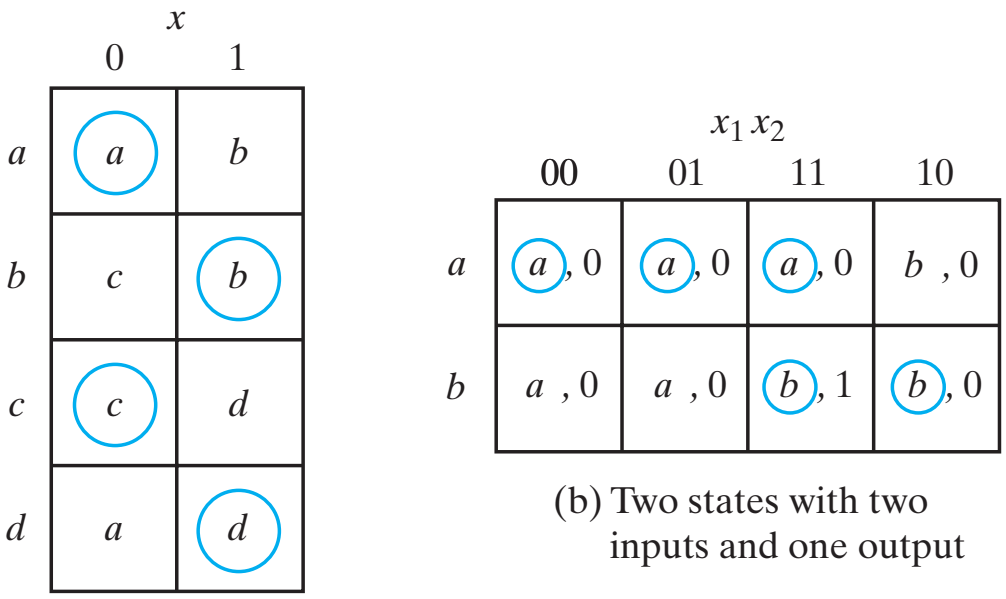


(a) Map for $Y_1 = xy_1 + x'y_2$

(b) Map for $Y_2 = xy'_1 + x'y_2$

(c) Transition table

Fig. 9-3 Maps and Transition Table for the Circuit of Fig. 9-2



	x = 0	x = 1
a	(a)	b
b	c	(b)
c	(c)	d
d	a	(d)

(a) Four states with one input

	x_1x_2 = 00	01	11	10
a	(a), 0	(a), 0	(a), 0	b , 0
b	a , 0	a , 0	(b), 1	(b), 0

(b) Two states with two inputs and one output

Fig. 9-4 Examples of Flow Tables

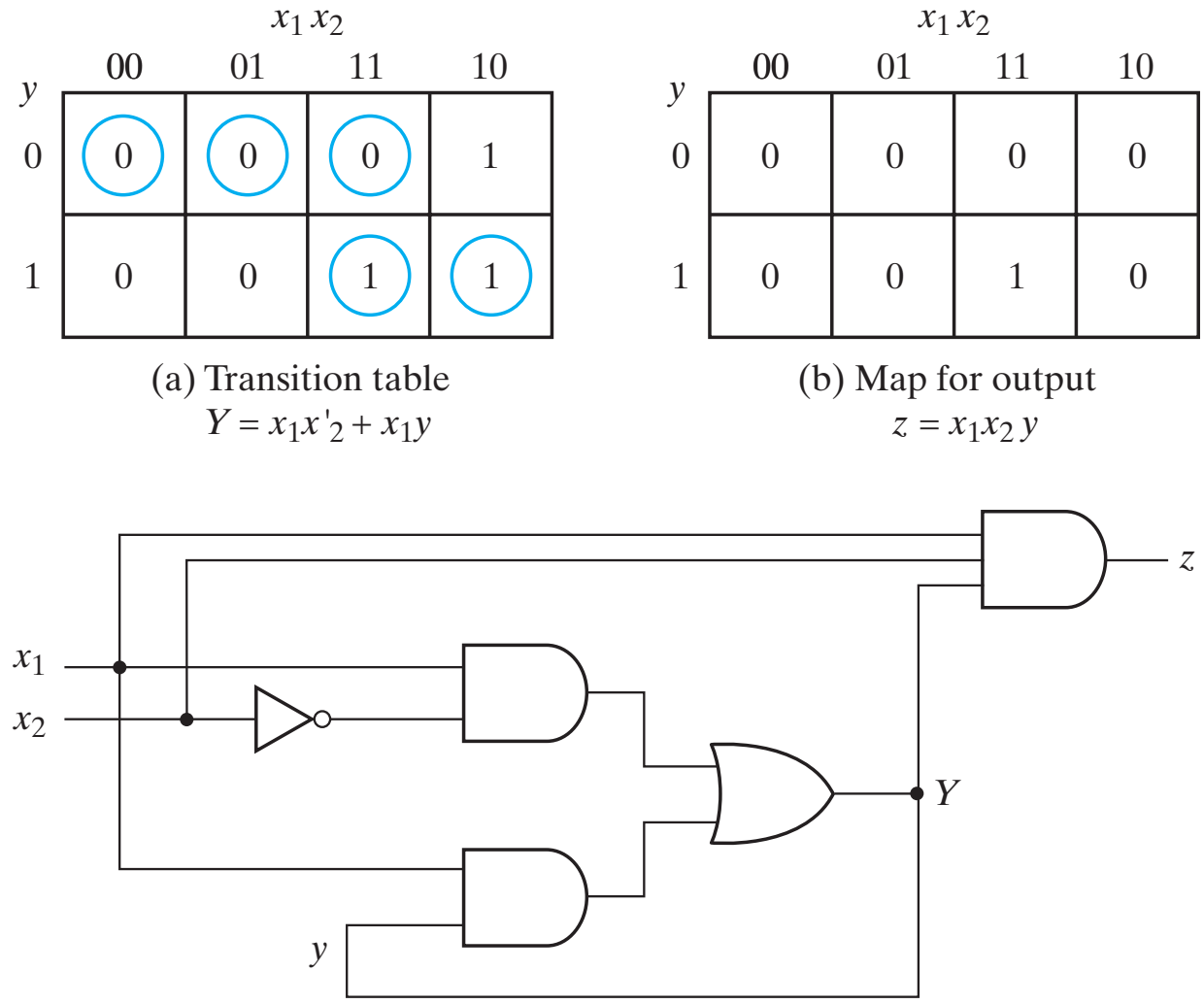
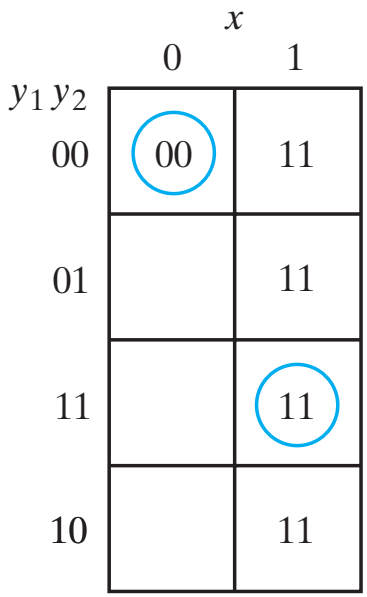
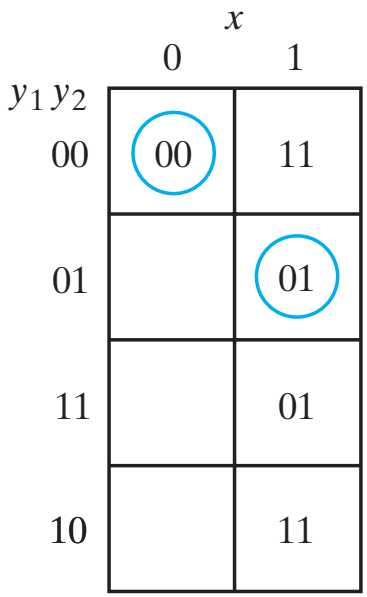


Fig. 9-5 Derivation of a Circuit Specified by the Flow Table of Fig. 9-4(b)



(a) Possible transitions:

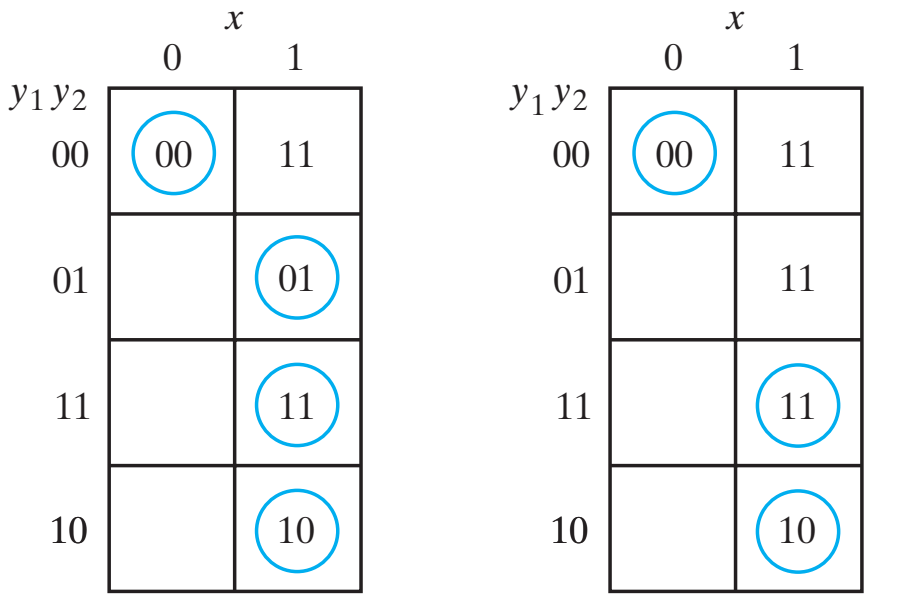
00 → 11
00 → 01 → 11
00 → 10 → 11



(b) Possible transitions:

00 → 11 → 01
00 → 01
00 → 10 → 11 → 01

Fig. 9-6 Examples of Noncritical Races



(a) Possible transitions:

00 → 11
00 → 01
00 → 10

(b) Possible transitions:

00 → 11
00 → 01 → 11
00 → 10

Fig. 9-7 Examples of Critical Races

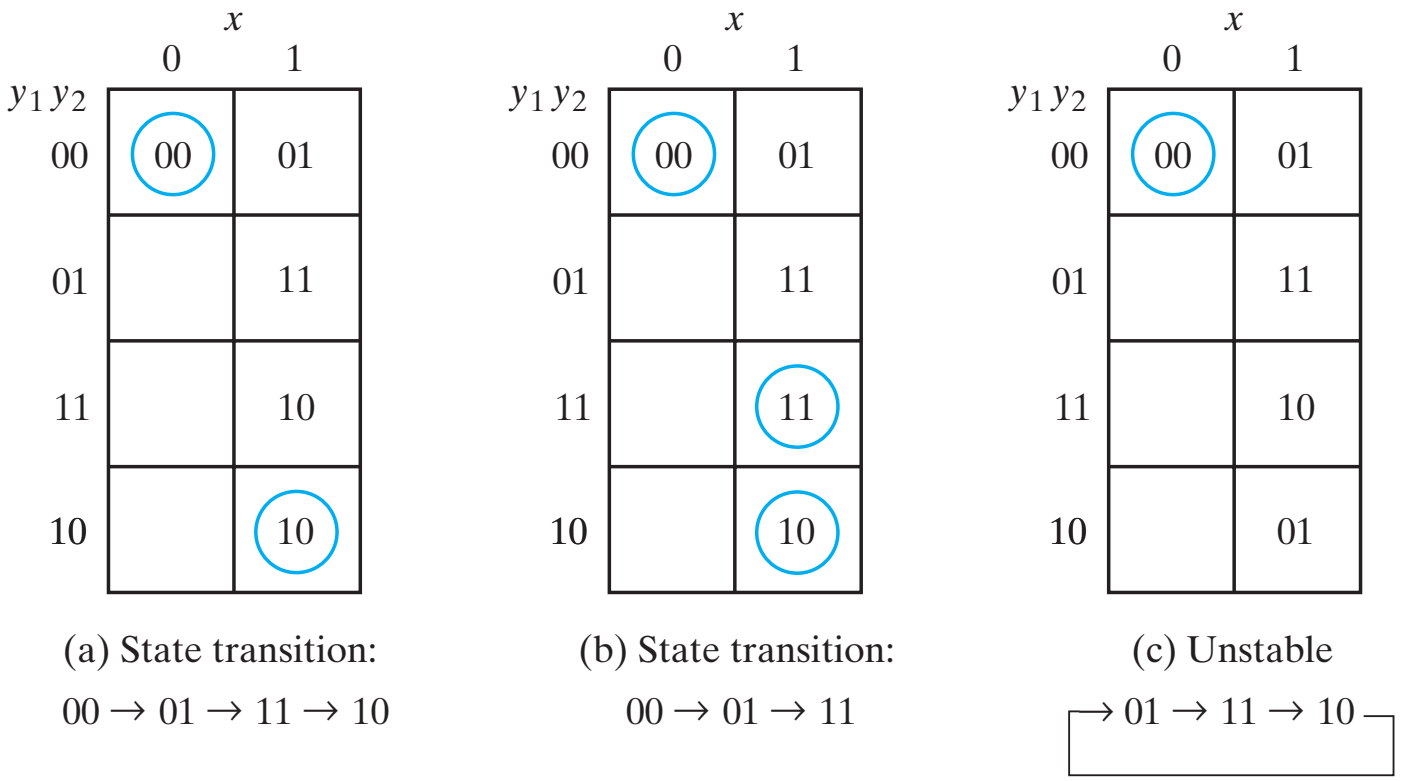
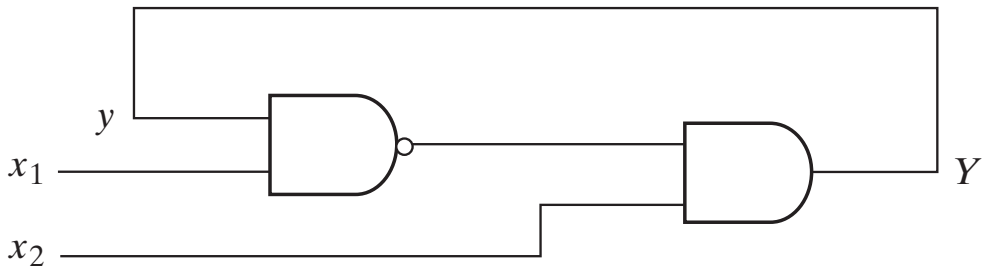


Fig. 9-8 Examples of Cycles

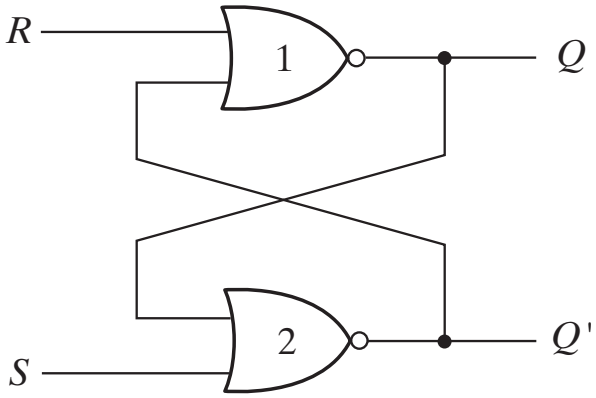


(a) Logic diagram

y \ $x_1 x_2$	00	01	11	10
0	(0)	1	1	(0)
1	0	(1)	0	0

(b) Transition table

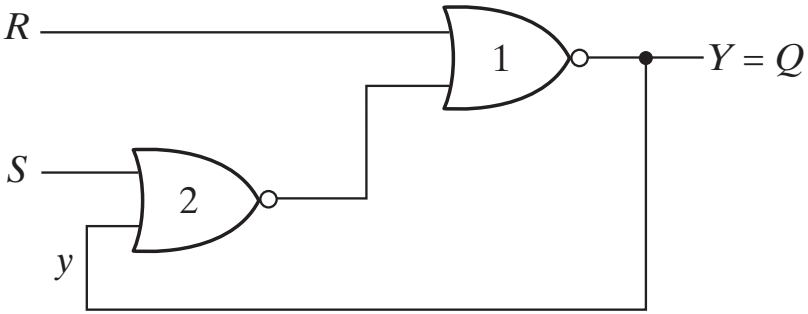
Fig. 9-9 Example of an Unstable Circuit



(a) Crossed-coupled circuit

S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(After $SR = 10$)
0	1	0	1	
0	0	0	1	(After $SR = 01$)
1	1	0	0	

(b) Truth table



(c) Circuit showing feedback

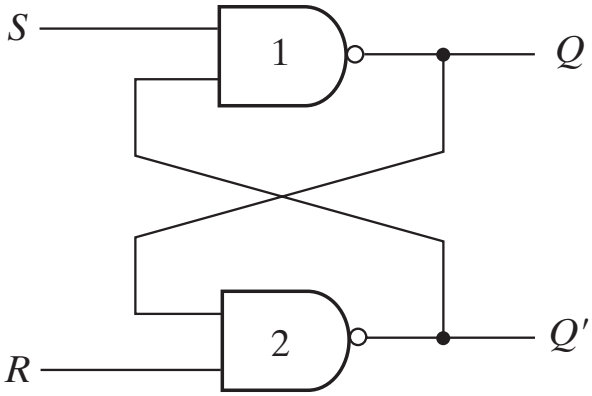
	SR			
y	00	01	11	10
0	0	0	0	1
1	1	0	0	1

$Y = SR' + R'y$

$Y = S + R'y$ when $SR = 0$

(d) Transition table

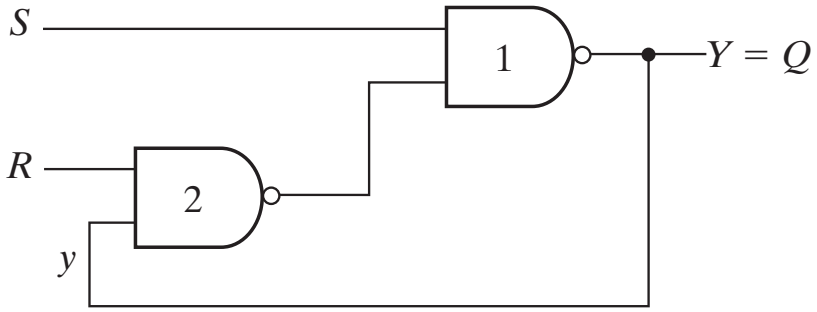
Fig. 9-10 *SR* Latch with NOR Gates



(a) Crossed-coupled circuit

S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(After $SR = 10$)
0	1	1	0	
1	1	1	0	(After $SR = 01$)
0	0	1	1	

(b) Truth table



(c) Circuit showing feedback

y	00	01	11	10
0	1	1	0	0
1	1	1	1	0

SR

$Y = S' + Ry$ when $S'R' = 0$

(d) Transition table

Fig. 9-11 *SR* Latch with NAND Gates

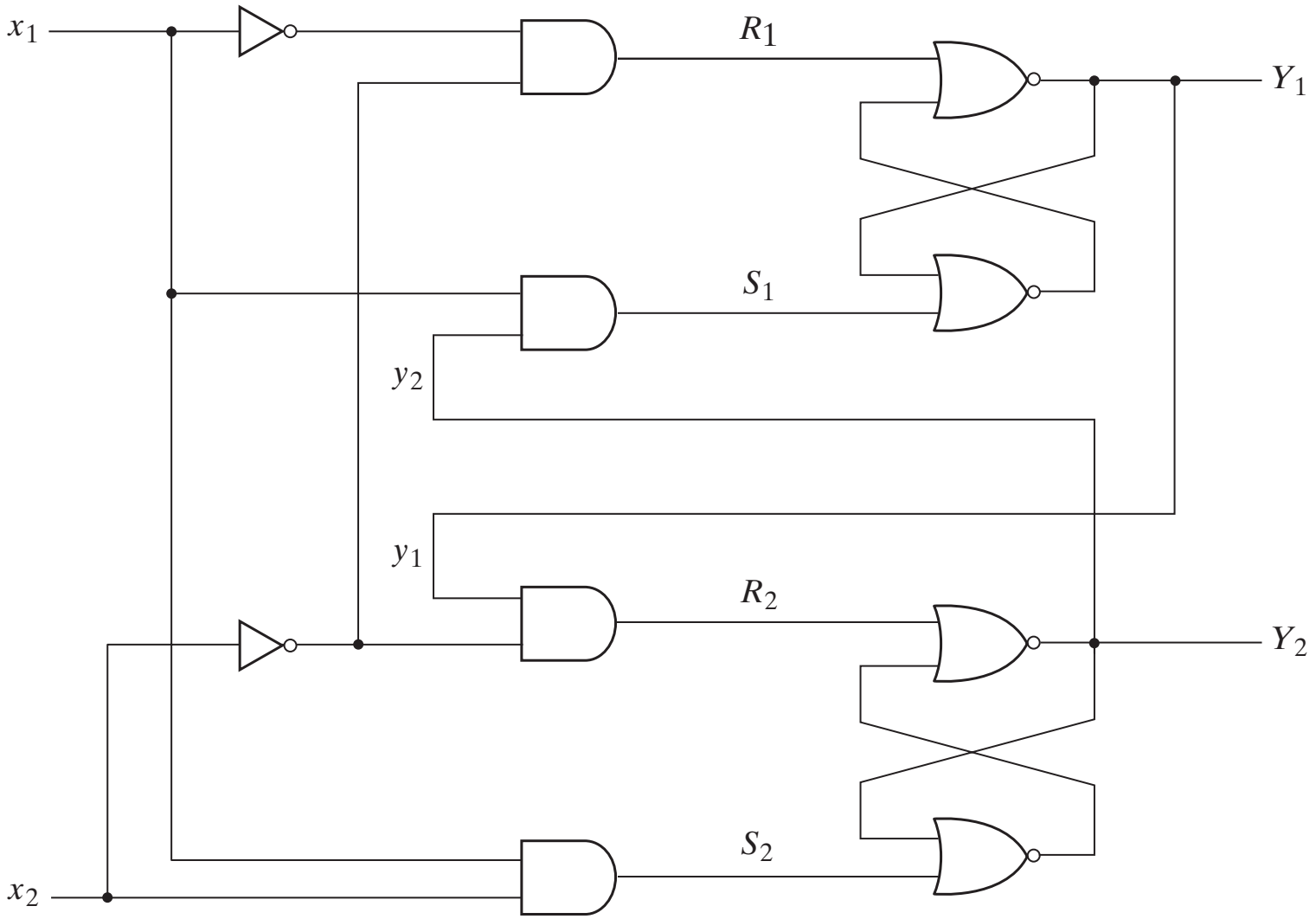


Fig. 9-12 Example of a Circuit with *SR* Latches

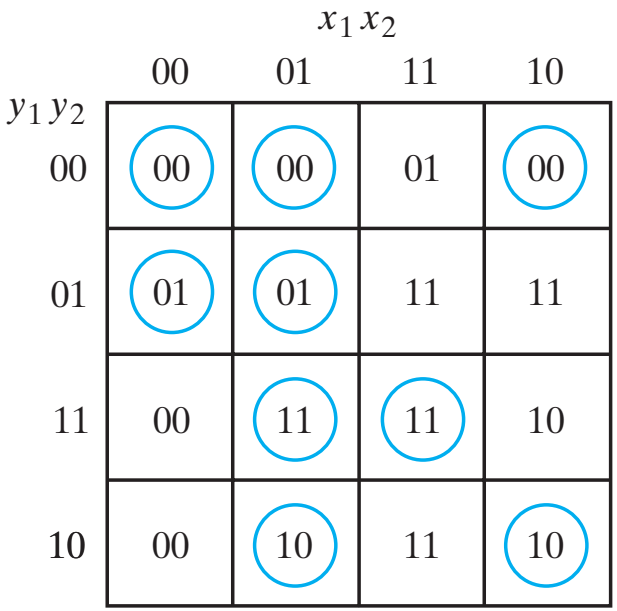


Fig. 9-13 Transition Table for the Circuit of Fig. 9-12

y \ x_1x_2	00	01	11	10
0	(0)	(0)	(0)	1
1	0	0	(1)	(1)

(a) Transition table

$Y = x_1x'_2 + x_1y$

y	Y	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	1

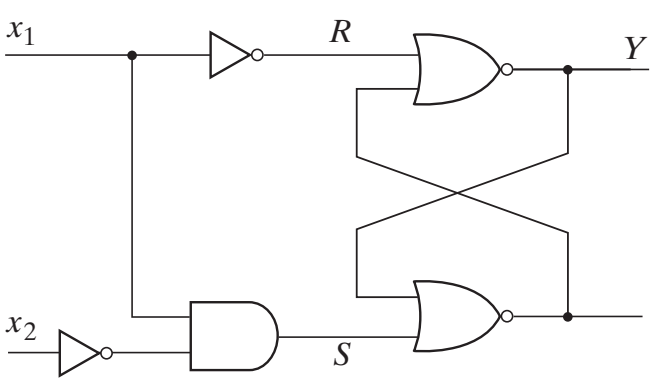
(b) Latch excitation table

y \ x_1x_2	00	01	11	10
0	0	0	0	1
1	0	0	X	X

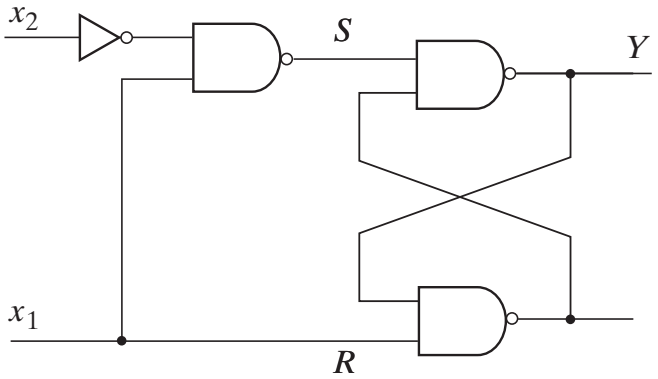
(c) Map for $S = x_1x'_2$

y \ x_1x_2	00	01	11	10
0	X	X	X	0
1	1	1	0	0

(d) Map for $R = x'_1$



(e) Circuit with NOR latch



(f) Circuit with NAND latch

Fig. 9-14 Derivation of a Latch Circuit from a Transition Table

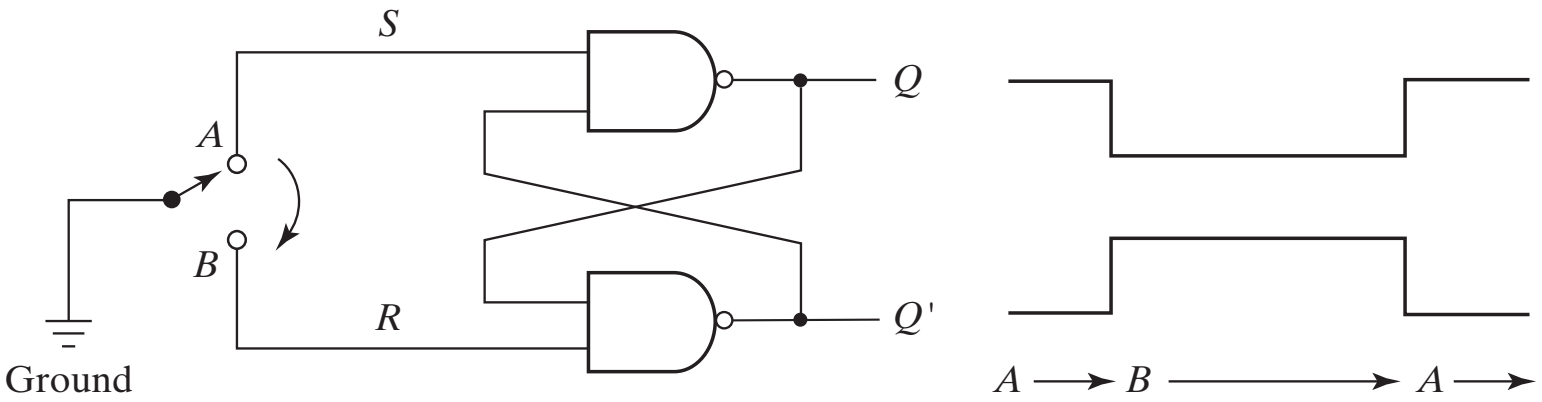
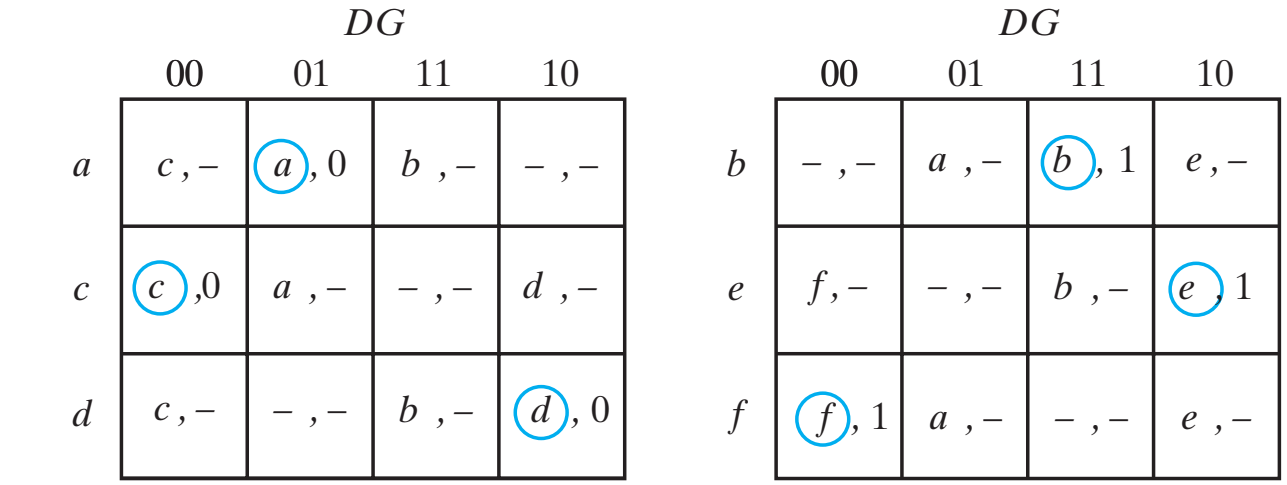


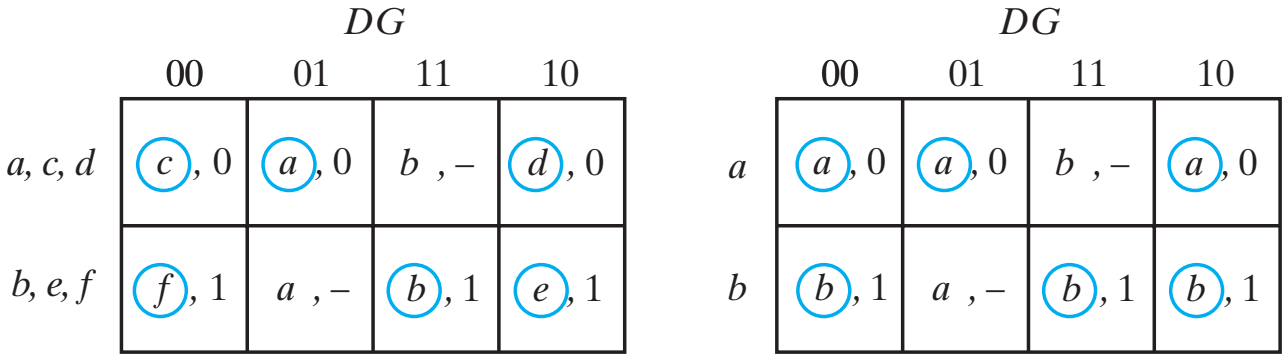
Fig. 9-15 Debounce Circuit

	DG = 00	DG = 01	DG = 11	DG = 10
a	c, –	(*a*), 0	b, –	–, –
b	–, –	a, –	(*b*), 1	e, –
c	(*c*), 0	a, –	–, –	d, –
d	c, –	–, –	b, –	(*d*), 0
e	f, –	–, –	b, –	(*e*), 1
f	(*f*), 1	a, –	–, –	e, –

Fig. 9-16 Primitive Flow Table

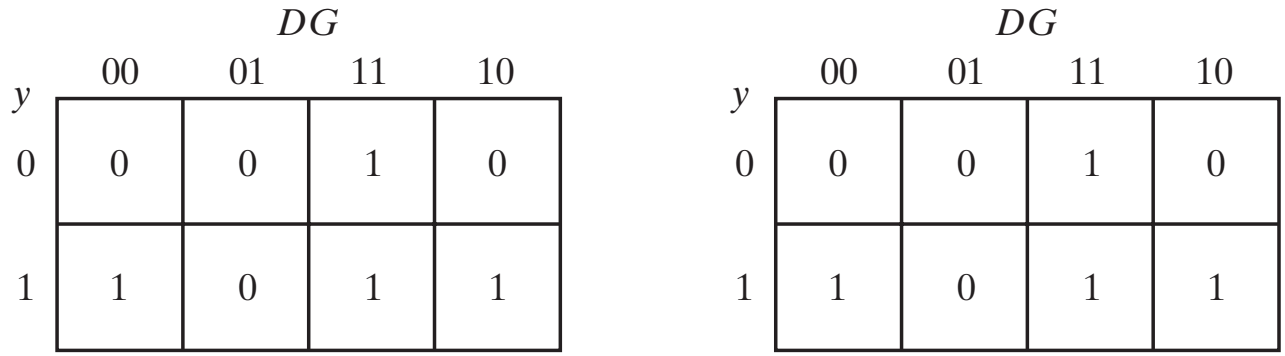


(a) States that are candidates for merging



(b) Reduced table (two alternatives)

Fig. 9-17 Reduction of the Primitive Flow Table



(a) $Y = DG + G'y$ (b) $Q = Y$

Fig. 9-18 Transition Table and Output Map for Gated Latch

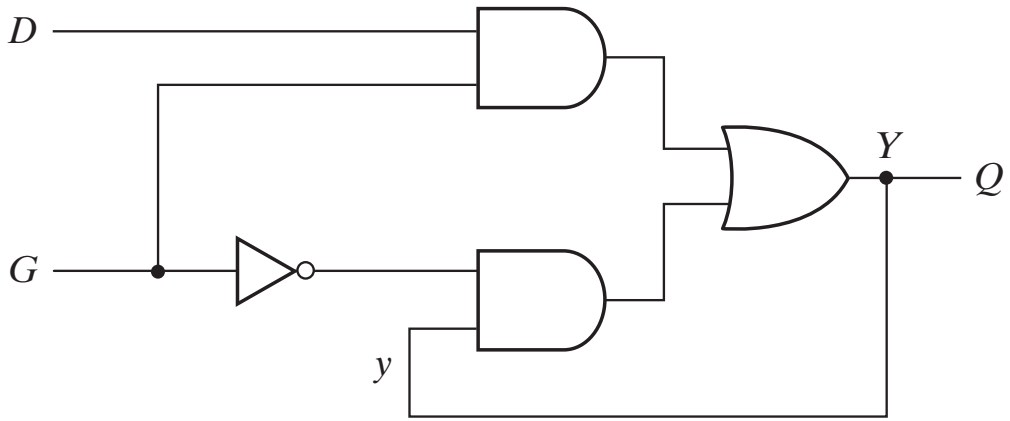
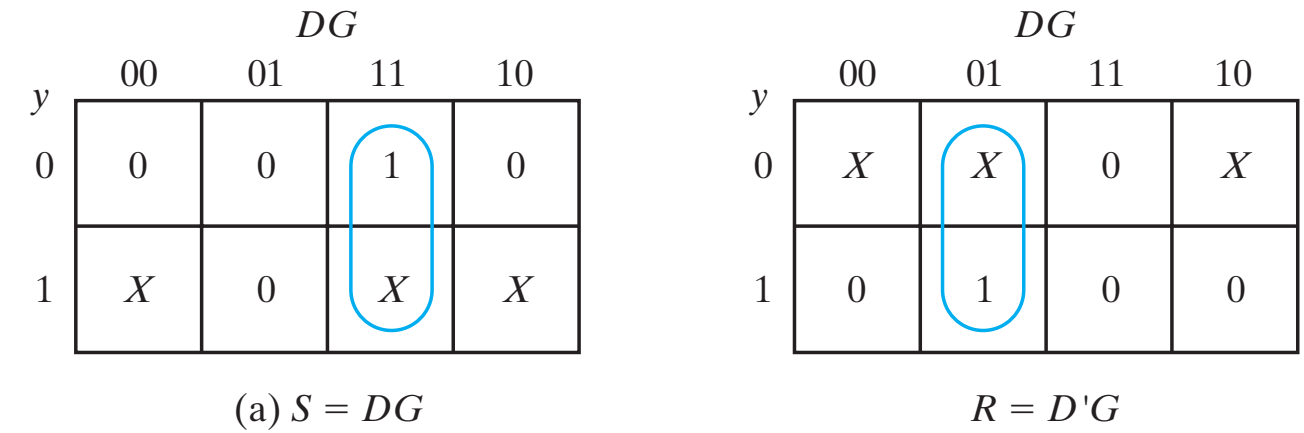
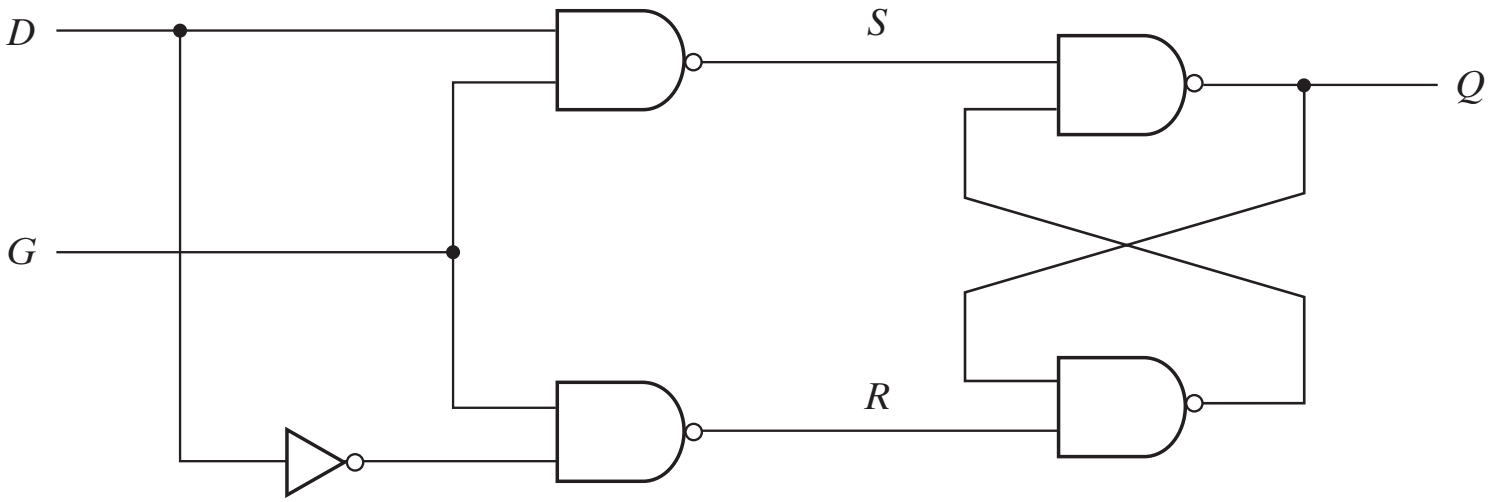


Fig. 9-19 Gated-Latch Logic Diagram



(a) Maps for S and R



(b) Logic diagram

FIG. 9-20 Circuit with SR Latch

a	(*a*), 0	*b* , –
b	*c* , –	(*b*), 0
c	(*c*), 1	*d* , –
d	*a* , –	(*d*), 1

(a) Flow table

0	0
X	0
1	1
X	1

(b) Output assignment

Fig. 9-21 Assigning Output Values to Unstable States

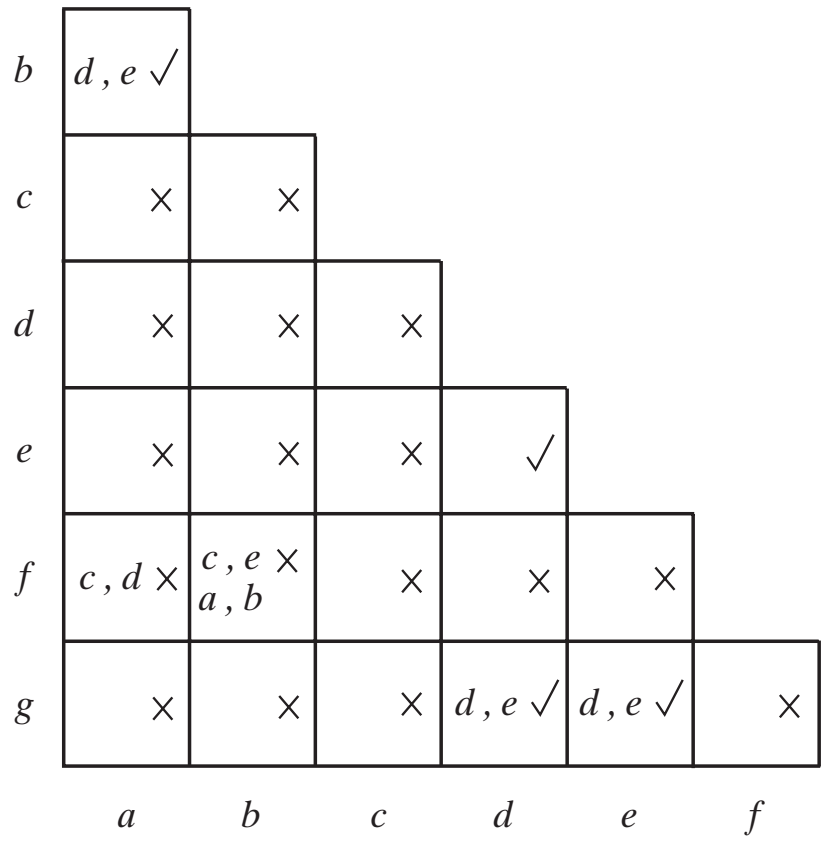


Fig. 9-22 Implication Table

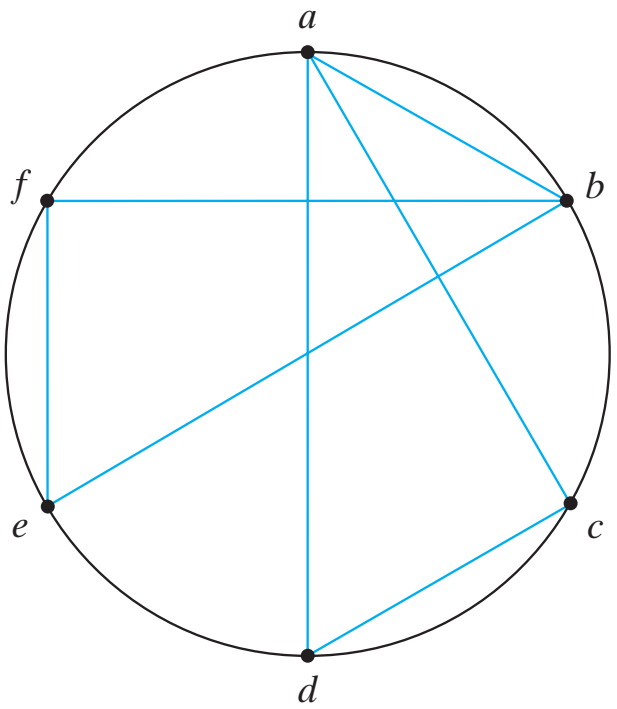
	00	01	11	10
a	*c* , –	(*a*), 0	*b* , –	– , –
b	– , –	*a* , –	(*b*), 1	*e* , –
c	(*c*), 0	*a* , –	– , –	*d* , –
d	*c* , –	– , –	*b* , –	(*d*), 0
e	*f* , –	– , –	*b* , –	(*e*), 1
f	(*f*), 1	*a* , –	– , –	*e* , –

(a) Primitive flow table

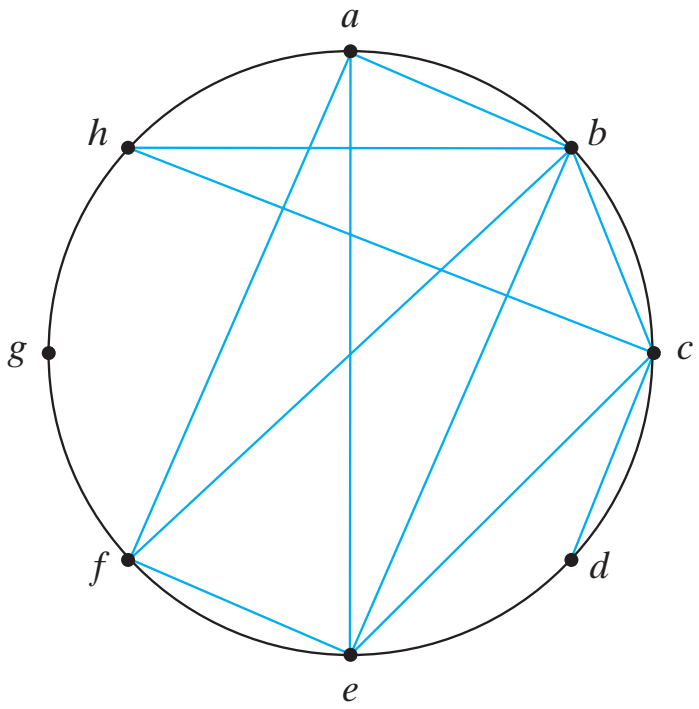
	a	*b*	*c*	*d*	*e*
b	✓				
c	✓	*d* , *e* ×			
d	✓	*d* , *e* ×	✓		
e	*c* , *f* ×	✓	*d* , *e* × *c* , *f* ×	×	
f	*c* , *f* ×	✓	×	*d* , *e* × *c* , *f* ×	✓

(b) Implication table

Fig. 9-23 Flow and Implication Tables

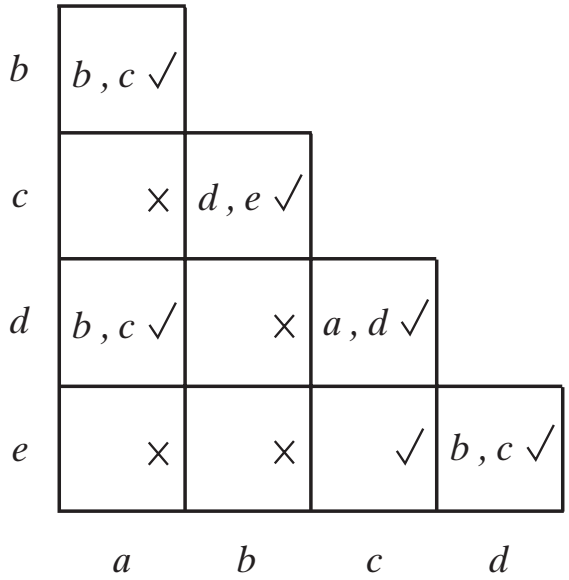


(a) Maximal compatible:
$(a, b,)$ (a, c, d) (b, e, f)

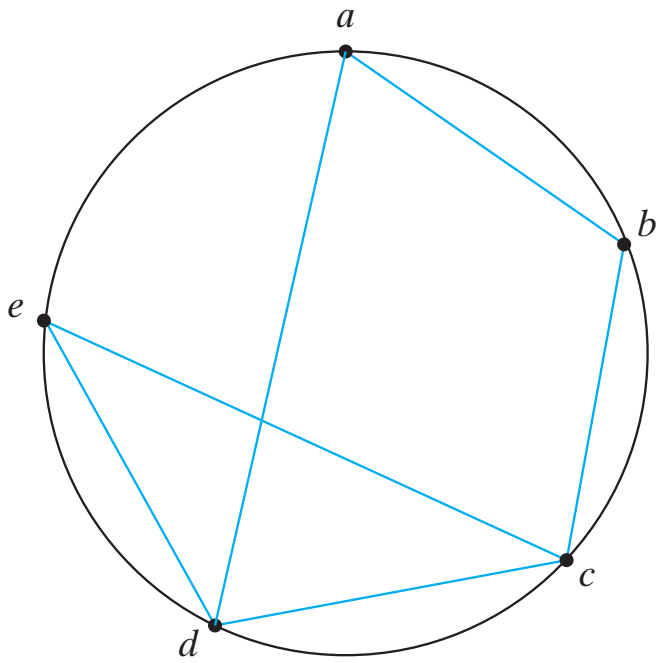


(b) Maximal compatible:
(a, b, e, f) (b, c, h) (c, d) (g)

Fig. 9-24 Merger Diagrams



(a) Implication table

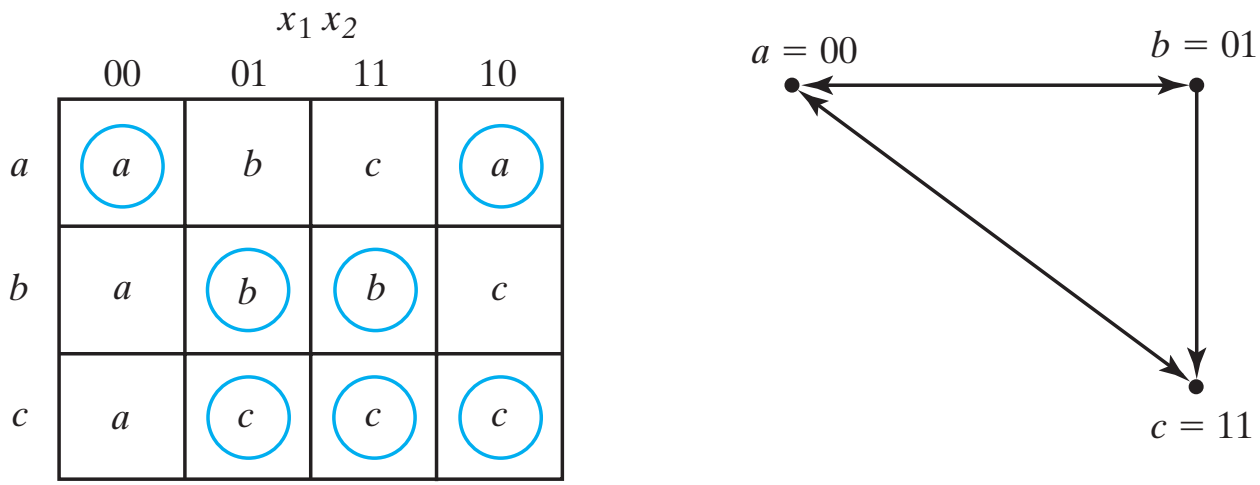


(b) Merger diagram

Compatibles	*(a, b)*	*(a, d)*	*(b, c)*	*(c, d, e)*
Implied states	*(b, c)*	*(b, c)*	*(d, e)*	*(a, d,)* *(b, c,)*

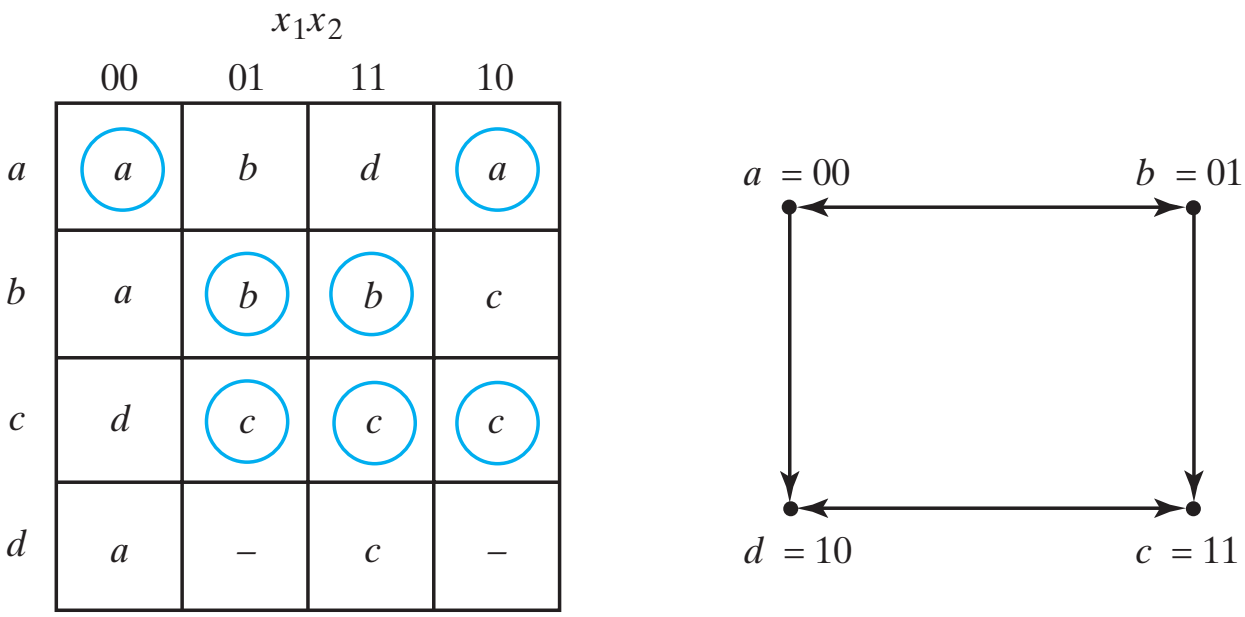
(c) Closure table

Fig. 9-25 Choosing a Set of Compatibles



(a) Flow table (b) Transition diagram

Fig. 9-26 Three-Row Flow-Table Example



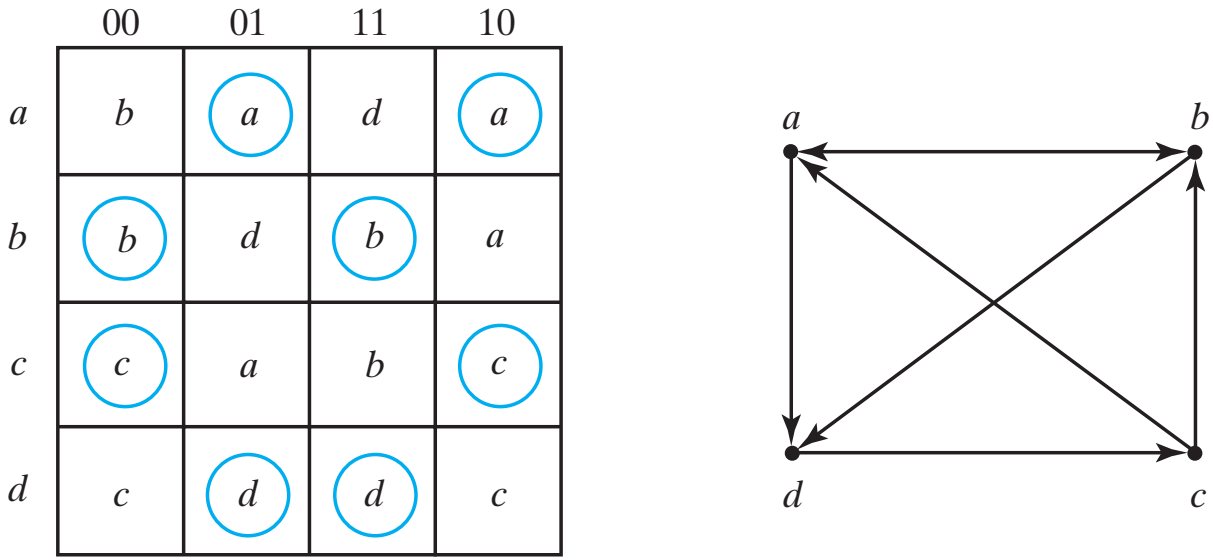
(a) Flow table

(b) Transition diagram

Fig. 9-27 Flow Table with an Extra Row

	x_1x_2 = 00	01	11	10
$a = 00$	(00)	01	10	(00)
$b = 01$	00	(01)	(01)	11
$c = 11$	10	(11)	(11)	(11)
$d = 10$	00	–	11	–

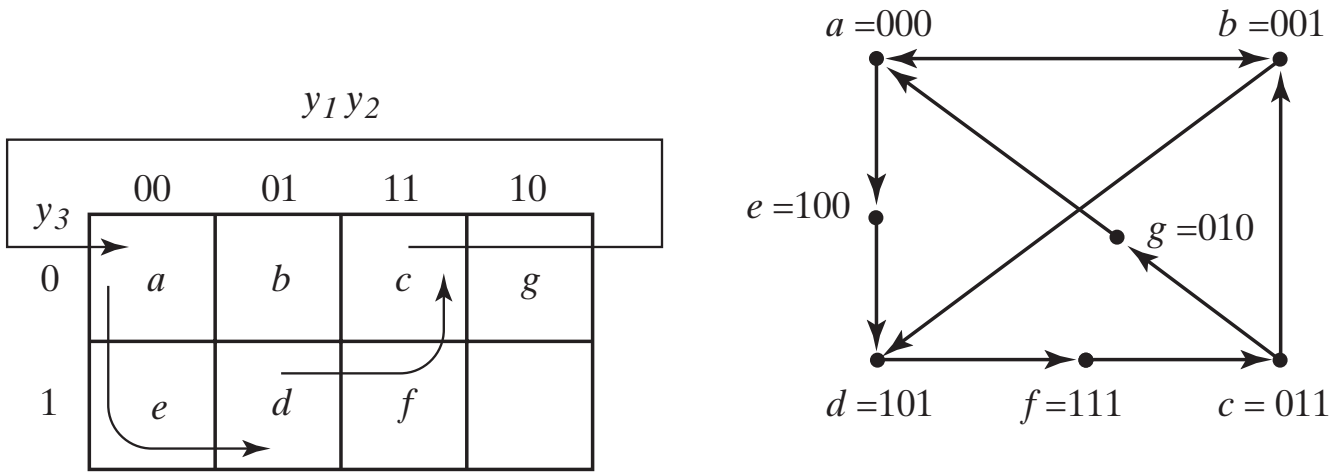
Fig. 9-28 Transition Table



(a) Flow table

(b) Transition diagram

Fig. 9-29 Four-Row Flow-Table Example



(a) Binary assignment

(b) Transition diagram

Fig. 9-30 Choosing Extra Rows for the Flow Table

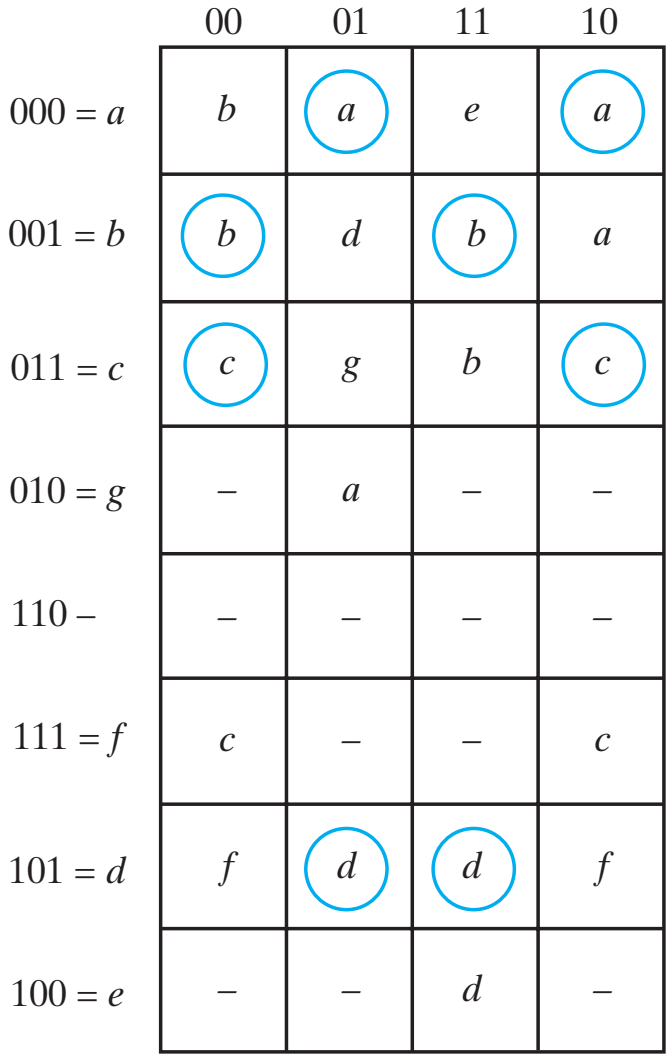


Fig. 9-31 State Assignment to Modified Flow Table

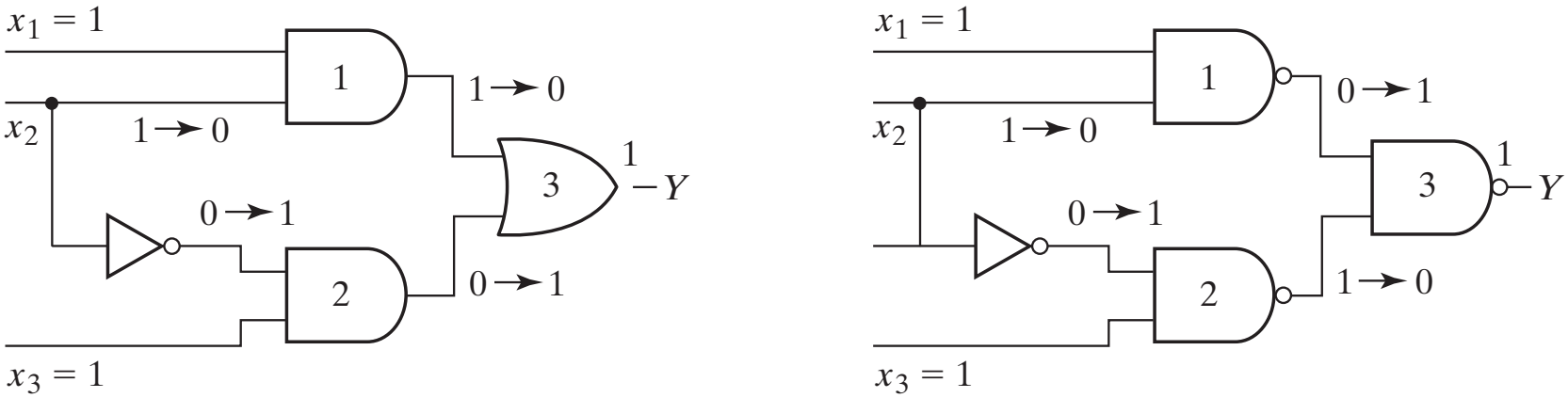
y_1	y_2y_3 = 00	01	11	10
0	a_1	b_1	c_1	d_1
1	c_2	d_2	a_2	b_2

(a) Binary assignment

	00	01	11	10
$000 = a_1$	b_1	(a_1)	d_1	(a_1)
$111 = a_2$	b_2	(a_2)	d_2	(a_2)
$001 = b_1$	(b_1)	d_2	(b_1)	a_1
$110 = b_2$	(b_2)	d_1	(b_2)	a_2
$011 = c_1$	(c_1)	a_2	b_1	(c_1)
$100 = c_2$	(c_2)	a_1	b_2	(c_2)
$010 = d_1$	c_1	(d_1)	(d_1)	c_1
$101 = d_2$	c_2	(d_2)	(d_2)	c_2

(b) Flow table

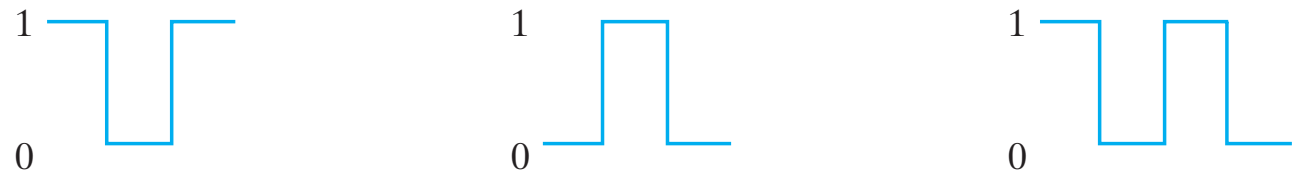
Fig. 9-32 Multiple-Row Assignment



(a) AND-OR circuit

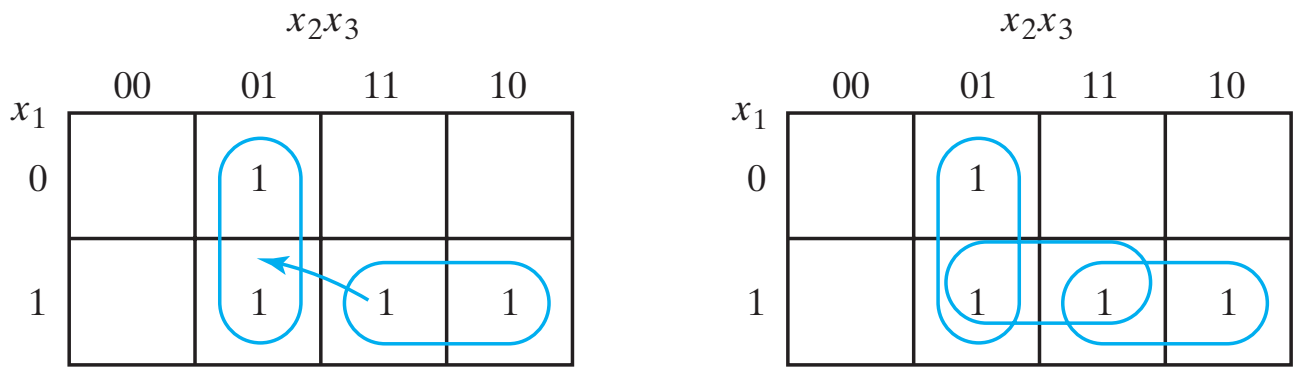
(b) NAND circuit

Fig. 9-33 Circuits with Hazards



(a) Static 1-hazard (b) Static 0-hazard (c) Dynamic hazard

Fig. 9-34 Types of Hazards



(a) $Y = x_1x_2 + x'_2x_3$ (b) $Y = x_1x_2 + x'_2x_3 + x_1x_3$

Fig. 9-35 Maps Demonstrating a Hazard and its Removal

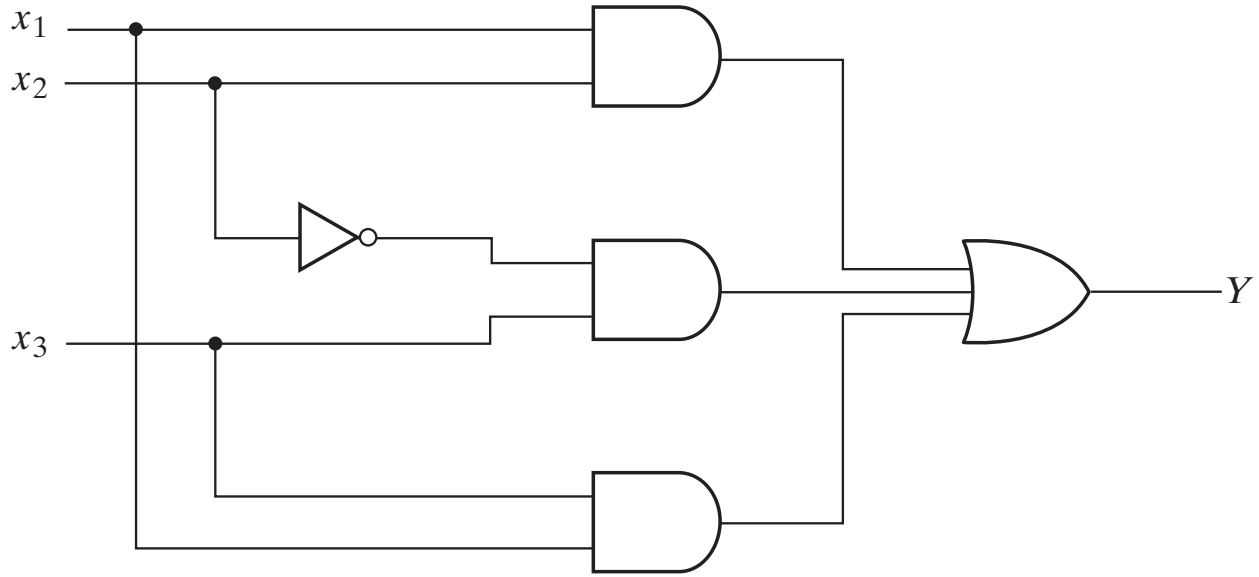
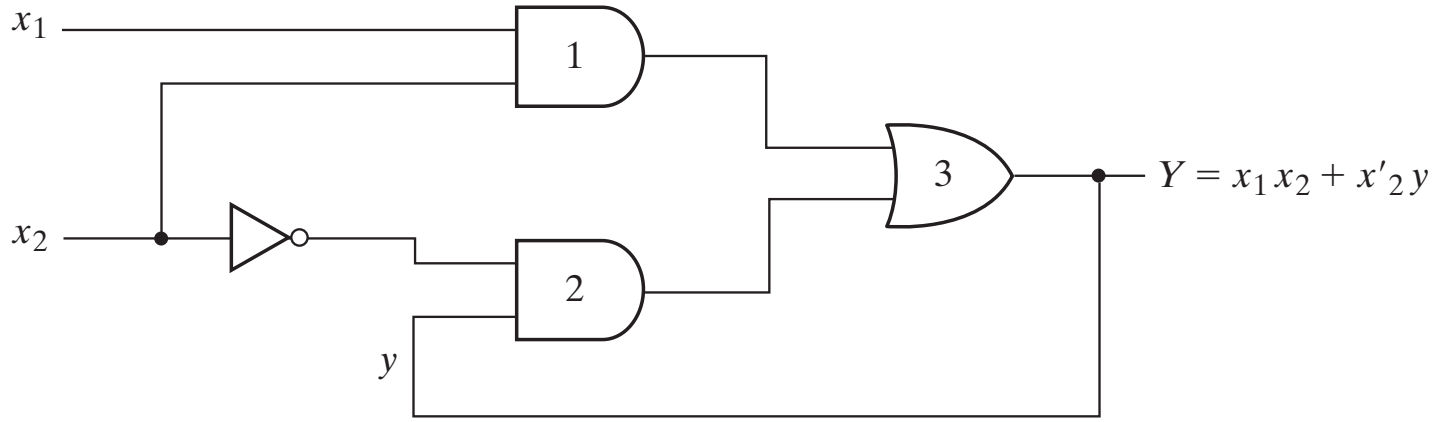


Fig. 9-36 Hazard-Free Circuit



(a) Logic diagram

y \ $x_1 x_2$	00	01	11	10
0	0	0	1	0
1	1	0	1	1

(b) Transition table

y \ $x_1 x_2$	00	01	11	10
0			1	
1	1		1	1

(c) Map for Y

Fig. 9-37 Hazard in an Asynchronous Sequential Circuit

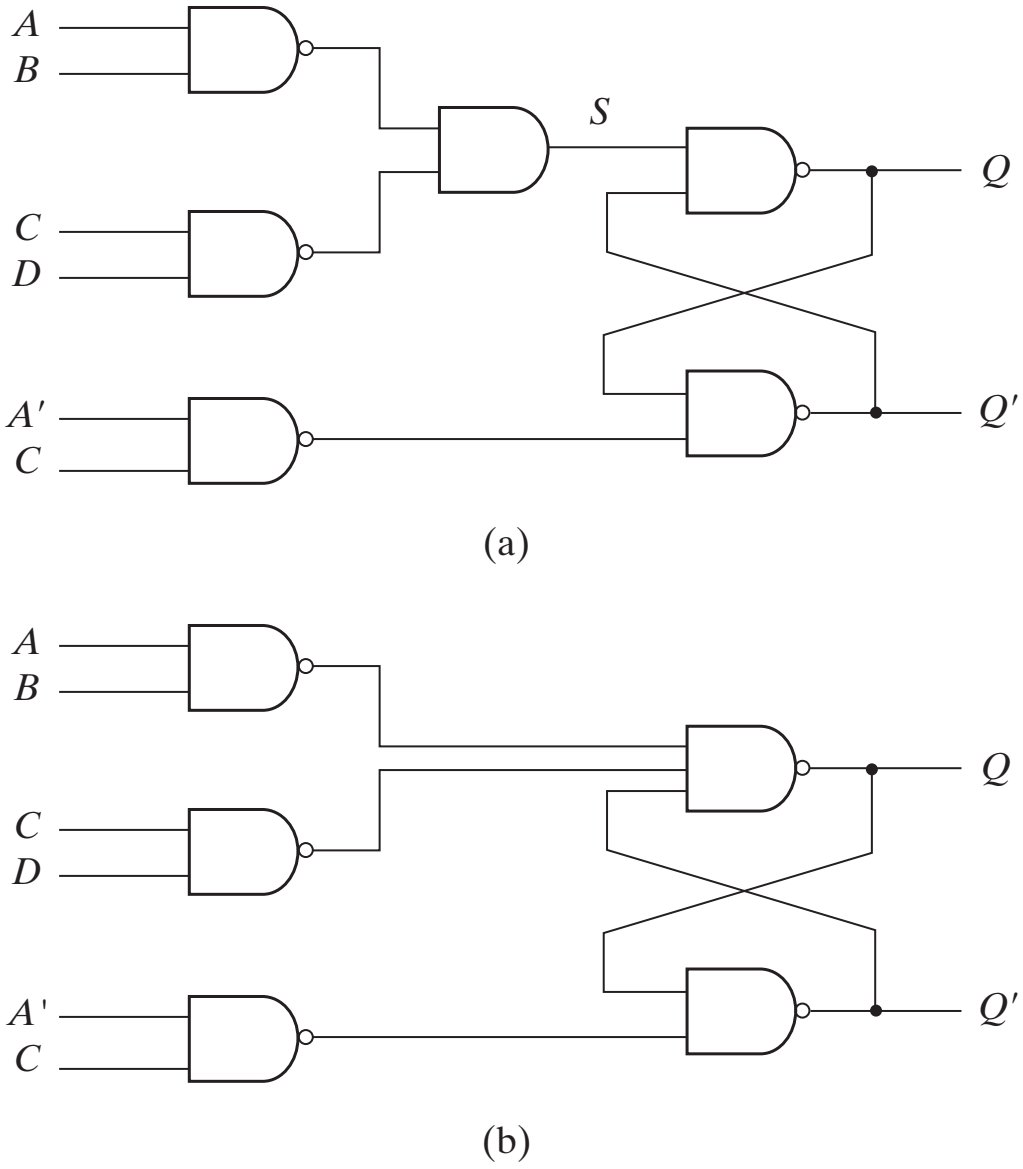


Fig. 9-38 Latch Implementation

	TC = 00	TC = 01	TC = 11	TC = 10
a	– , –	*f* , –	(*a*), 0	*b* , –
b	*g* , –	– , –	*c* , –	(*b*), 1
c	– , –	*h* , –	(*c*), 1	*d* , –
d	*e* , –	– , –	*a* , –	(*d*), 0
e	(*e*), 0	*f* , –	– , –	*d* , –
f	*e* , –	(*f*), 0	*a* , –	– , –
g	(*g*), 1	*h* , –	– , –	*b* , –
h	*g* , –	(*h*), 1	*c* , –	– , –

Fig. 9-39 Primitive Flow Table

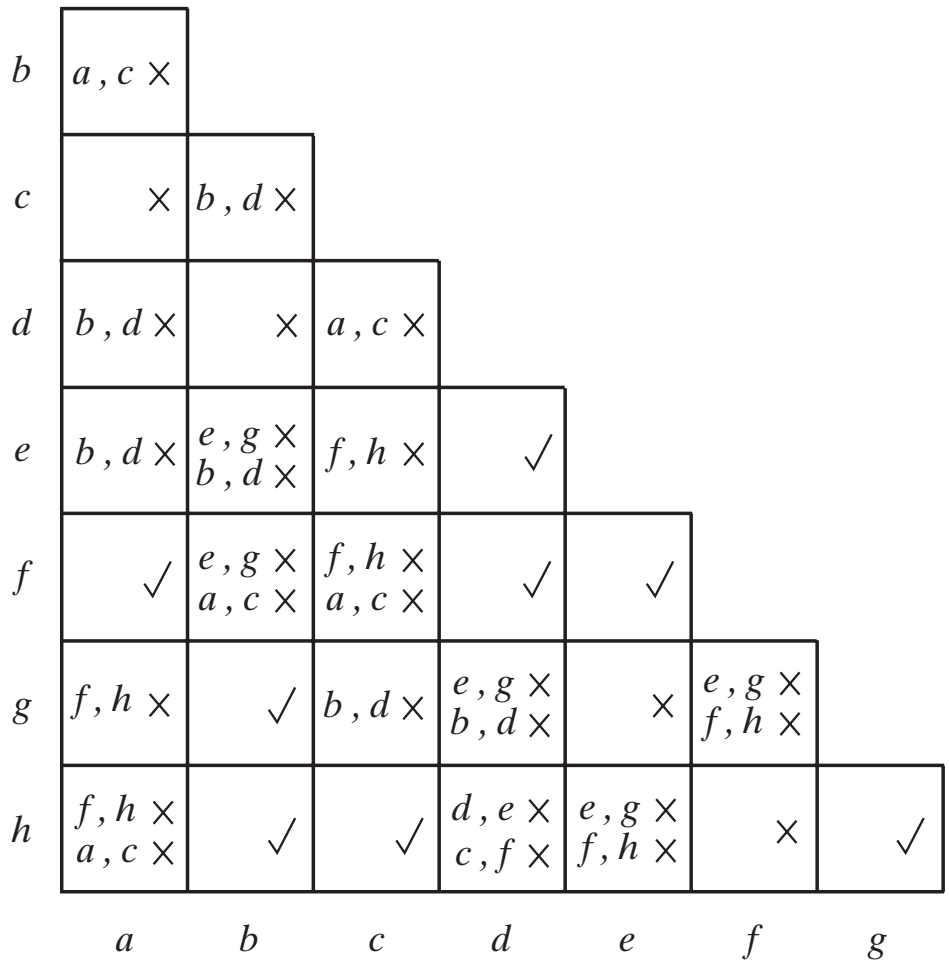


Fig. 9-40 Implication Table

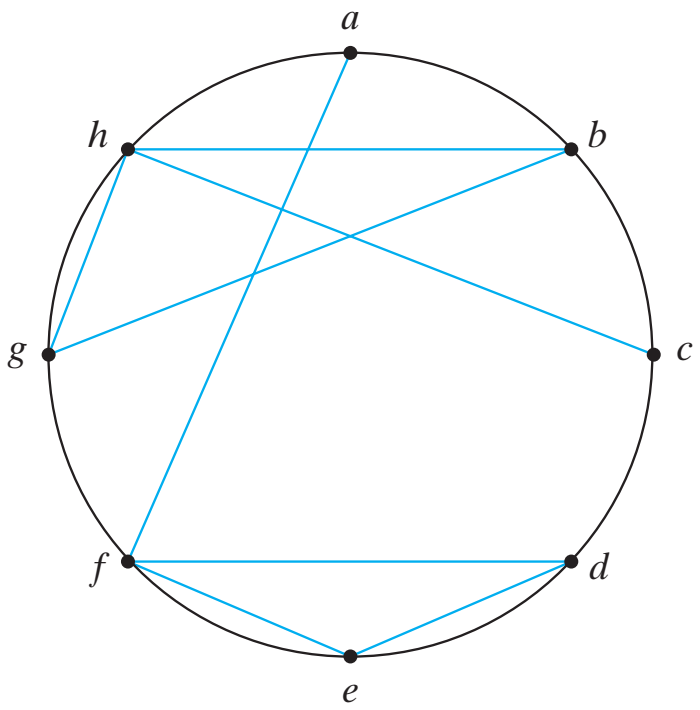
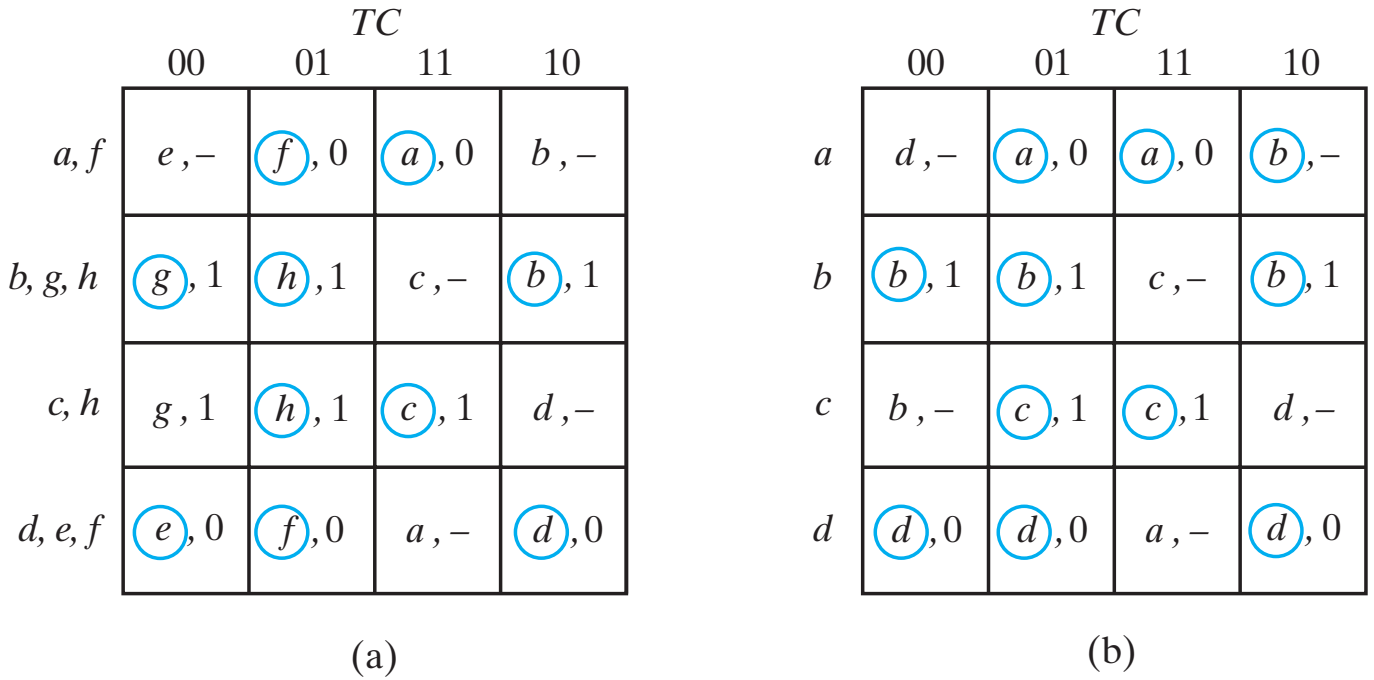


Fig. 9-41 Merger Diagram



	TC = 00	TC = 01	TC = 11	TC = 10
a, f	*e* , –	(*f*), 0	(*a*), 0	*b* , –
b, g, h	(*g*), 1	(*h*), 1	*c* , –	(*b*), 1
c, h	*g* , 1	(*h*), 1	(*c*), 1	*d* , –
d, e, f	(*e*), 0	(*f*), 0	*a* , –	(*d*), 0

(a)

	TC = 00	TC = 01	TC = 11	TC = 10
a	*d* , –	(*a*), 0	(*a*), 0	(*b*), –
b	(*b*), 1	(*b*), 1	*c* , –	(*b*), 1
c	*b* , –	(*c*), 1	(*c*), 1	*d* , –
d	(*d*), 0	(*d*), 0	*a* , –	(*d*), 0

(b)

Fig. 9-42 Reduced Flow Table

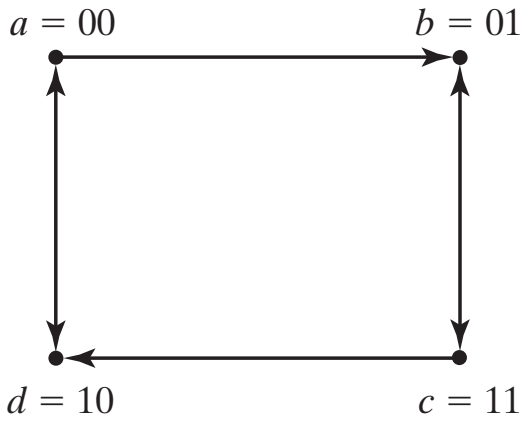
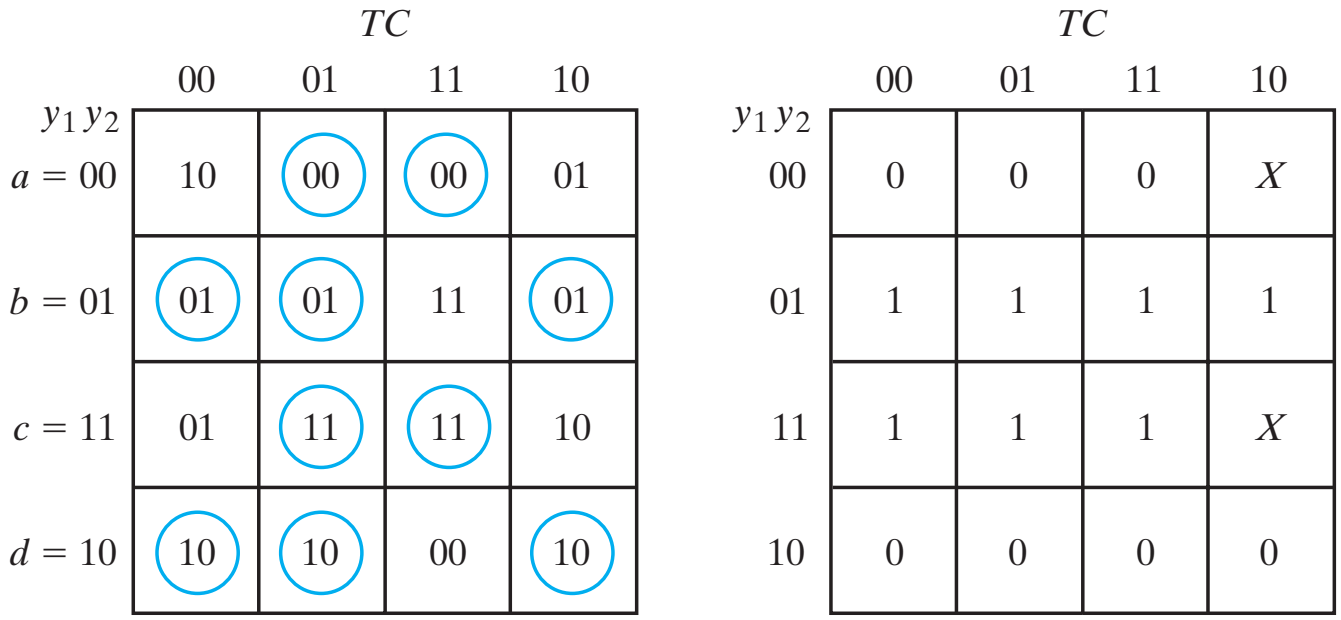


Fig. 9-43 Transition Diagram



(a) Transition table

(b) Output map $Q = y_2$

Fig. 9-44 Transition Table and Output Map

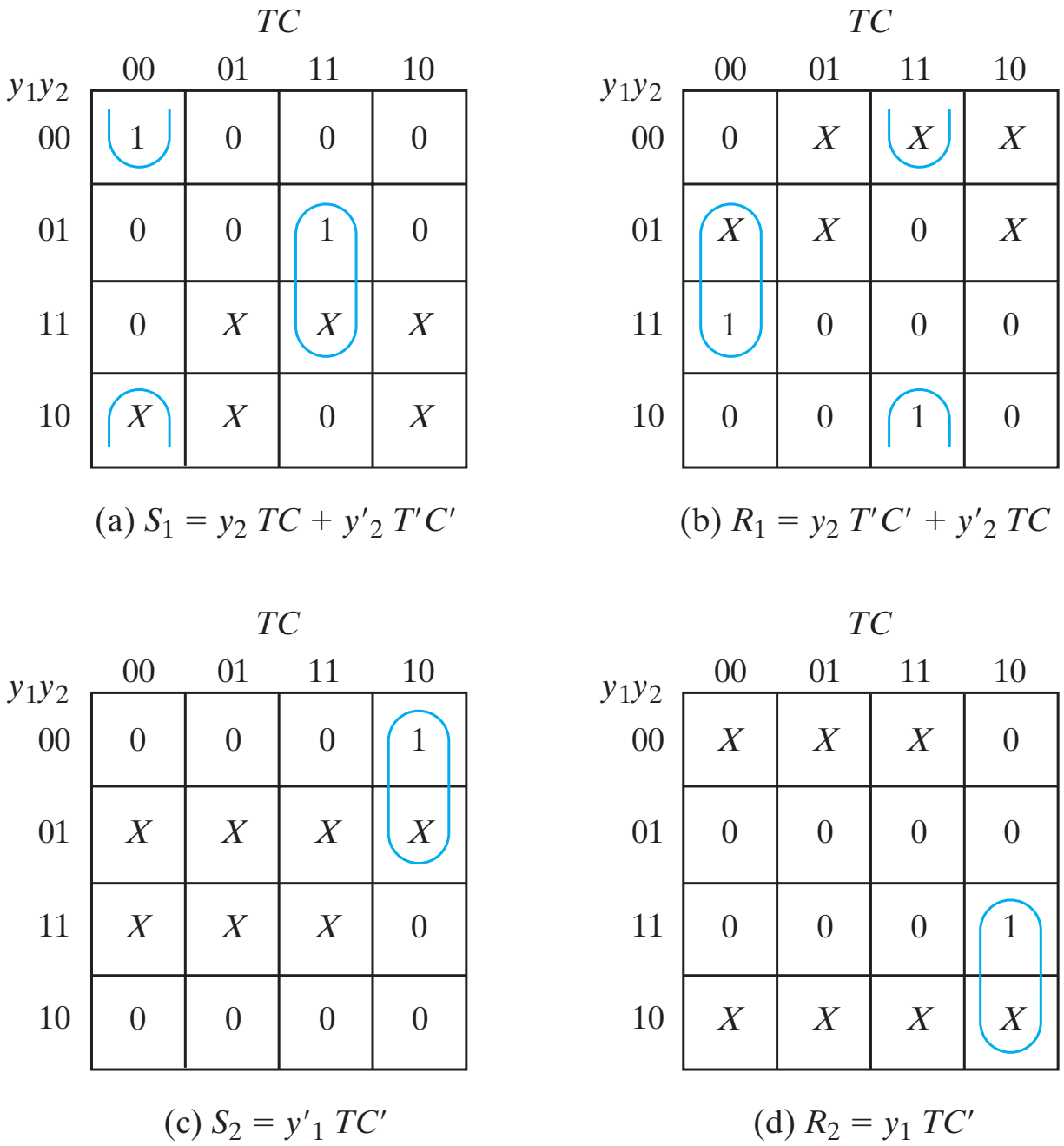


Fig. 9-45 Maps for Latch Inputs

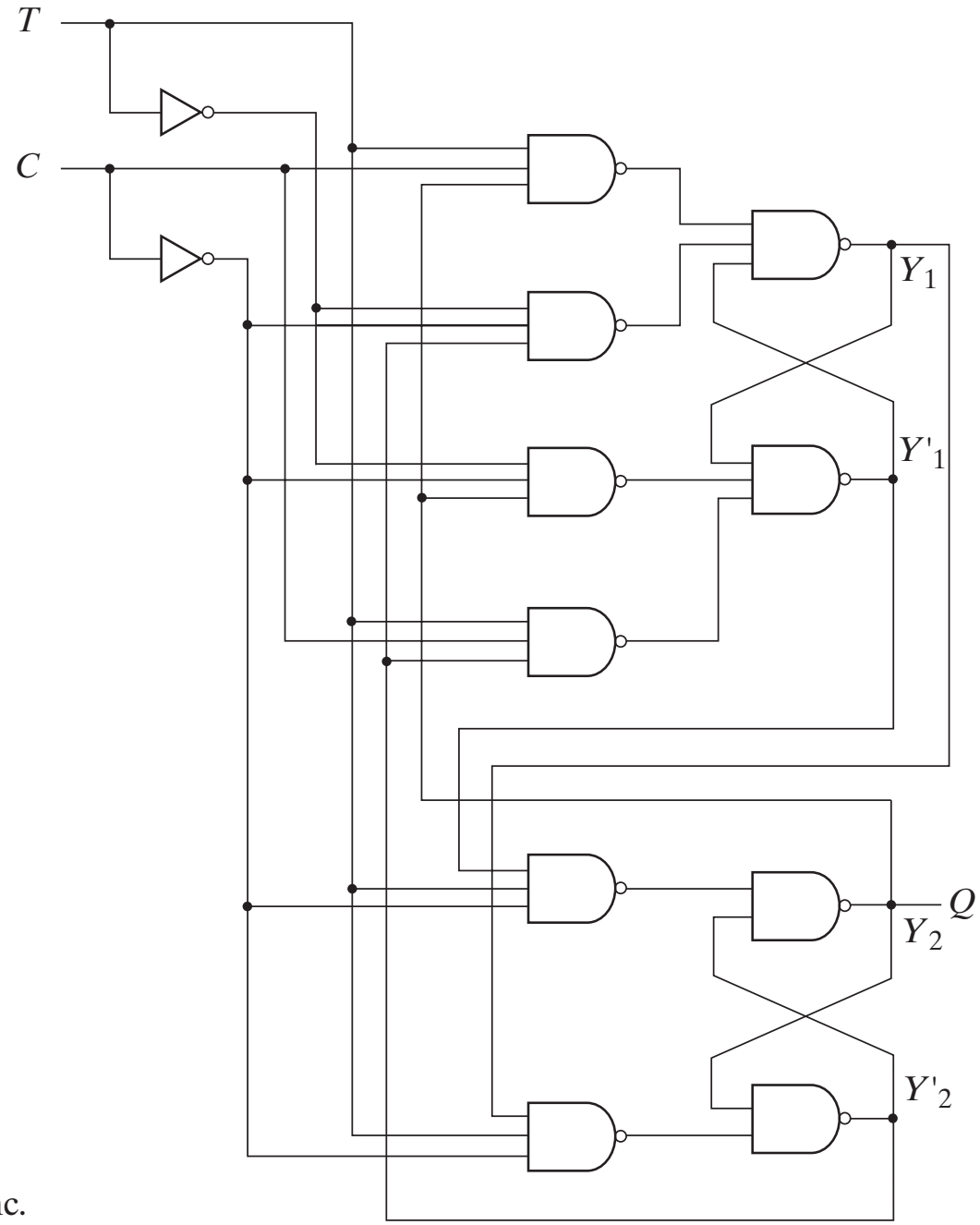


Fig. 9-46 Logic Diagram of Negative-Edge-Triggered *T* Flip-Flop

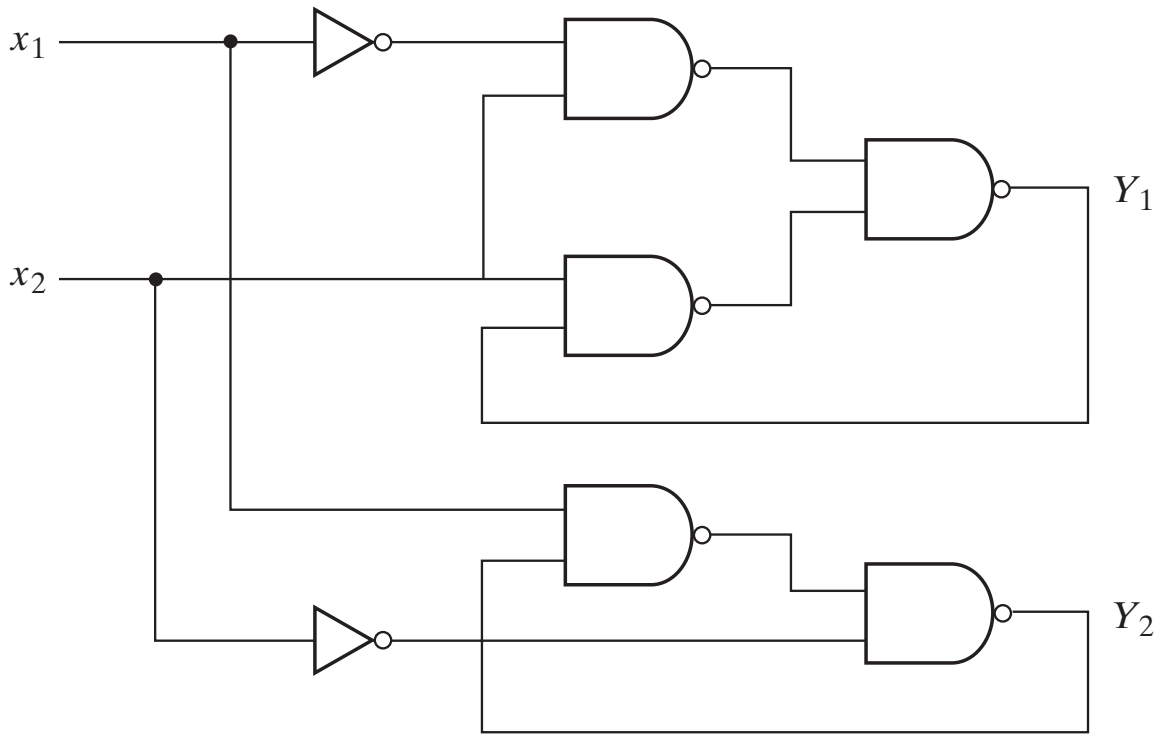


Fig. P9-2

	x_1x_2 = 00	01	11	10
a	(*a*), 0	*b* , –	*c* , –	(*a*), 1
b	*a* , –	(*b*), 0	(*b*), 0	*c* , –
c	*a* , –	*b* , –	(*c*), 1	(*c*), 0

Fig. P9-5

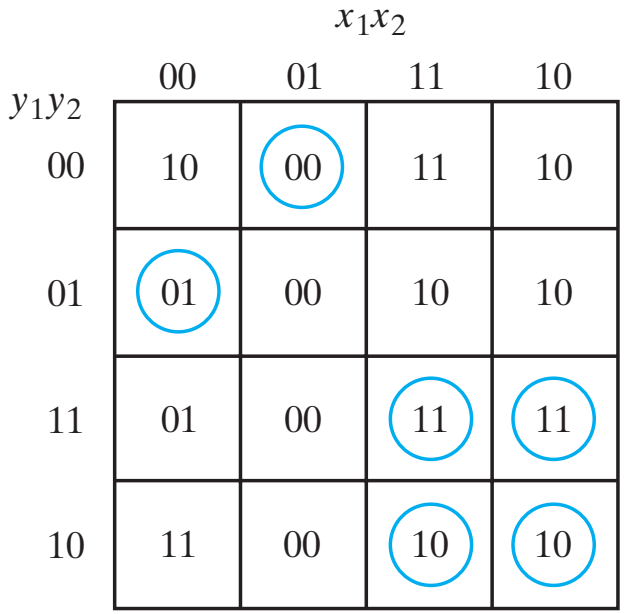


Fig. P9-6

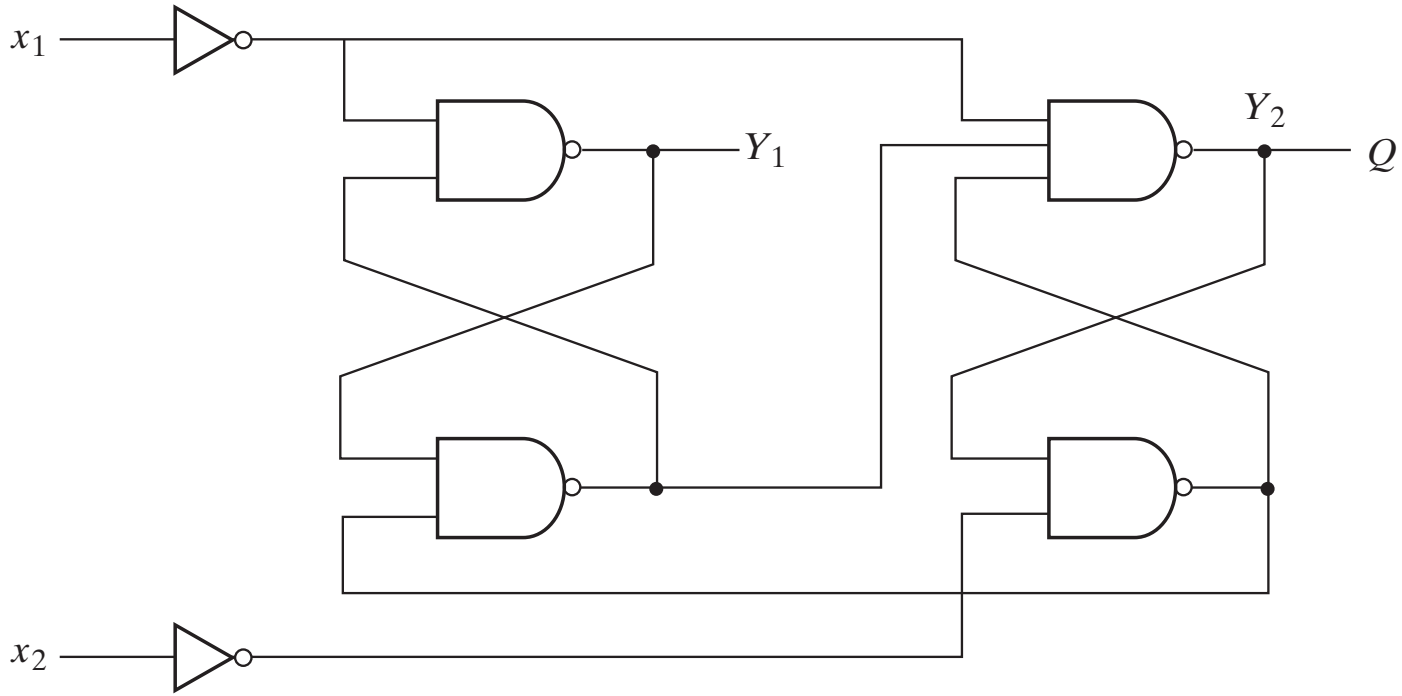


Fig. P9-9

	00	01	11	10
a	(a), 0	(a), 1	b , –	(a), 1
b	a , –	(b), 0	(b), 0	(b), 0

Fig. P9-14

	00	01	11	10
a	(*a*), 0	*b* , –	– , –	*d* , –
b	*a* , –	(*b*), 1	(*b*), 1	*c* , –
c	*b* , –	– , –	*b* , –	(*c*), 0
d	*c* , –	(*d*), 1	*c* , –	(*d*), 1

(a)

	00	01	11	10
a	(*a*), 0	*b* , –	*b* , –	(*a*), 0
b	*a* , –	(*b*), 0	(*b*), 1	*c* , –
c	*b* , –	*d* , –	(*c*), 1	(*c*), 1
d	(*d*), 0	(*d*), 1	*c* , –	*a* , –

(b)

Fig. P9-15

	00	01	11	10
a	(*a*), 0	*b* , –	– , –	*e* , –
b	*a* , –	(*b*), 0	*c* , –	– , –
c	– , –	*d* , –	(*c*), 0	*h* , –
d	*a* , –	(*d*), 1	– , –	– , –
e	*a* , –	– , –	*f* , –	(*e*), 0
f	– , –	*g* , –	(*f*), 0	*h* , –
g	*a* , –	(*g*), 0	– , –	– , –
h	*a* , –	– , –	– , –	(*h*), 0

(a)

	00	01	11	10
a	(*a*), 1	*f* , –	– , –	*e* , –
b	*c* , –	– , –	*j* , –	(*b*), 0
c	(*c*), 0	*d* , –	– , –	*b* , –
d	*c* , –	(*d*), 0	*g* , –	– , –
e	*a* , –	– , –	*g* , –	(*e*), 1
f	*a* , –	(*f*), 1	*g* , –	– , –
g	– , –	*d* , –	(*g*), 0	*k* , –
h	(*h*), 0	*d* , –	– , –	*k* , –
j	– , –	*f* , –	(*j*), 1	*b* , –
k	*a* , –	– , –	*j* , 1	(*k*), 0

(b)

Fig. P9-18

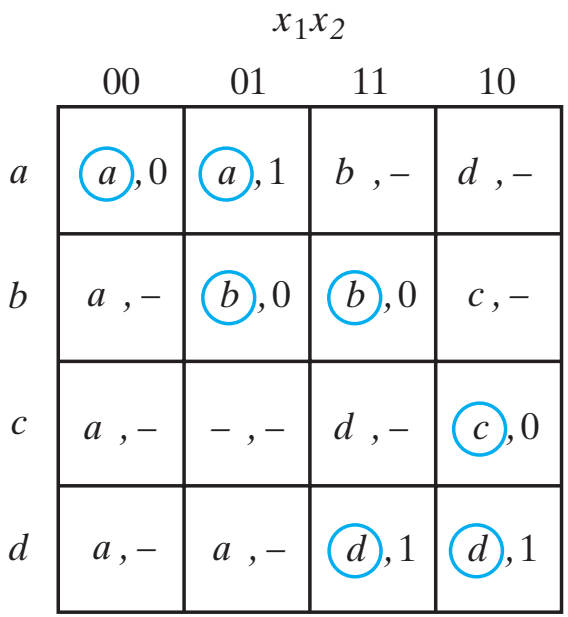


Fig. P9-19

	00	01	11	10
a	(*a*)	*d*	(*a*)	*c*
b	*a*	(*b*)	(*b*)	*d*
c	*d*	(*c*)	*b*	(*c*)
d	(*d*)	(*d*)	*e*	(*d*)
e	*f*	*c*	(*e*)	*c*
f	(*f*)	*b*	*a*	(*f*)

Fig. P9-20

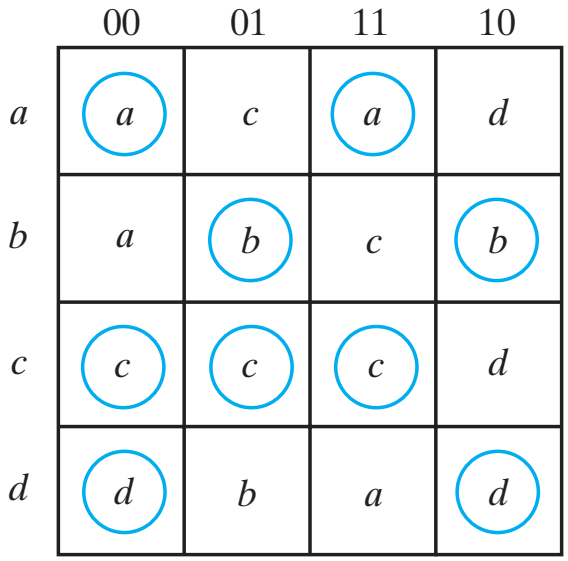


Fig. P9-21