Digital Design
Lecture 9

Sequential Logic

A General Sequential Circuit

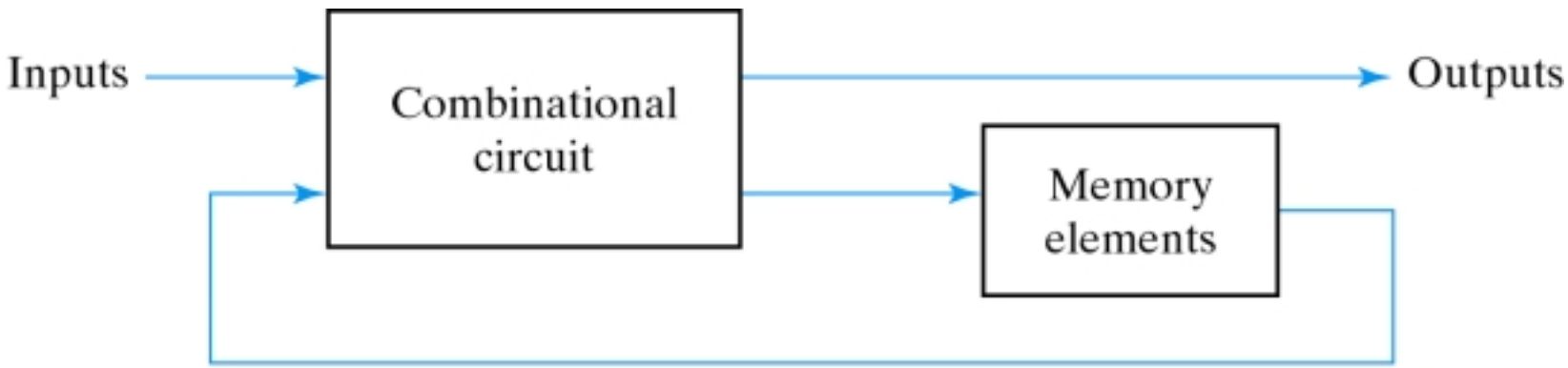
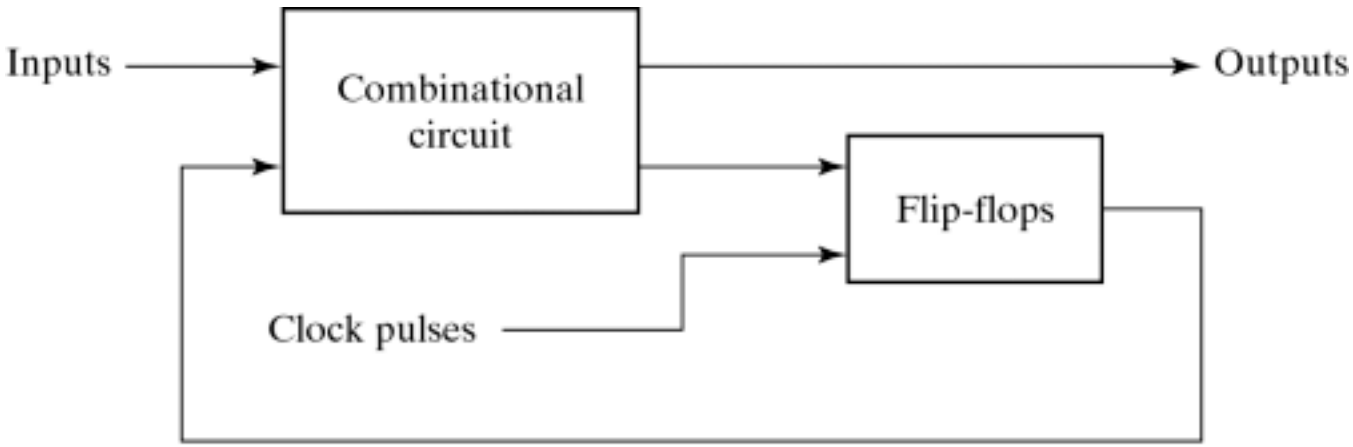


Fig. 5-1 Block Diagram of Sequential Circuit

Synchronous Sequential Circuits

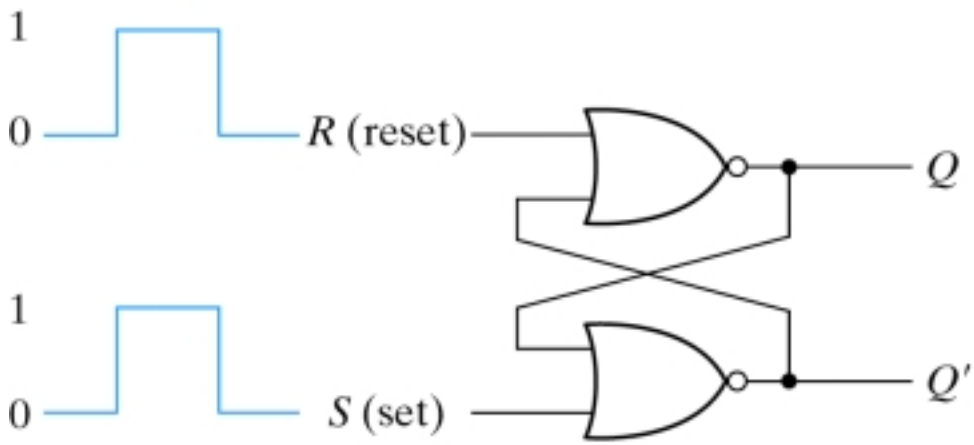


(a) Block diagram

(b) Timing diagram of clock pulses

Fig. 5-2 Synchronous Clocked Sequential Circuit

Set/Reset Latch (NORs)



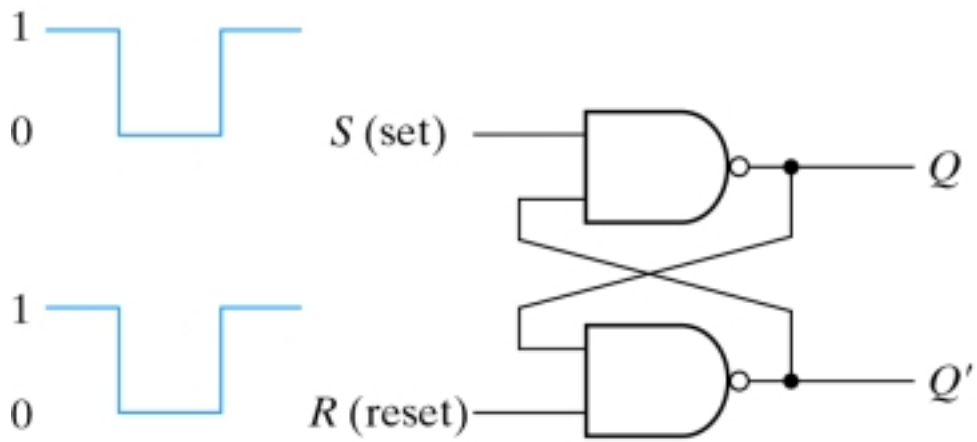
(a) Logic diagram

S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after $S = 1, R = 0$)
0	1	0	1	
0	0	0	1	(after $S = 0, R = 1$)
1	1	0	0	

(b) Function table

Fig. 5-3 *SR* Latch with NOR Gates

Set/Reset Latch (NANDs)

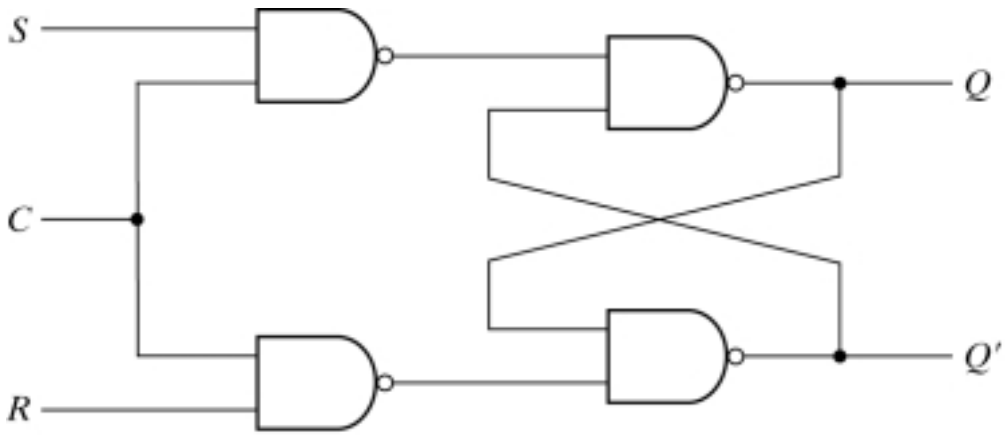


S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	

(a) Logic diagram (b) Function table

Fig. 5-4 *SR* Latch with NAND Gates

SR Latch with Control



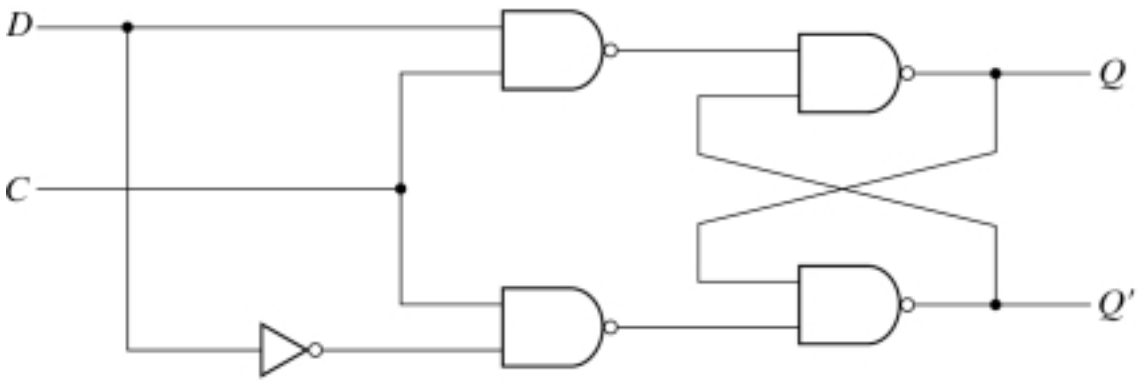
(a) Logic diagram

C	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$; Reset state
1	1	0	$Q = 1$; set state
1	1	1	Indeterminate

(b) Function table

Fig. 5-5 SR Latch with Control Input

D Latch



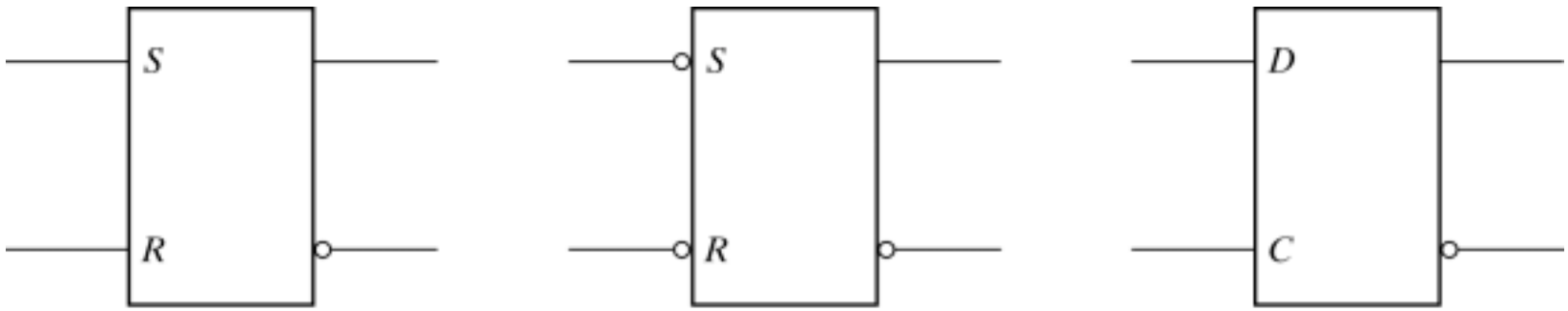
(a) Logic diagram

C	D	Next state of Q
0	X	No change
1	0	Q = 0; Reset state
1	1	Q = 1; Set state

(b) Function table

Fig. 5-6 D Latch

Latch Symbols



SR $\overline{S}\overline{R}$ D

Fig. 5-7 Graphic Symbols for Latches

Clock Response

(a) Response to positive level

(b) Positive-edge response

(c) Negative-edge response

Fig. 5-8 Clock Response in Latch and Flip-Flop

Master-Slave D Flip-Flop

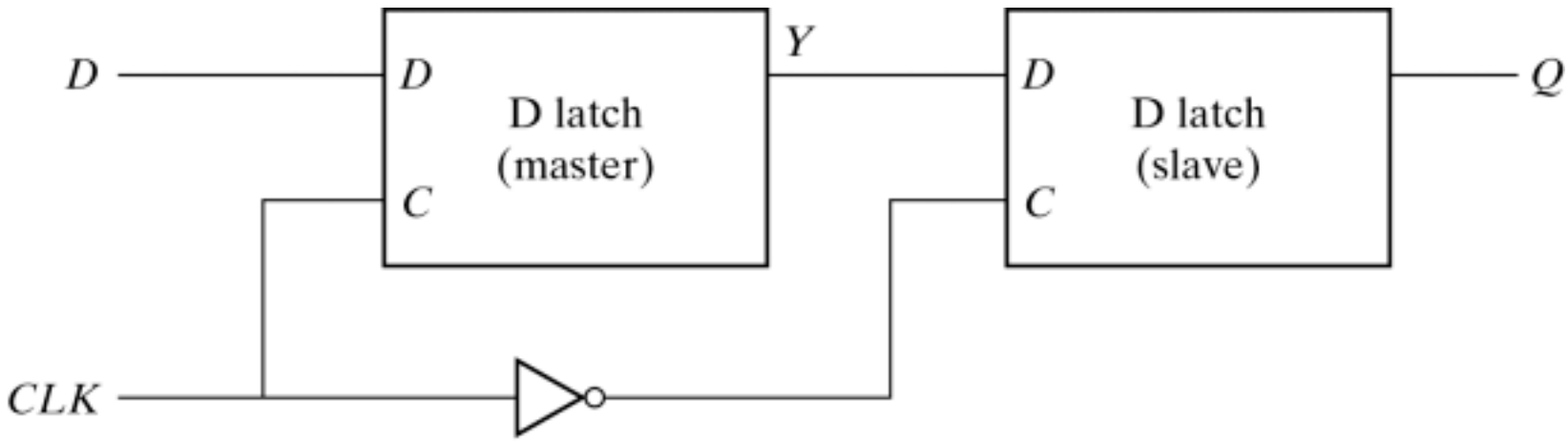


Fig. 5-9 Master-Slave *D* Flip-Flop

D-Type Positive-Edge Triggered Flip-Flop

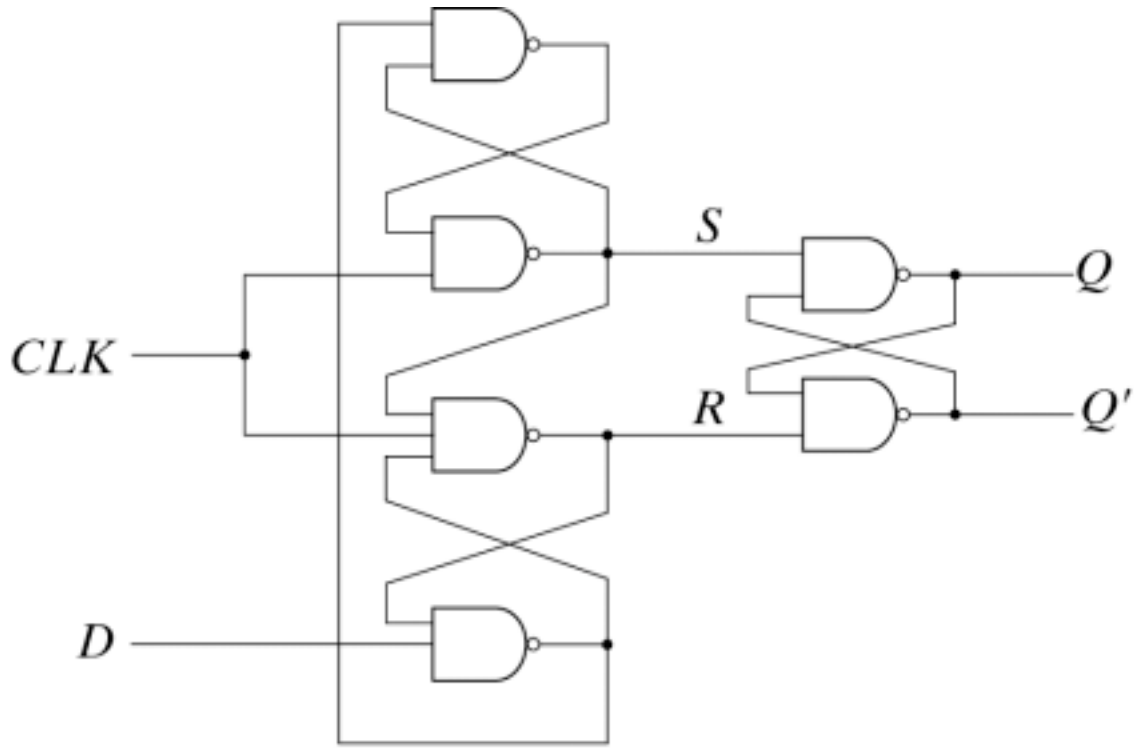
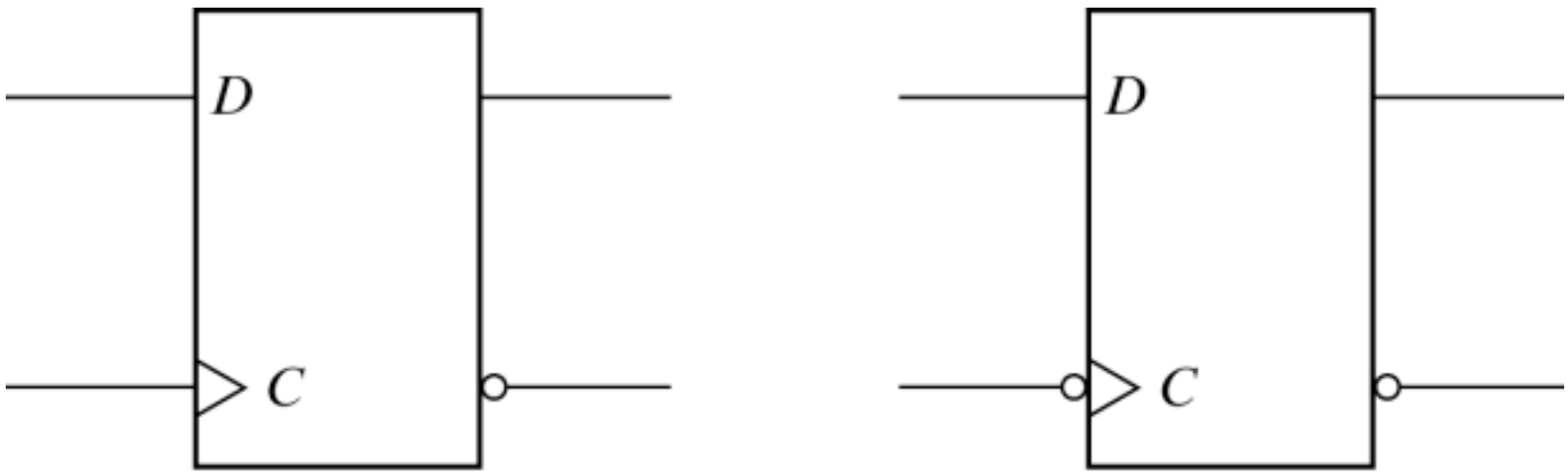


Fig. 5-10 *D*-Type Positive-Edge-Triggered Flip-Flop

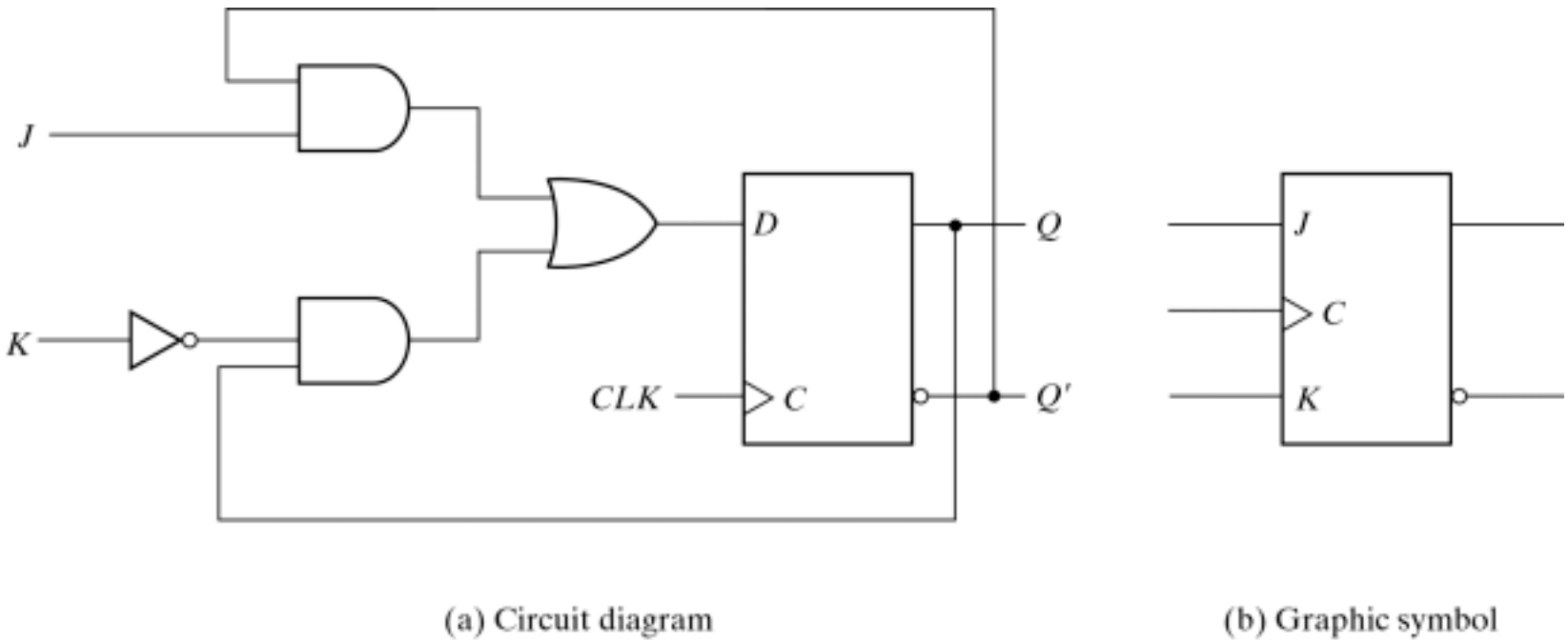
Edge-Triggered D Flip-Flop Graphic Symbol



(a) Positive-edge (a) Negative-edge

Fig. 5-11 Graphic Symbol for Edge-Triggered *D* Flip-Flop

JK Flip-Flop



(a) Circuit diagram

(b) Graphic symbol

Fig. 5-12 *JK* Flip-Flop

Flip-Flop Characteristic Tables

D – Flip-Flop

D	Q(t+1)
0	0 - Reset
1	1 - Set

T – Flip-Flop

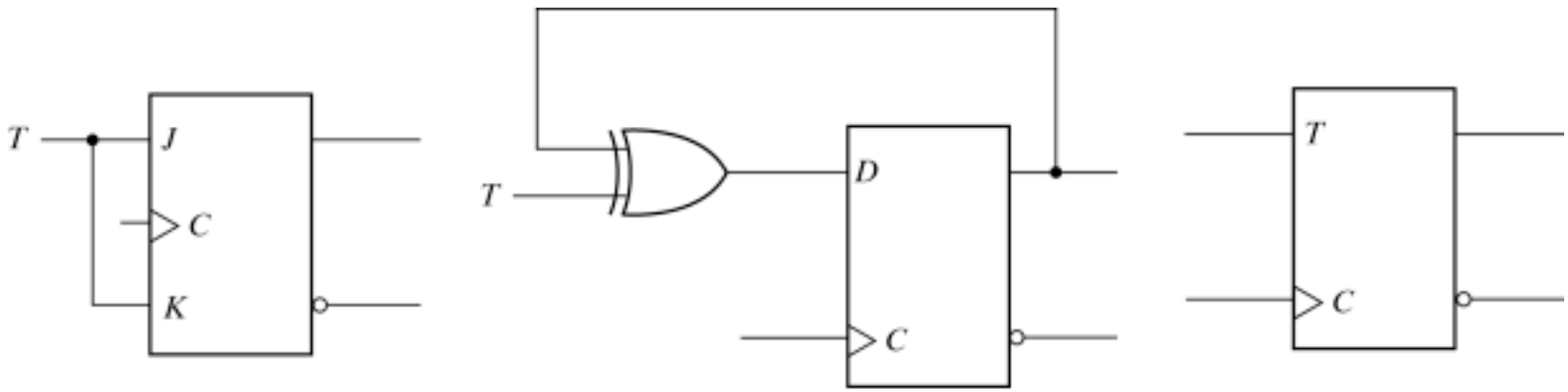
T	Q(t+1)
0	Q(t) – No change
1	Q′(t) - Complement

JK – Flip-Flop

J	K	Q(t+1)
0	0	Q(t) – No change
0	1	0 – Reset
1	0	1 – Set
1	1	Q′(t) – Complement

Table 5.1

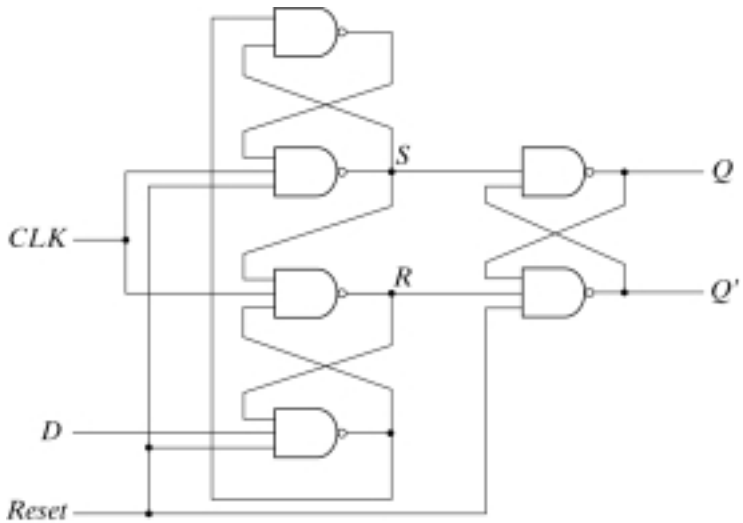
T Flip-Flop



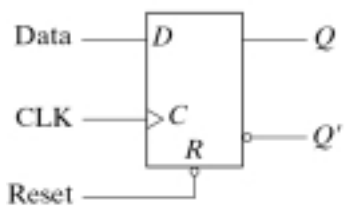
(a) From *JK* flip-flop (b) From *D* flip-flop (c) Graphic symbol

Fig. 5-13 T Flip-Flop

D Flip-Flop with Reset



(a) Circuit diagram



(b) Graphic symbol

R	C	D	Q	Q'
0	X	X	0	1
1	↑	0	0	1
1	↑	1	1	0

(b) Function table

Fig. 5-14 *D* Flip-Flop with Asynchronous Reset

Sequential Circuit Analysis

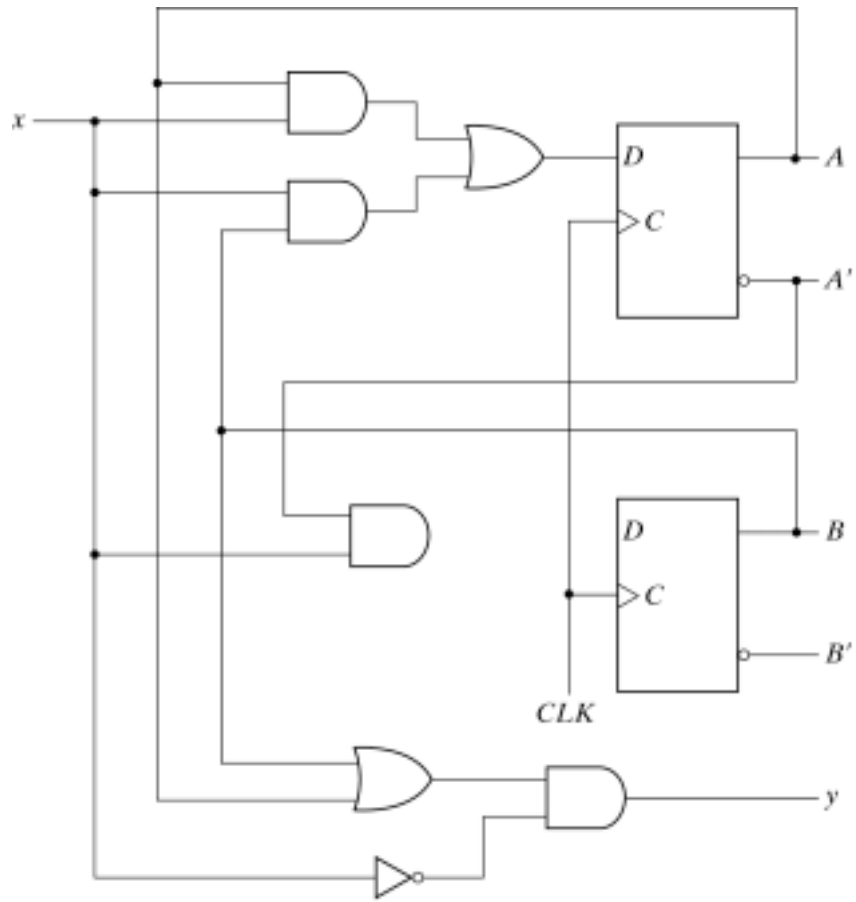


Fig. 5-15 Example of Sequential Circuit

State Diagrams

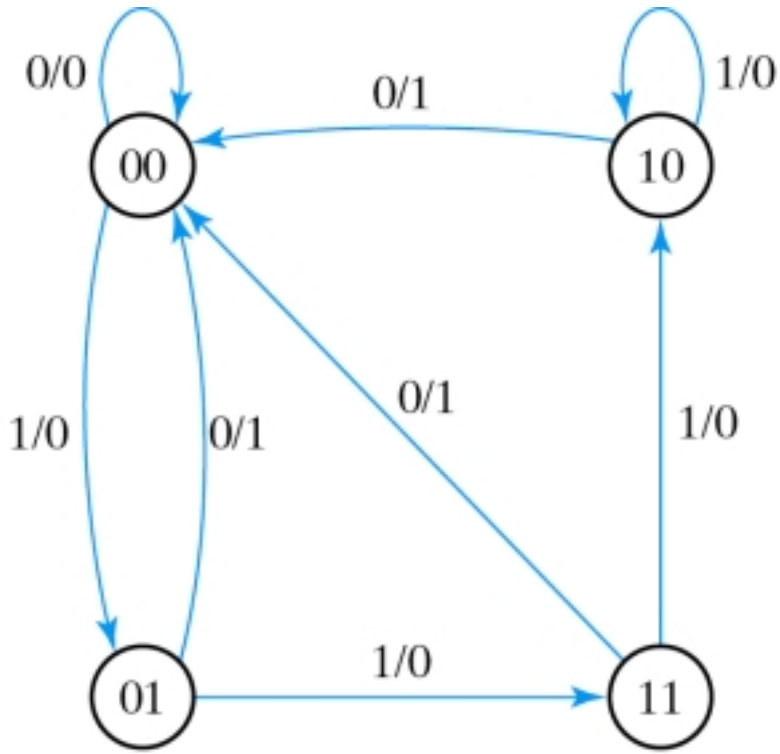
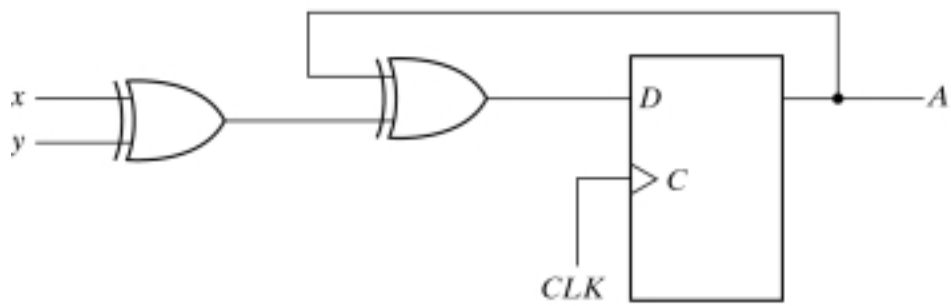


Fig. 5-16 State Diagram of the Circuit of Fig. 5-15

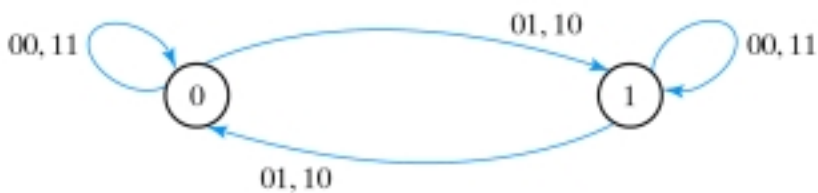
Sequential Circuit: D Flip-Flop



(a) Circuit diagram

Present state	Inputs		Next state
A	*x*	*y*	*A*
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

(b) State table



(c) State diagram

Fig. 5-17 Sequential Circuit with *D* Flip-Flop

Sequential Circuit: JK Flip-Flop

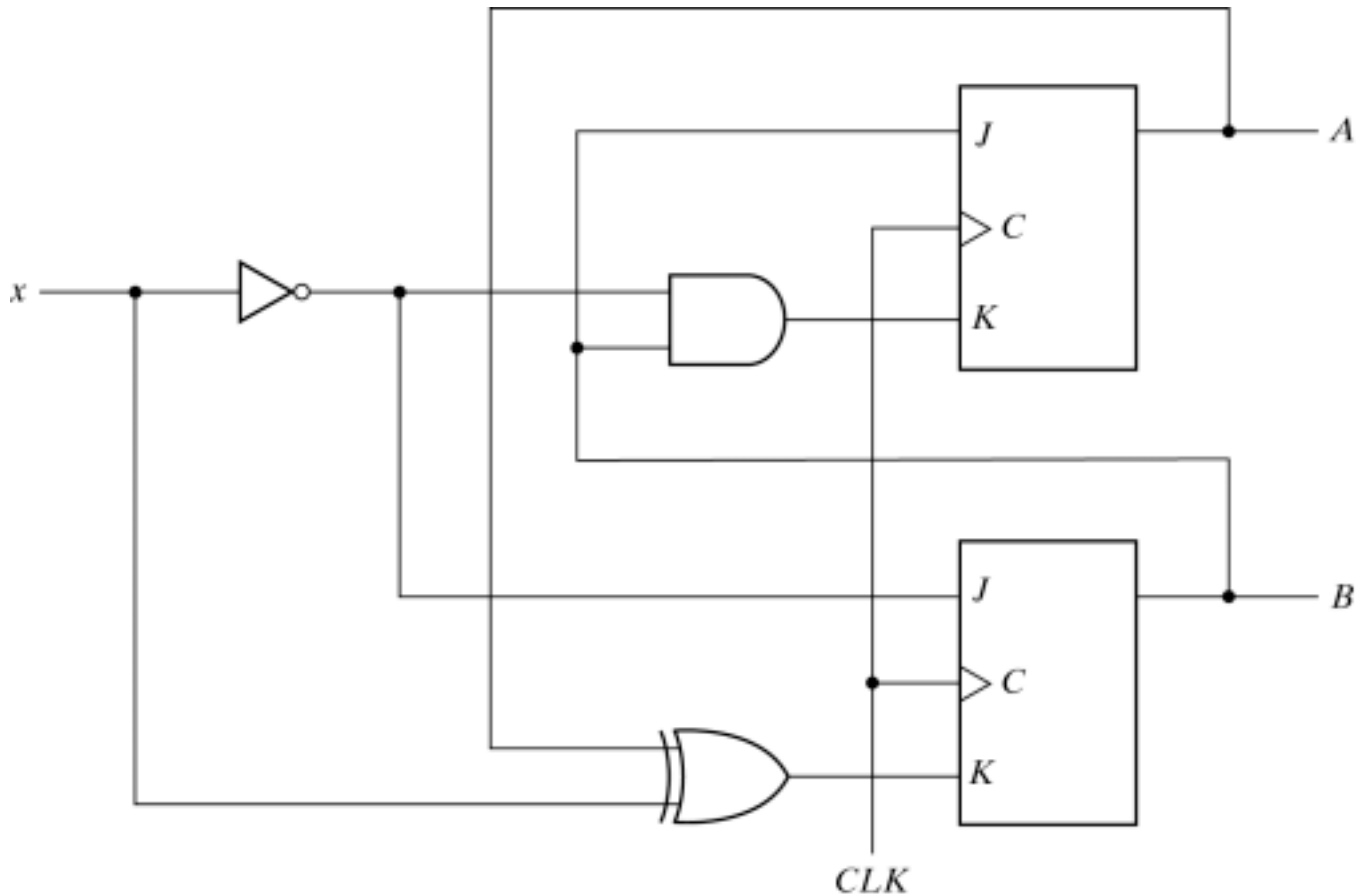


Fig. 5-18 Sequential Circuit with *JK* Flip-Flop

State Diagram for JK Circuit

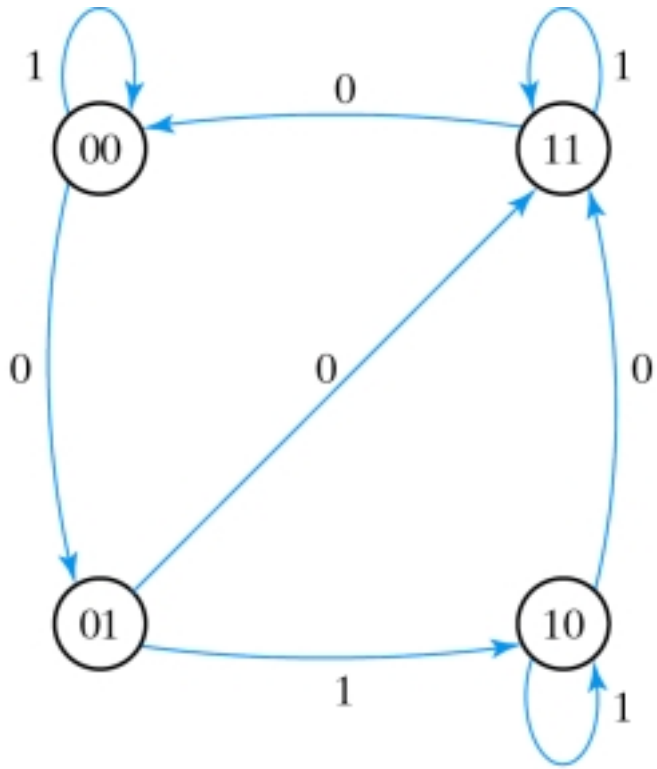
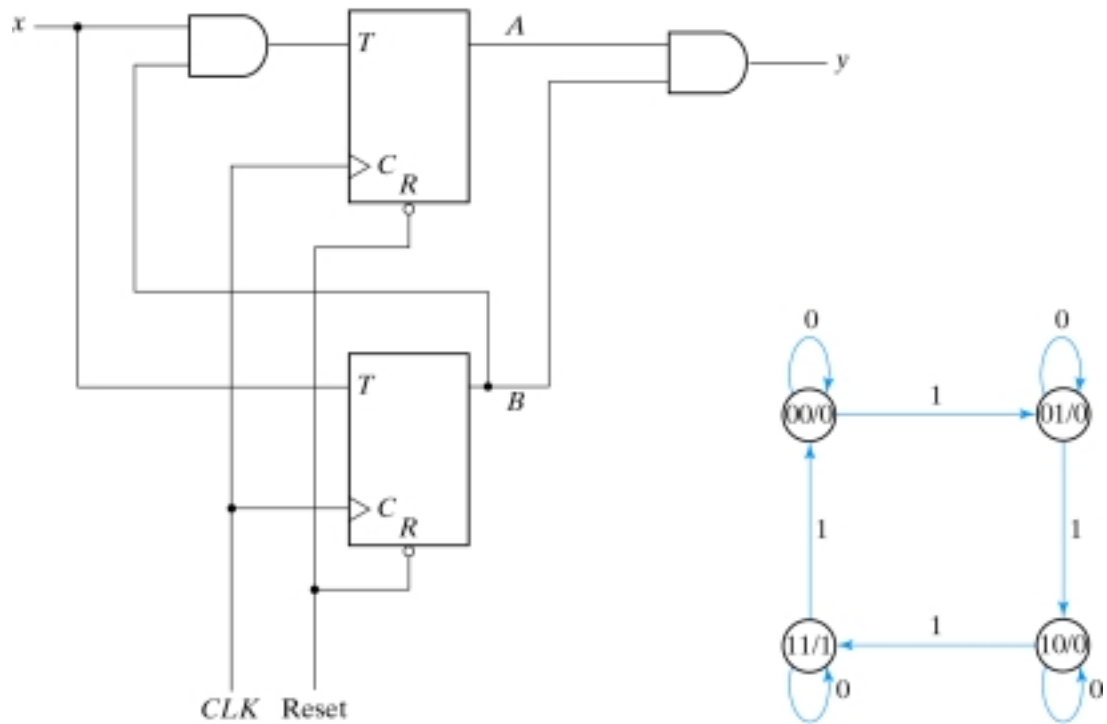


Fig. 5-19 State Diagram of the Circuit of Fig. 5-18

Sequential Circuit: T Flip-Flop



(a) Circuit diagram (b) State diagram

Fig. 5-20 Sequential Circuit with *T* Flip-Flops

Mealy and Moore Models Finite State Machines

- Mealy
  - Output is a function of both the present state and the present input
  - See Figure 5-15 (Slide 16: Sequential Analysis)
- Moore
  - Output is only a function of the current state
  - See Figure 5-18 (Slide 19: JK Flip-Flop)