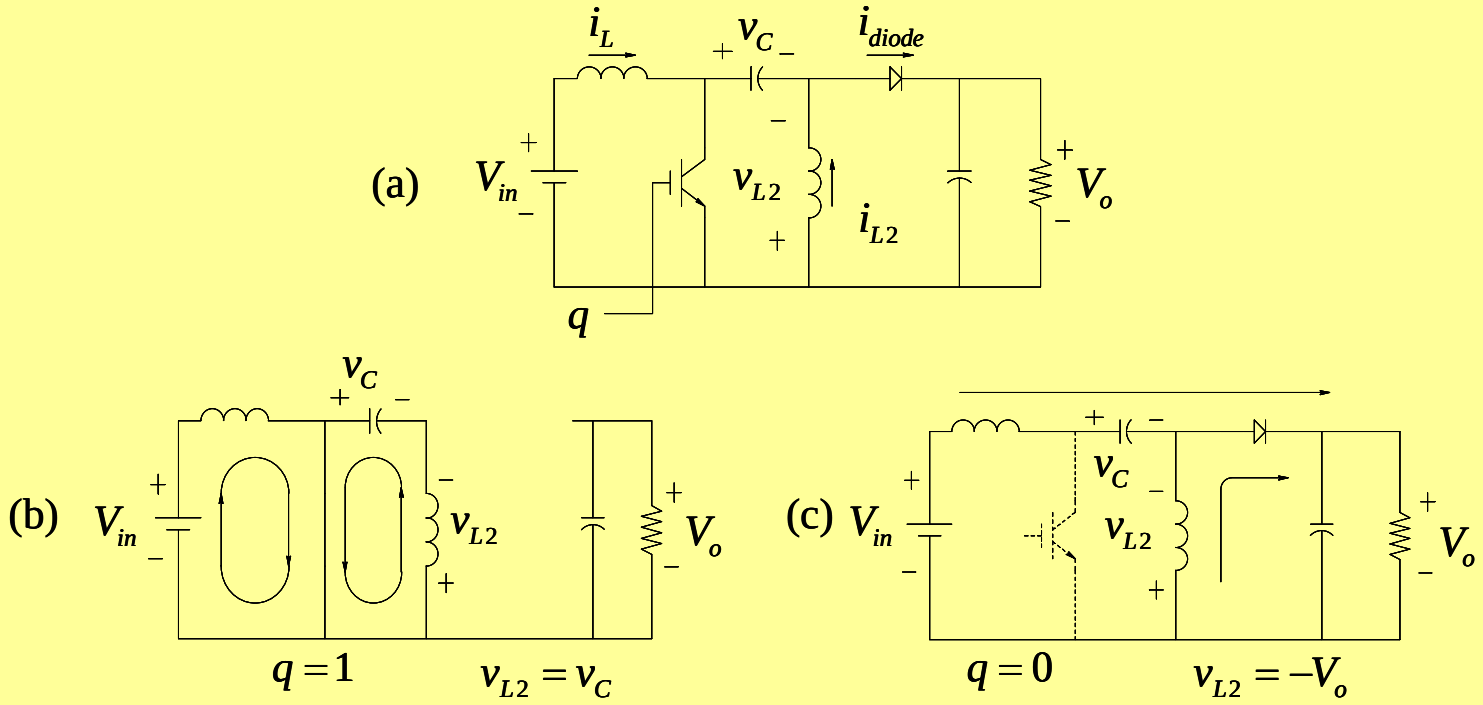
Other Considerations in DC-DC Converters

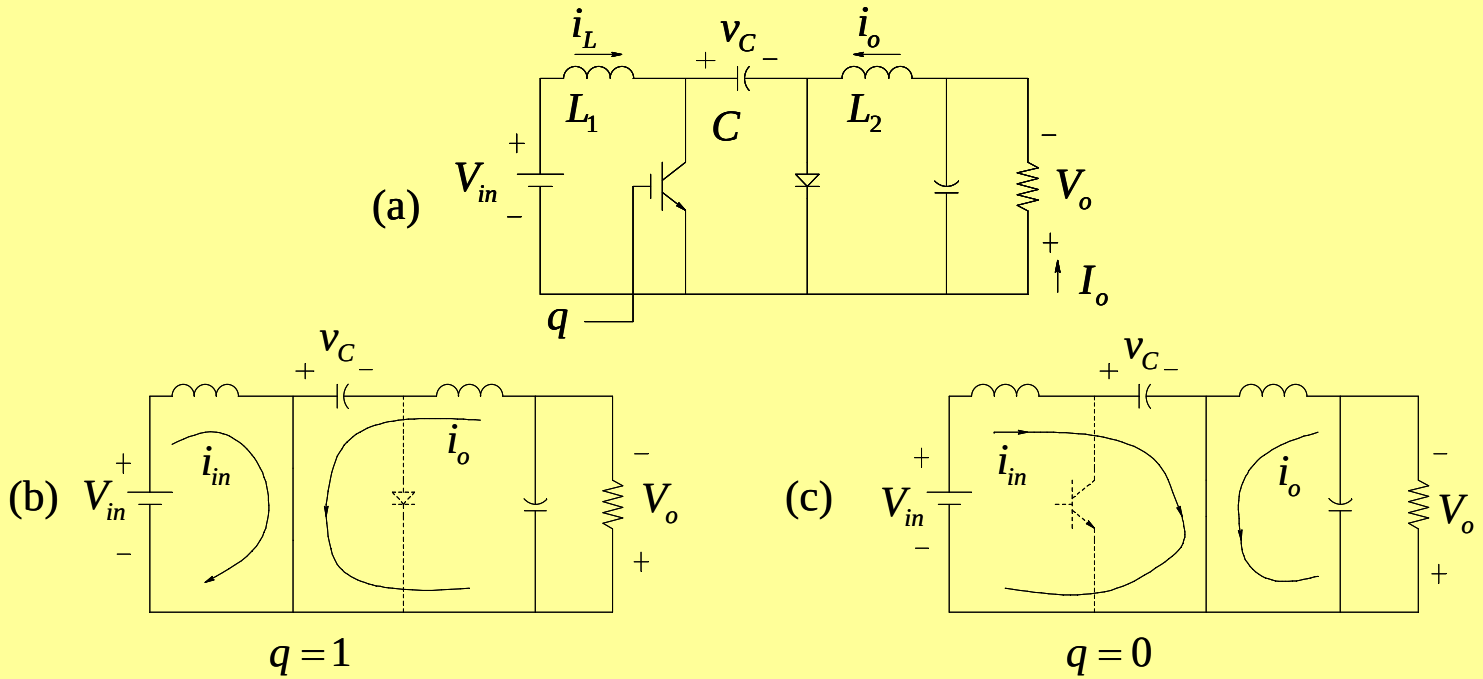
- Other DC-DC Converters
  - SEPIC and Cuk Converters
  - Synchronous-Rectified Buck Converters
  - Interleaving in Converters
- Topology Selection
- Worst-Case Design

SEPIC Converters (Single-Ended Primary Inductor Converters)



$$DV_{in} = (1-D)V_o \qquad \frac{V_o}{V_{in}} = \frac{D}{1-D}$$

Cuk Converter

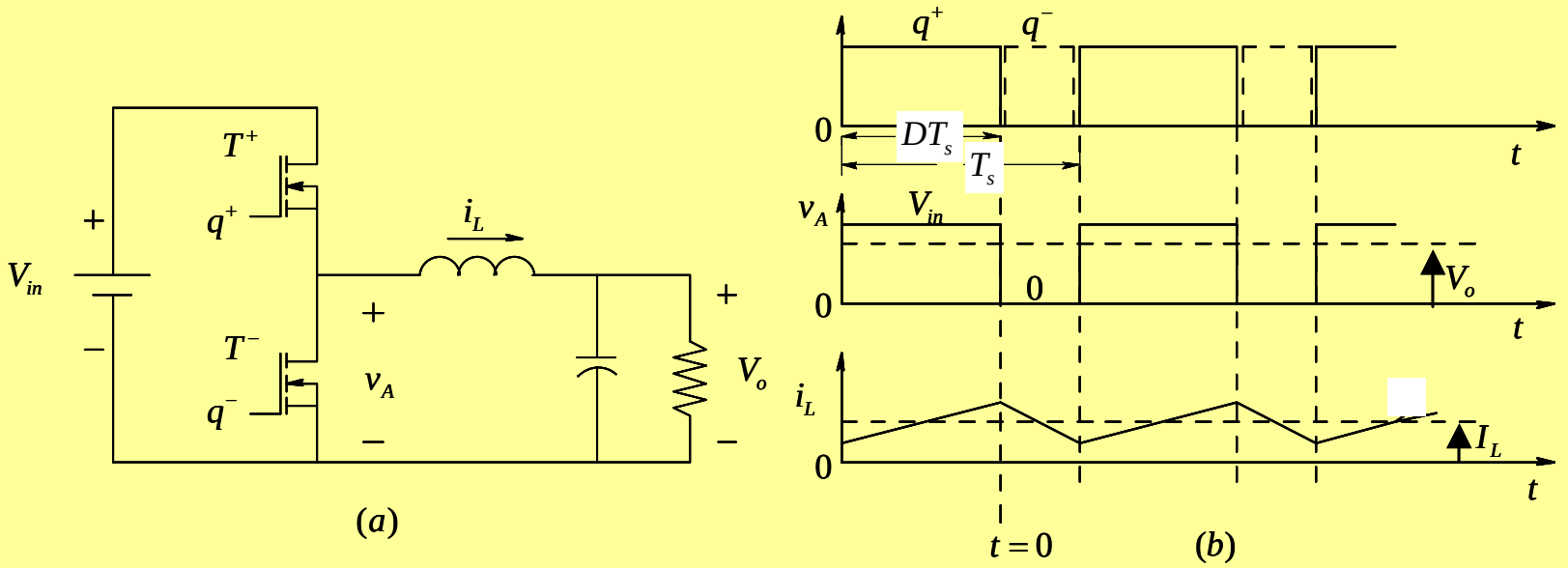


$$DI_o = (1-D)I_{in}$$

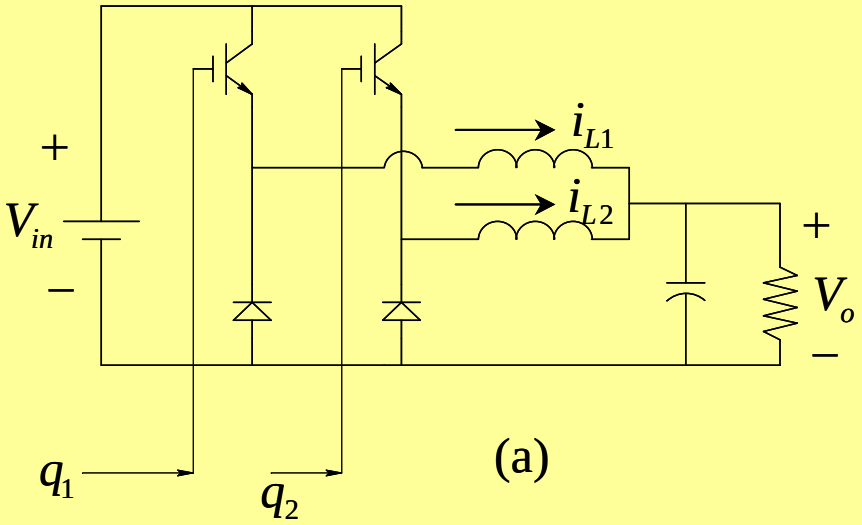
$$\frac{I_{in}}{I_o} = \frac{D}{1-D}$$

$$\frac{V_o}{V_{in}} = \frac{D}{1-D}$$

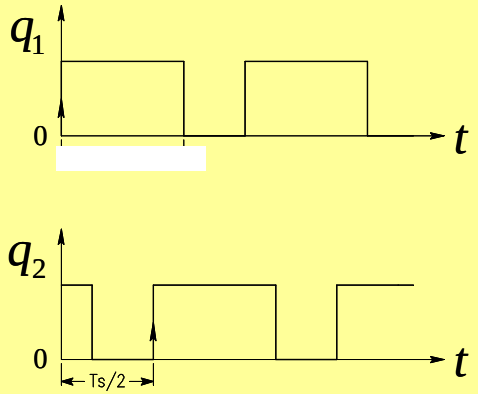
SYNCHRONOUS-RECTIFIED BUCK CONVERTER FOR VERY LOW OUTPUT VOLTAGES



INTERLEAVING OF CONVERTERS



(a)



(b)

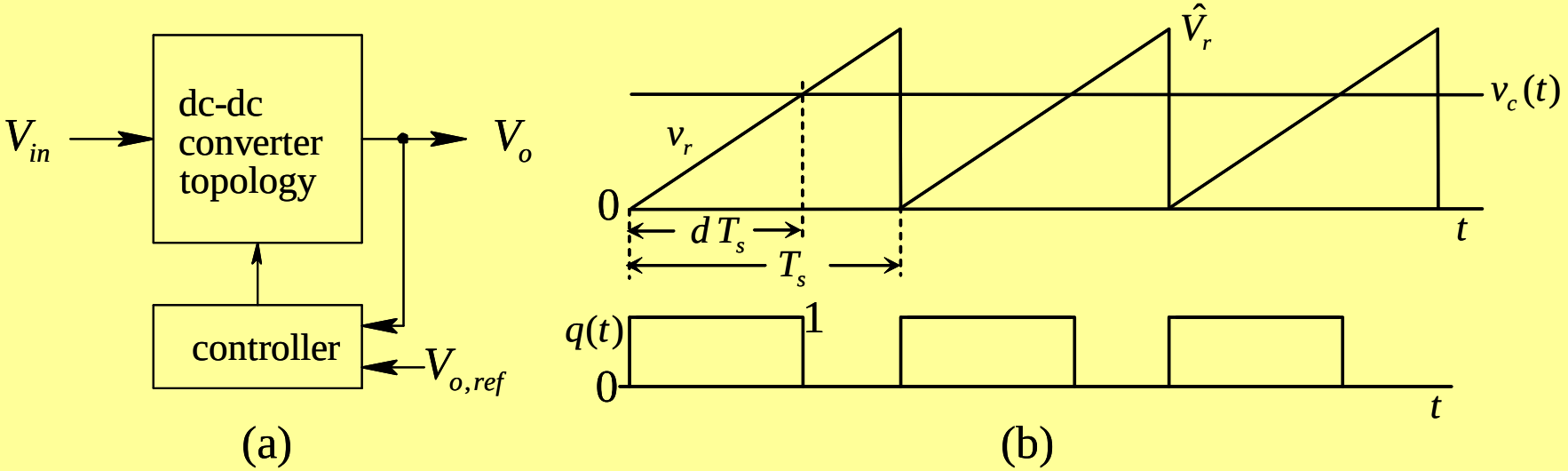
TOPOLOGY SELECTION

Criterion		Buck	Boost	Buck-Boost
Transistor $\hat{V}$		V_{in}	V_o	$(V_{in}+V_o)$
Transistor $\hat{I}$		I_o	I_{in}	$I_{in}+I_o$
I_{rms}	Transistor	$\sqrt{D}I_o$	$\sqrt{D}I_{in}$	$\sqrt{D}\left(I_{in}+I_o\right)$
I_{avg}	Transistor	DI_o	DI_{in}	$D\left(I_{in}+I_o\right)$
	Diode	$(1-D)I_o$	$(1-D)I_{in}$	$(1-D)\left(I_{in}+I_o\right)$
I_L		I_o	I_{in}	$I_{in}+I_o$
Effect of L on C		significant	little	little
Pulsating Current		input	output	both

WORST-CASE DESIGN

The worst-case design should consider the ranges in which the input voltage and the output load vary. As mentioned earlier, often converters above a few tens of watts are designed to operate in CCM. To ensure CCM even under very light load conditions would require prohibitively large inductance. Hence, the inductance value chosen is often no larger than three times the critical inductance $\left(L < 3L_c\right)$, where, as discussed in section 3-15, the critical inductance L_c is the value of the inductor that will make the converter operate at the border of CCM and DCM at full-load.

REGULATION OF DC-DC CONVERTERS BY PWM



$$d(t) = \frac{v_c(t)}{\hat{V}_r}$$

Summary

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