		1960 - Semiconductor memory foreseen? (Fairchild) The following quote from a Company Profile on **Fairchild Semiconductor** published in *Solid State Journal* September/October 1960 shows how aware the founders were of the importance of reducing memory size to the long term growth of their business. But did they see the possibility of semiconductor memory as a solution? "Even though the Fairchild concept (of Micrologic integrated circuits) brings these computer elements in greatly reduced space, further reductions are still possible under current techniques. However, until the reductions are possible in other portions of a computer – especially the memory system – progress will be slower. There's not too much point for a "pea-sized" logic element and a "barrel-sized" memory system, is the way the founders put it."	
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	SRAM	**1961 - Bob Norman proposes integrated circuit memory (Fairchild)** According to Gordon Moore ["Fairchild Chronicles" interview], Bob Norman, the applications engineer working with Jay Last's Micrologic group, suggested that they could build a solid state memory by putting multiple flip-flops on a single integrated circuit chip. It was deemed impractical with the current state of technology.	\
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	SRAM	**1961 - "A few hundred bits of semiconductor memory" shipped (TI)** From "Invention of the Integrated Circuit" by Jack Kilby IEEE Transactions on Electron Devices Vol. ED-23, No.7, July1976, page 653 "In October of that year (1961) TI delivered to the Air Force a small working computer complete with a few hundred bits of semiconductor memory, and announced the Series 51."	\
		1965 – Moore predicts "memories built of integrated electronics" In the 1965 article that first published "Moore's Law," Gordon Moore, Director, Research and Development Laboratories, Fairchild Semiconductor, also predicted that "Computers will be more powerful, and will be organized in completely different ways. For example, memories built of integrated electronics may be distributed throughout the machine instead of being concentrated in a central unit." [Electronics, Volume 38, Number 8, April 19, 1965]	
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	SRAM	**1965 - Monolithic Megabit Memory report (IBM)** Abstracted from: "To the Digital Age" by Rod Bassett page 103 Bob Heale (appointed an IBM Fellow in 1964) collaborated on a January 1965 report "Potential for Monolithic Megabit Memories." That month CD began a 16-bit (bipolar) chip for use in the storage protect circuit of the high-end System/360. In 1967 IBM qualified a 64-bit chip used to implement a cache memory. IBM introduced the16-bit bipolar memory chip in a System/360 Model 95 developed for NASA in1966.	\

		Ref: Bob Donlan and David Pricer, "Pushing the Limits: Looking Forward...Looking Back," Microelectronic Design, Vol. 1. (1987).	
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	SRAM	**1966 – Honeywell 16-bit TTL memory (Transitron, et al)** A group led by Tom Longo created the first commercial multi-cell dedicated memory chip when in 1966 Transitron developed a 16 bit SRAM chip using TTL technology for Honeywell, Billerica, Mass for use as a minicomputer scratchpad memory. This device was alternate sourced by several suppliers of TTL logic, including Fairchild and TI. See: Longo Transcript 8.14.06	\
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	DRAM	**1966 – Single transistor DRAM Cell Invented (IBM)** The single transistor Dynamic Random Access Memory - DRAM memory cell was invented by IBM researcher Robert Dennard as a simpler alternative to the earlier multi-transistor SRAM memory cell. Bio at: http://domino.watson.ibm.com/comm/pr.nsf/pages/news.20050422_bobdennard.html	
	BUBBLE	**1966 - Magnetic-bubble memories invented (Bell Labs)** Andrew Bobeck working with Richard C. Sherwood and Umberto F. Gianola used semiconductor lithographic and deposition methods to build non-volatile magnetic bubble memories of 4096-bit capacity in the mid-1960s. Intel introduced a1Megabit device in xxx. Their promise dimmed with the development of faster, lower-cost disk drives "State Of The Art" by Stan Augarten: http://smithsonianchips.si.edu/augarten/p20.htm	
	SRAM	**1967 - 64-bit MOS RAM Project (Fairchild)** From: "To the Digital Age" by Rod Bassett page 358 "In April 1967, Fairchild essentially restarted the integrated MOST memory project now called SAM (Semiconductor Advanced Memory) which was transferred to the physics department in July 1967. The project was still attempting to build a 64-bit memory chip, the same density Fairchild R&D had been working on in 1964. "Monthly Technical Summary Physics," July 1967, 27, Box 14, Folder 2." [In the Stanford Special Collections archives]	
	SRAM	**1968 - 64-bit Bipolar TTL RAM (Fairchild, et al)** Organized 16 words x 4-bits this device was a four times larger version of the Honeywell/Transitron 16-bit TTL RAM. Packaged in a 16-pin DIP, typical access time was 60ns. The original vendor was either Fairchild (4103/93403) or TI (7489). The device was alternate sourced by several companies including AMD (AM 3103). The 3101 introduced in 1969 was Intel's first product and the first version to employ Schottky TTL technology.	
	SRAM	**1968 - Multichip memory projects (CMT, Fairchild, Intel)**	

		The **Fairchild** SAM project was extended to a multichip configuration to supply a high density memory system for Burroughs. With SAM now re-designated Semiconductor Advanced Memory, it involved mounting sixteen 64-bit MOS RAM chips face down bonded to an 80-lead metallized ceramic substrate. Multiple 1024-bit packages were then stacked vertically and interconnected to create a semiconductor memory sub-system. A December 1968 report to Security Analysts includes a photograph of the SAM package. The project was eventually cancelled due to poor reliability of the chip attach technology. Tony Holbrook (former president of AMD) left Fairchild in the early 1970's to work for Computer Micro-Technology (CMT), a start-up created to pursue multi-chip memory modules using beam-lead technology. They failed due to cracking of the beams. In "The Man behind the Microchip" page 180, Leslie Berlin describes Intel's multi-chip memory effort in 1969; "Intel had no problem building the individual memory chips but could not reliably attach them to their ceramic base." Motorola, TI and other also had a multi-chip memory programs around the same time.	
PROM	**1969 – PROM**	
		Based on an earlier development of the diode matrix, Radiation Inc. (later Harris Semiconductor) developed the first PROM, user programmable by blowing Ni-chrome fuses. This device soon became widely popular among computer designers as a medium for easily loading and debugging and changing "firmware" microcode, the internal instructions that the CPU uses to decode and execute the external software instructions that comprise of the operating and applications programs.	
CCD	**1969 – CCD as Memory**	
		The invention of the CCD was by Willard S. Boyle and George E. Smith at BTL in 1969. Later developed into image capture devices at Fairchild by Gil Amelio and Jim Early, a former BTL employee..	
SRAM	**1970 - 256-Bit Bipolar TTL RAM and system for Illiac IV (Fairchild)**	
		Based on an earlier test chip created by Wendell Sander, H. T. (Hua-Thye) Chua designed the 4100 (aka 93400) the first 256-bit bipolar TTL RAM introduced by Fairchild in 1970. The partially-decoded array of 16 by 16 six-transistor SRAM cells organized 256 words x 1 bit offered a 100 nsec access time in a 16-pin DIP. This device was used by a group managed by Rex Rice at Fairchild R & D to build the Processor Element Memory (PEM) system for the Burroughs Illiac IV supercomputer. This is believed to be the first mainframe computer to employ semiconductor main memory. See: 'Notes from Interview with Wendell Sander' by Jeff Katz "State Of The Art" by Stan Augarten: http://smithsonianchips.si.edu/augarten/p24.htm	
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DRAM	**1970 - First commercial DRAM (Intel 1103)** Intel announced the first commercially successful 1024-bit Dynamic RAM (DRAM) based on Dennard's dynamic cell concept in 1970. Designed by former Honeywell engineer William Regitz and Joel Karp, other contributors to the product included cell improvements by Ted Hoff and Ted Rowe and circuit design assistance by Leslie Vadasz, Bob Abbott. Product engineer was John Reed. The 1103 was slow and difficult to make and use but established the viability of low cost semiconductor memories in computers. "State Of The Art" by Stan Augarten: http://smithsonianchips.si.edu/augarten/p26.htm From: http://www.mpoweruk.com/history.htm	
EPROM	**1971 - First Erasable PROM (Intel 1702)** Designed by Dov Frohman formerly of Bell Labs, the Intel1702 2048-bit Erasable Programmable Read-Only Memory (EPROM) was the first commercial application of a floating gate technique proposed by Kahng and Sze also of Bell Labs. The first devices were programmed electrically but required a quartz window package so they could be erased by exposure to ultra violet light. One Time Programmable (OTP) versions offered lower cost but could not be erased. "State Of The Art" by Stan Augarten: http://smithsonianchips.si.edu/augarten/p32.htm	
SRAM	**1971 - Fast 256-bit Oxide-Isolated Bipolar TTL RAM (Fairchild 94310)** A 256-bit TTL RAM (93401) was the first device fabricated with an oxide-isolated (Isoplanar) bipolar process developed by Fairchild. It provided a 50% size reduction and 30% speed improvement over junction isolation. This technology allowed Fairchild to dominate the high-performance memory market for many years. (Electronics March 29, 1971)	
SRAM	**1972 – Fast 1024-bit Oxide-Isolated TTL and ECL RAMs (Fairchild 94315, 95415)**	
SRAM	**1972 – Intel 2107 4K ?**	
DRAM	**1973 – First 4K DRAM ?**	

		TI Introduces 22-pin DRAM	
	DRAM	**1973 – 4K DRAM in 16-pin Package** Mostek MK 4096 multiplex addressing allowed a small package (16-pin) size and established Mostek as a world leader in dynamic RAMs in terms of volume production and also as a design innovator. The "official" pinout for the 4K DRAM generation was 22-pins. However, the MK4096 4K DRAM featured multiplexed addresses that permitted space-saving 16-pin packaging. For over a year, the industry seemed uncertain as to which design would become standard. Mostek fellow Bob Proebsting, who invented and developed the multiplexed address concept, comments that even though more and more customers were endorsing Mostek's smaller 16-pin design, the trade press continued to refer to our pinout as "the maverick 4K package." Eventually, the Mostek pin configuration did become the industry standard, not only for 4K DRAMs, but also for the next three generations of DRAMs - the 16K DRAMs, the 64K DRAMs and even the 256K DRAMs The MK4096 4KRAM included other noteworthy design innovations, such as a sense amplifier design and a clock generator design - and others -which allowed the MK4096 to consume less than half the power of competitive circuits http://www.mindspring.com/~mary.hall/mosteklives/history/15Ann/MostekFirsts.html	
	EPROM	**1974 – 8K N-Channel EPROM** Intel 2708, developed by George Perlegos, to complement the newly introduced N-Channel 8080 microprocessor.	
	DRAM	**1974 - First 4K - bit DRAM with 1T Cell** [http://www.icknowledge.com/history/history.html] The 4Kbit DRAM introduced the 1 transistor cell and the silicon gate NMOS process. The 3T to 1T memory cell transition is the first major DRAM transition. The silicon gate NMOS process required 6 masks and had 8µm minimum features. The resulting product had a 1,280µm2 memory cell size, a die size of approximately 15mm^2 and sold for around $18 at introduction.	
	DRAM	**1976 - 16K - bit DRAM introduced** [http://www.icknowledge.com/history/history.html] The 16Kbit DRAM introduced dual polysilicon layers allowing more efficient memory cell layout. The single to dual polysilicon layer transition is the second major DRAM transition. The dual polysilicon NMOS process required 7 masks and had 5µm minimum features. The resulting product had a 500µm^2 memory cell size, a die size of approximately 19mm^2 and sold for around $33 at introduction.	
	DRAM	**1976 - Mostek 16K** http://smithsonianchips.si.edu/augarten/p50.htm	

EPROM	**1976 – Intel 2716 – first 5-voly only EPROM** Developed by George Perlegos, this device complemented the 5-voly only 8085 microprocessor. It was the first EPROM to incorporate an on-chip charge-pump to develop the required high voltages for programming the device without a separate power supply voltage input. I greatly simplified microprocessor-based system design and manufacturing.	
DRAM	**1977 - The First 65,536-Bit (64K) Dynamic RAM (IBM)** http://smithsonianchips.si.edu/augarten/p56.htm	
DRAM	**1979 - 64K-bit DRAM introduced** [http://www.icknowledge.com/history/history.html] The 64Kbit DRAM was produced on a dual polysilicon NMOS process requiring 8 to 10 masks and had 3µm minimum features. The resulting product had a $180µm^2$ memory cell size, a die size of approximately $31mm^2$ and sold for around \$47 at introduction	
DRAM	**1980 - One of the Most Popular 65,536-Bit (64K) Dynamic RAMs** http://smithsonianchips.si.edu/augarten/p64.htm	
DRAM	**1981 - The First 294,912-Bit (288K) Dynamic RAM** http://smithsonianchips.si.edu/augarten/p66.htm	
DRAM	**1982 - 256K-bit DRAM** [http://www.icknowledge.com/history/history.html] Initially, the 256Kbit DRAM was produced on a dual polysilicon NMOS process requiring 8 to 10 masks and had 2µm minimum features. The resulting product had a $70µm^2$ memory cell size, a die size of approximately $45mm^2$ and sold for around \$51 at introduction. Later versions converted to CMOS with 1.5µm features.	
DRAM	**1983 - 1st CMOS DRAM** [http://www.icknowledge.com/history/history.html] Intel develops a 1Mbit CMOS DRAM, the 1st CMOS DRAM. Ironically Intel soon exits the DRAM business.	
EEPROM	**1983 - EEPROM Invented** 16Kbit EEPROMs introduced based on the floating gate and MNOS Reference: WG. Groeseneken, H.E. Maes, J. Van Houdt, and J.S. Witters, "Basics of Nonvolatile Semiconductor Memory," in William D. Brown and Joe E. Brewer Eds. "Nonvolatile Semiconductor Memory Technology", IEEE Press (1998). [Found at: http://www.icknowledge.com/history/history.html]	
FLASH	**1984 - Flash memory invented by Fujio Masuoka of Toshiba** Fujio Masuoka of Toshiba disclosed at IEDM the invention of a Flash, a form of Electrically-Erasable Programmable Read-Only Memory (EEPROM) that allows multiple memory locations to be erased or written in one programming operation, at	

	Toshiba in 1984. It uses floating gate construction and depends on quantum tunneling effects induced by relatively high voltages for both writing and erasing. The architecture also required only a single transistor per memory cell rather than 2 transistors per cell the way standard EEPROM did. Flash memory is commonly used in USB memory sticks. "Fujio Masuoka: Thanks For The Memory" http://www.businessweek.com/magazine/content/06_14/b3978021.htm	
FLASH	**1985 - Commercial Flash memory introduced** [http://www.icknowledge.com/history/history.html] Toshiba introduces a 256Kbit flash memory chip.	
FLASH	**1986 - ETOX style Flash introduce** 256Kbit introduced by Intel. ETOX is the most common style of Flash today. Reference: Manzur Gill and Stefan Lai, "Floating Gate Flash Memories," in William D. Brown and Joe E. Brewer Eds. "Nonvolatile Semiconductor Memory Technology", IEEE Press (1998). [Found at: http://www.icknowledge.com/history/history.html]	
DRAM	**1986 - 1M-bit DRAM** The 1Mbit DRAM introduced the use of non-planar DRAM memory cells such as stacked or trench cells, although some planar cells were also produced. The transition from a planar to a non planar cell is the third major DRAM transition. The 1Mbit DRAM was produced on a CMOS process requiring approximately 18 masks with 2 to 3 polysilicon layers and 1.2µm minimum features. The resulting product had a $25µm^2$ memory cell size, a die size of approximately $70mm^2$ and sold for around $100 at introduction. [Found at: http://www.icknowledge.com/history/1980s.html]	
DRAM	**1988 - 4M-bit DRAM** [http://www.icknowledge.com/history/history.html] The 4Mbit DRAM was produced on a CMOS process requiring 20 to 25 masks, with 2 to 3 polysilicon layers, 2 metal layers and 0.8µm minimum features. All 4Mbit memory was produced with a stacked or trenched cell, 1Mbit DRAM was the end of the planar cell. The resulting product had a $12µm^2$ memory cell size, a die size of approximately $95mm^2$ and sold for around $124 at introduction. Later versions utilized smaller line widths to shrink the die. [Found at: http://www.icknowledge.com/history/1990s.html]	
	1991 - 16M-bit DRAM The 16Mbit DRAM was produced on a CMOS process with 3 to 4 polysilicon layers, 2 metal layers and 0.5µm minimum features. The resulting product had a $4.2µm^2$ memory cell size, a die size of approximately $130mm^2$ and sold for around $275 at introduction. Later versions utilized smaller line widths to shrink the die. [Found at: http://www.icknowledge.com/history/1990s.html]	
	1994 - 64M-bit DRAM The 64Mbit DRAM was produced on a CMOS process with 3 to 5 polysilicon layers, 2 to 3 metal layers and 0.35µm minimum features. The resulting product had a $1.5µm^2$ memory cell size, a die size of approximately $170mm^2$ and sold for around	

		$575 at introduction. Later versions utilized smaller line widths to shrink the die. [Found at: http://www.icknowledge.com/history/1990s.html]	
		1998 - 256M-bit DRAM The 256Mbit DRAM was produced on a CMOS process with 4 to 5 polysilicon layers, 2 to 3 metal layers and 0.25µm minimum features. The 256Mbit DRAM introduced the use of high-k dielectrics, although many parts are also produced without high-k, high-k dielectric represents the fourth major DRAM transition. The resulting product had a die size of approximately 204mm^2 and sold for around $575 at introduction. Later versions utilized smaller line widths to shrink the die [Found at: http://www.icknowledge.com/history/1990s.html]	