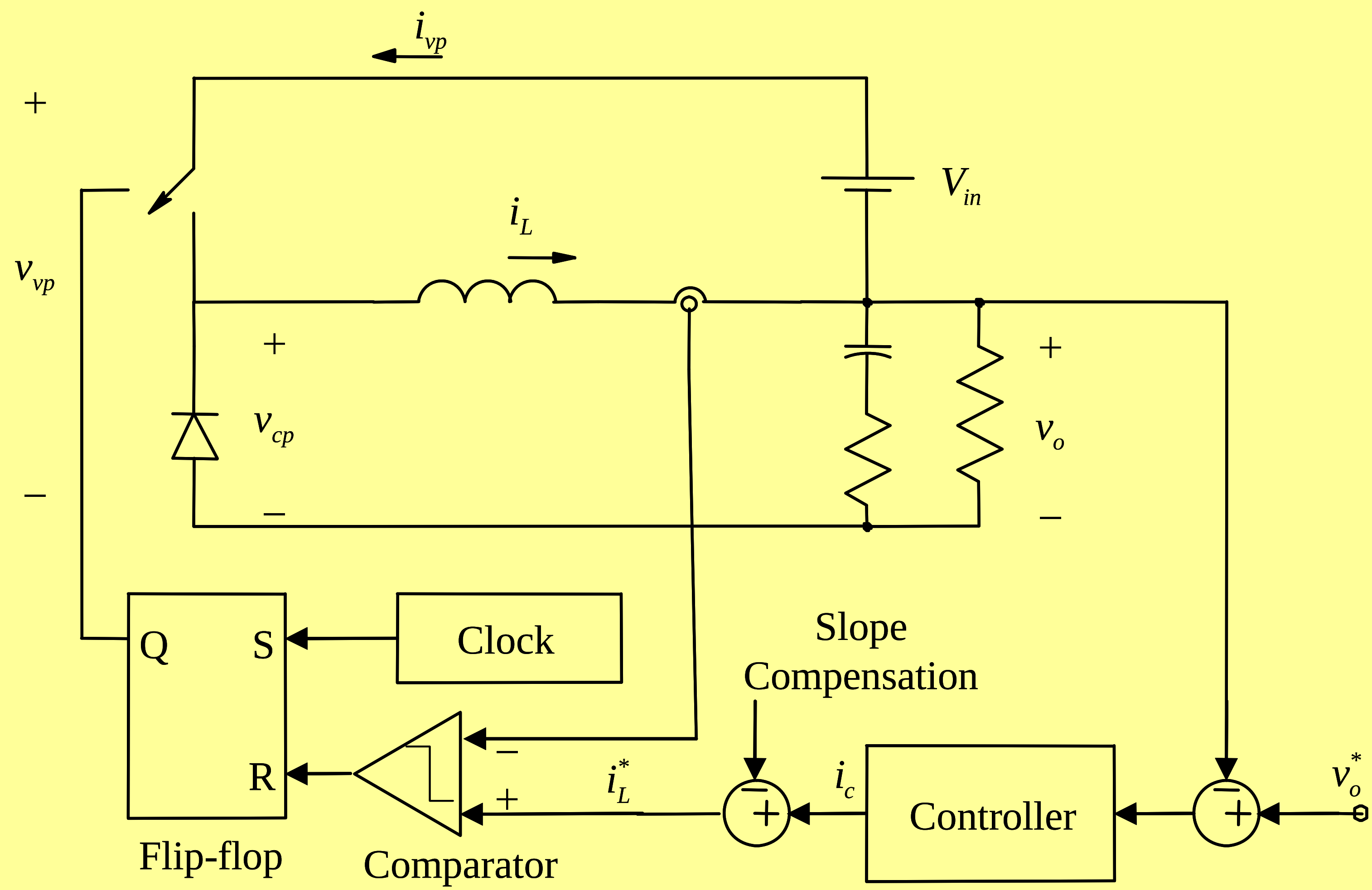
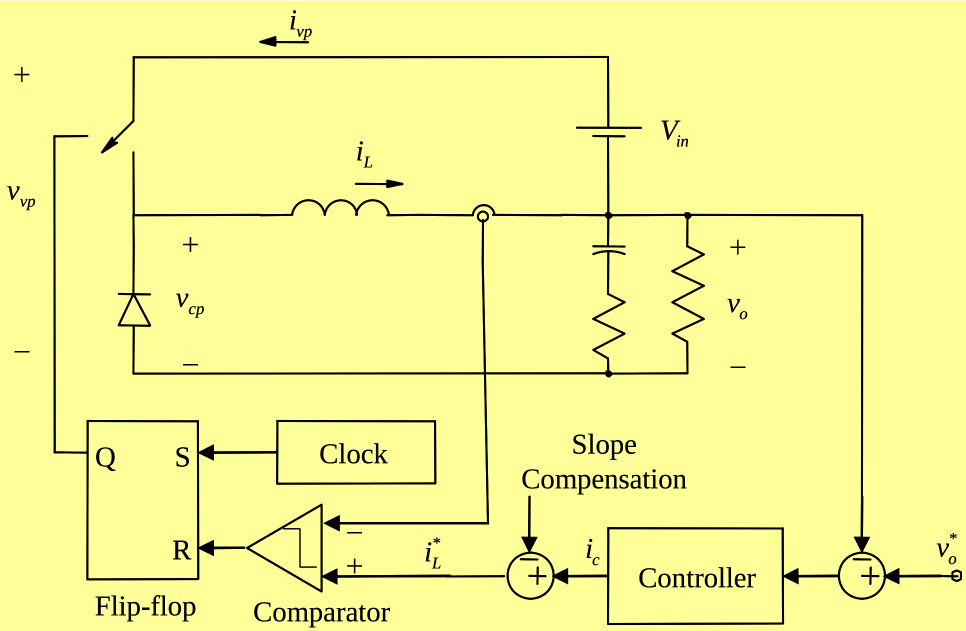
Feedback Control Design in Regulated DC Power Supplies

- Peak-Current-Mode Control
- Control in Discontinuous-Conduction Mode (DCM)

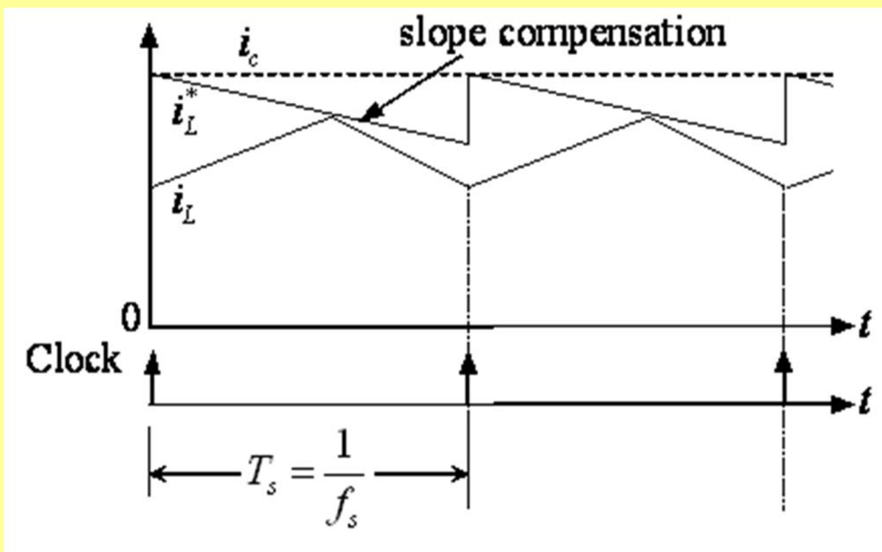
PEAK-CURRENT MODE CONTROL

- Peak-Current-Mode Control, and
- Average-Current-Mode Control.

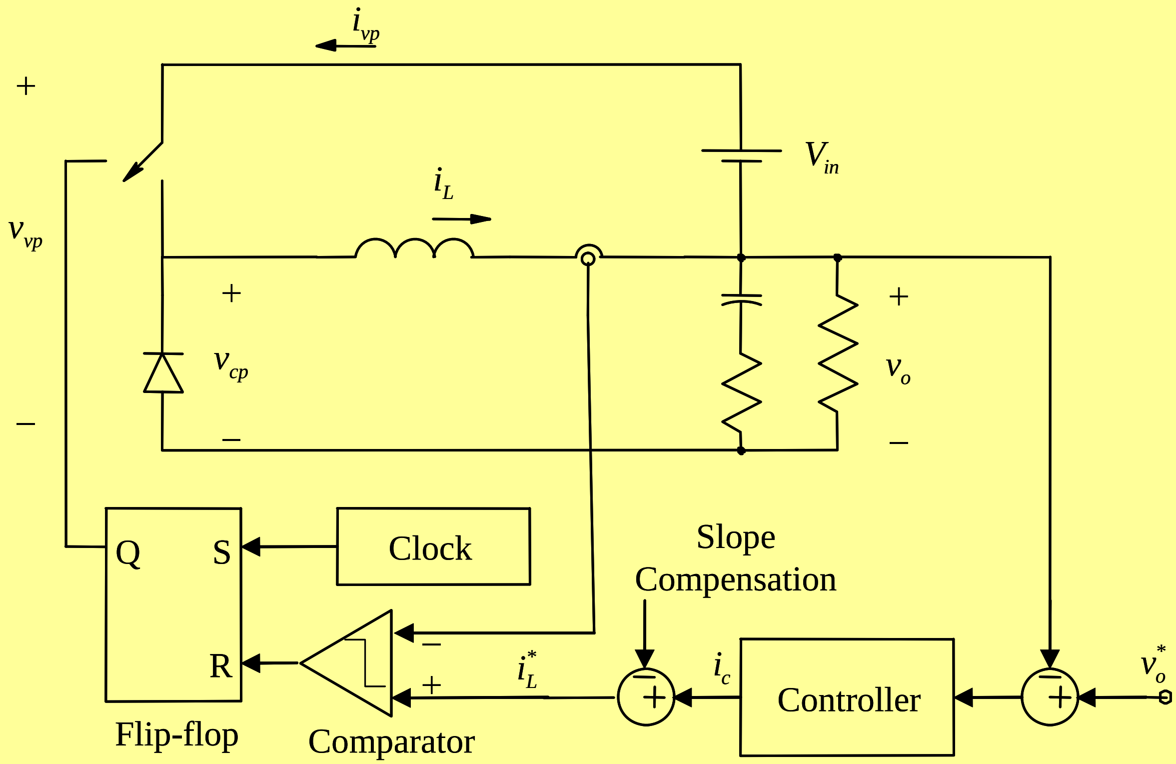


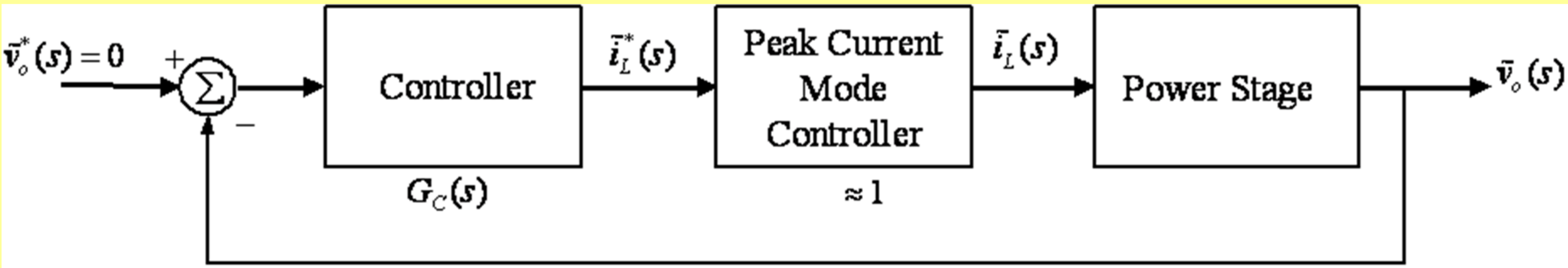


i_{vp}
+
V_{in}
i_L
v_{vp}
+
v_{cp}
–
+
v_o
–
–
Q
S
Clock
Slope
Compensation
R
–
+
i_L^*
i_c
Controller
v_o^*
Flip-flop
Comparator

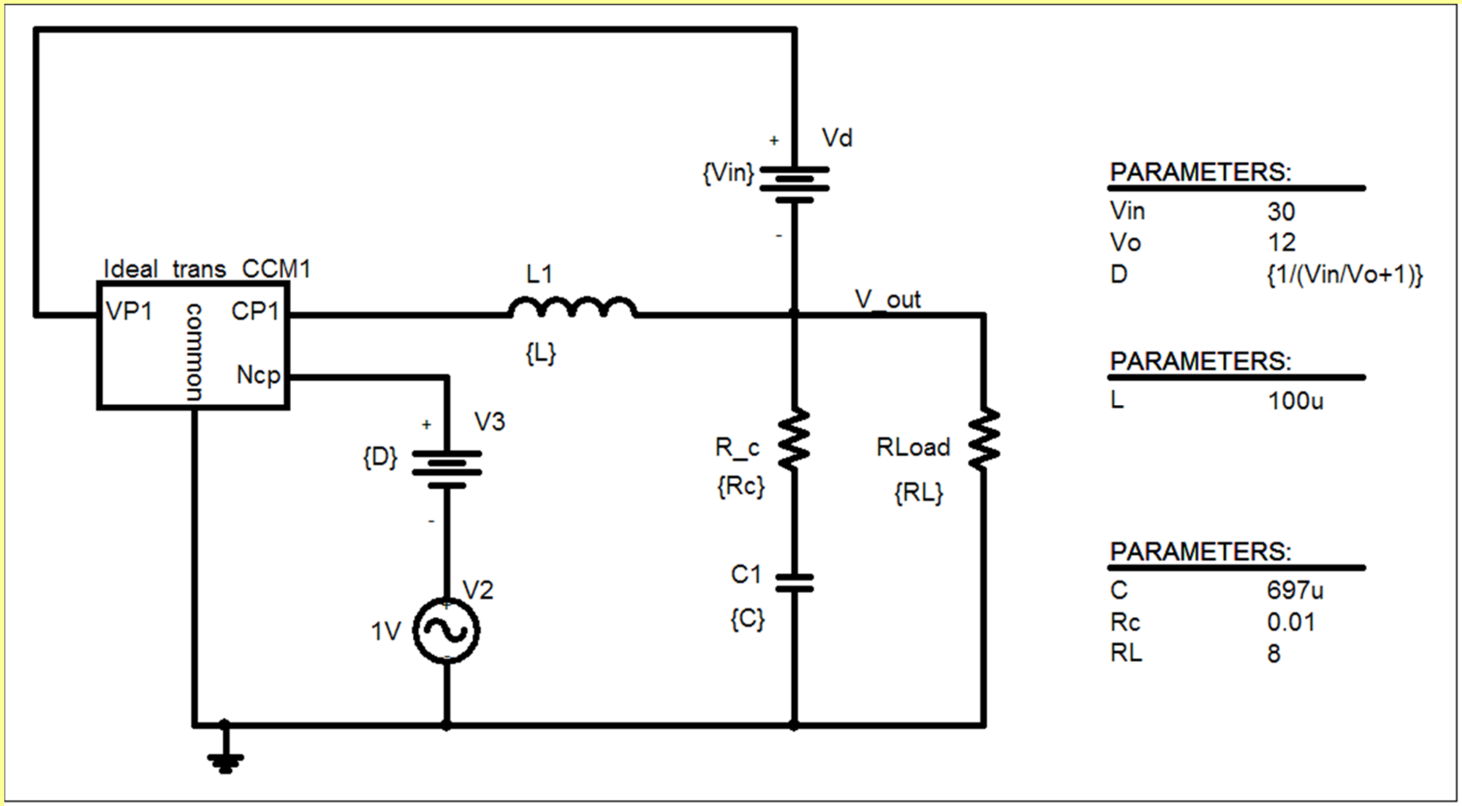


i_c
slope compensation
i_L^*
i_L
0
t
Clock
t
$T_s = \frac{1}{f_s}$

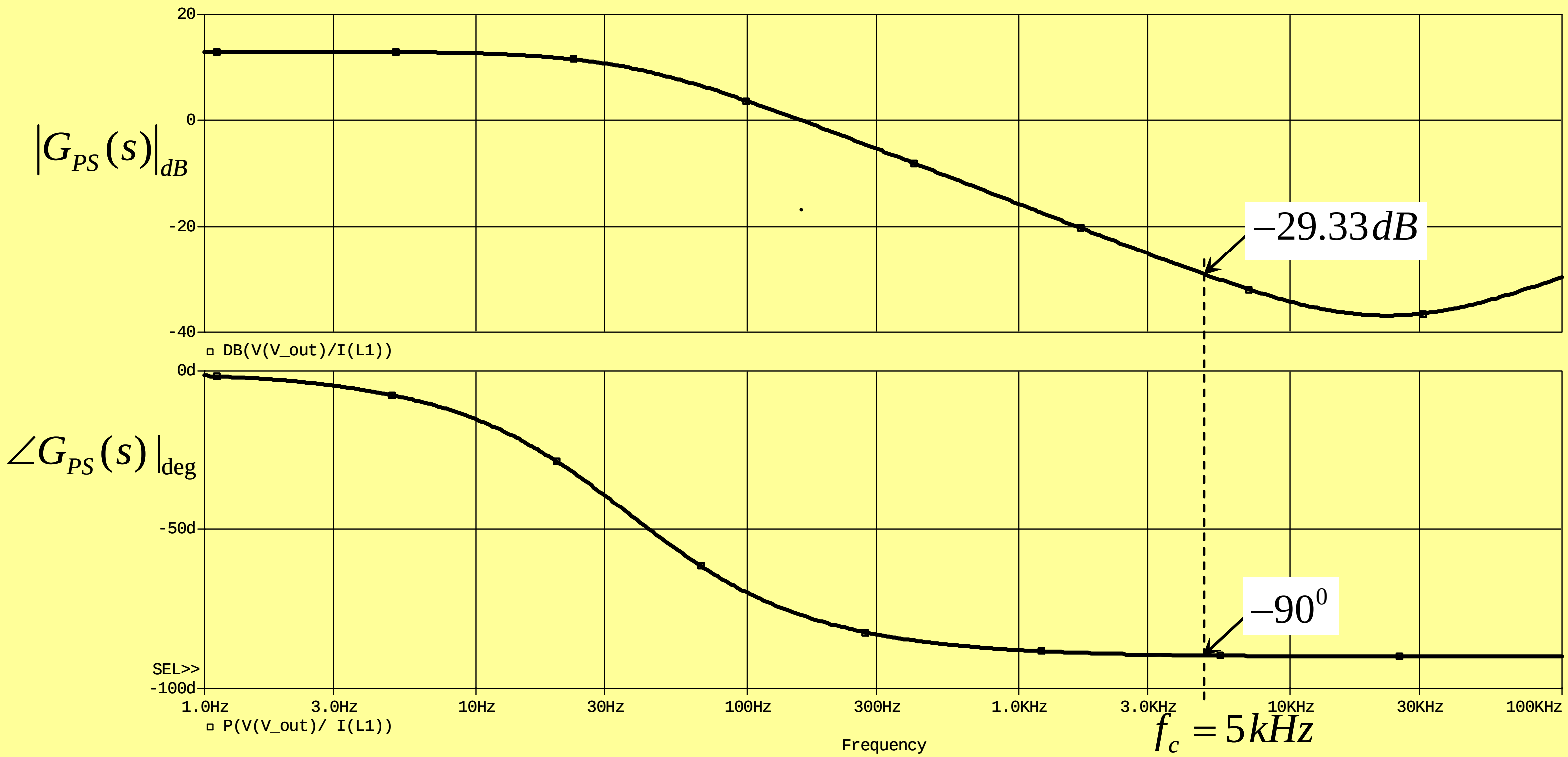

i_{vp}
+
V_{in}
i_L
v_{vp}
+
v_{cp}
+
v_o
–
–
–
Q
S
Clock
Slope
Compensation
R
–
+
i_L^*
i_c
Controller
v_o^*
Flip-flop
Comparator


$\tilde{v}_o^*(s) = 0$
+
–
Controller
$G_C(s)$
$\tilde{i}_L^*(s)$
Peak Current
Mode
Controller
≈ 1
$\tilde{i}_L(s)$
Power Stage
$\tilde{v}_o(s)$

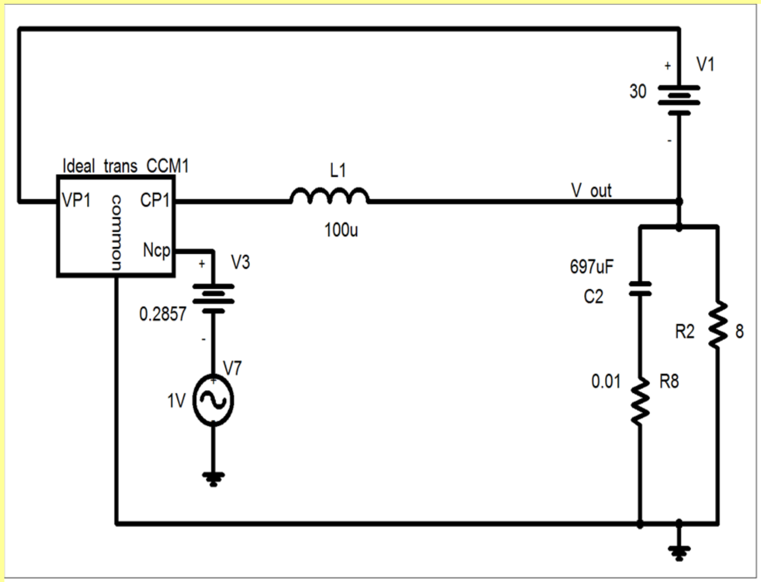
In this example, we will design a peak-current-mode controller for a Buck-Boost converter that has the following parameters and operating conditions: $L = 100\,\mu\text{H}$, $C = 697\,\mu\text{F}$, $r = 0.01\Omega$, $f_s = 100\text{ kHz}$, $V_{in} = 30\text{V}$. The output power $P_o = 18\text{W}$ in CCM and the duty-ratio D is adjusted to regulate the output voltage $V_o = 12\text{V}$. The phase margin required for the voltage loop is 60^0. Assume that in the voltage feedback network, $k_{FB} = 1$.

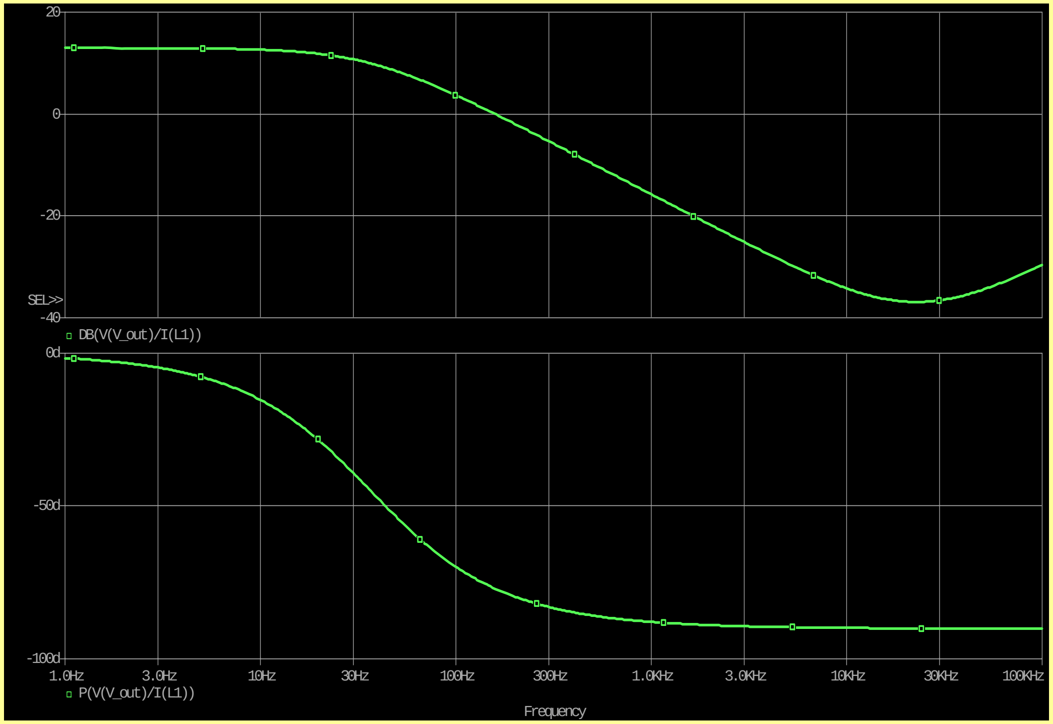


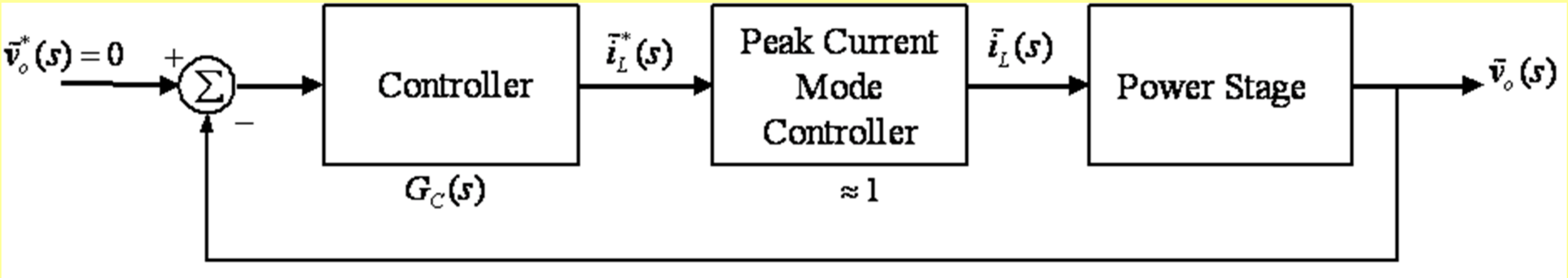
$$\frac{\tilde{v}_o}{\tilde{i}_L}(s) = \frac{R(1-D)\left(1 - \frac{sLD}{R(1-D)^2}\right)(1 + srC)}{(1+D)\left(1 + \frac{sRC}{1+D}\right)}$$



PSpice Modeling:

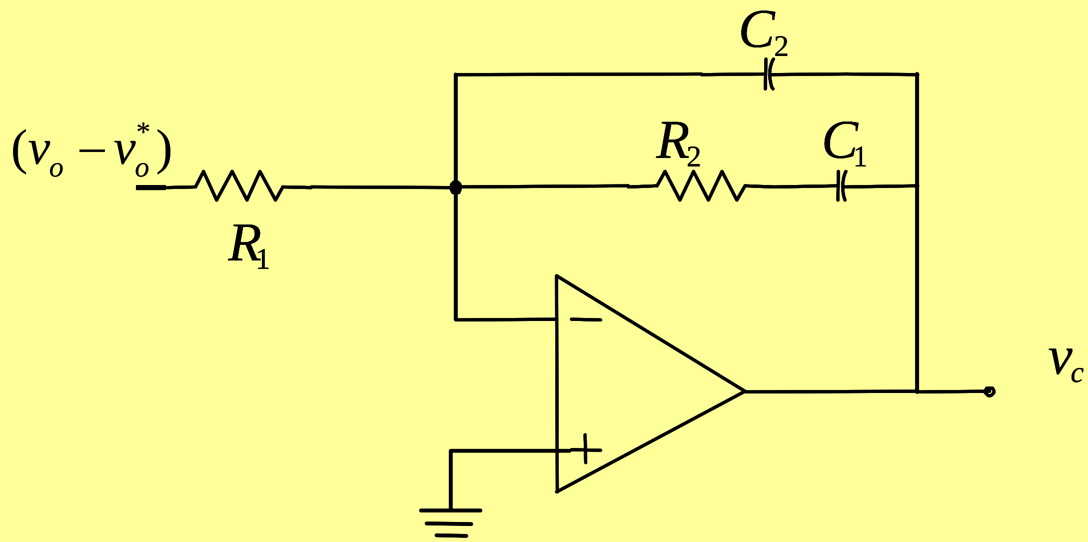






$$G_c(s) = \frac{k_c}{s} \frac{(1+s/\omega_z)}{(1+s/\omega_p)} \qquad f_c = \sqrt{f_z f_p} \qquad \sqrt{\frac{f_p}{f_z}} = \tan\left(45^o + \frac{\phi_{boost}}{2}\right)$$

$$\left|G_C(s)\right|_{f_c} \times \left|G_{PS}(s)\right|_{f_c} = 1$$

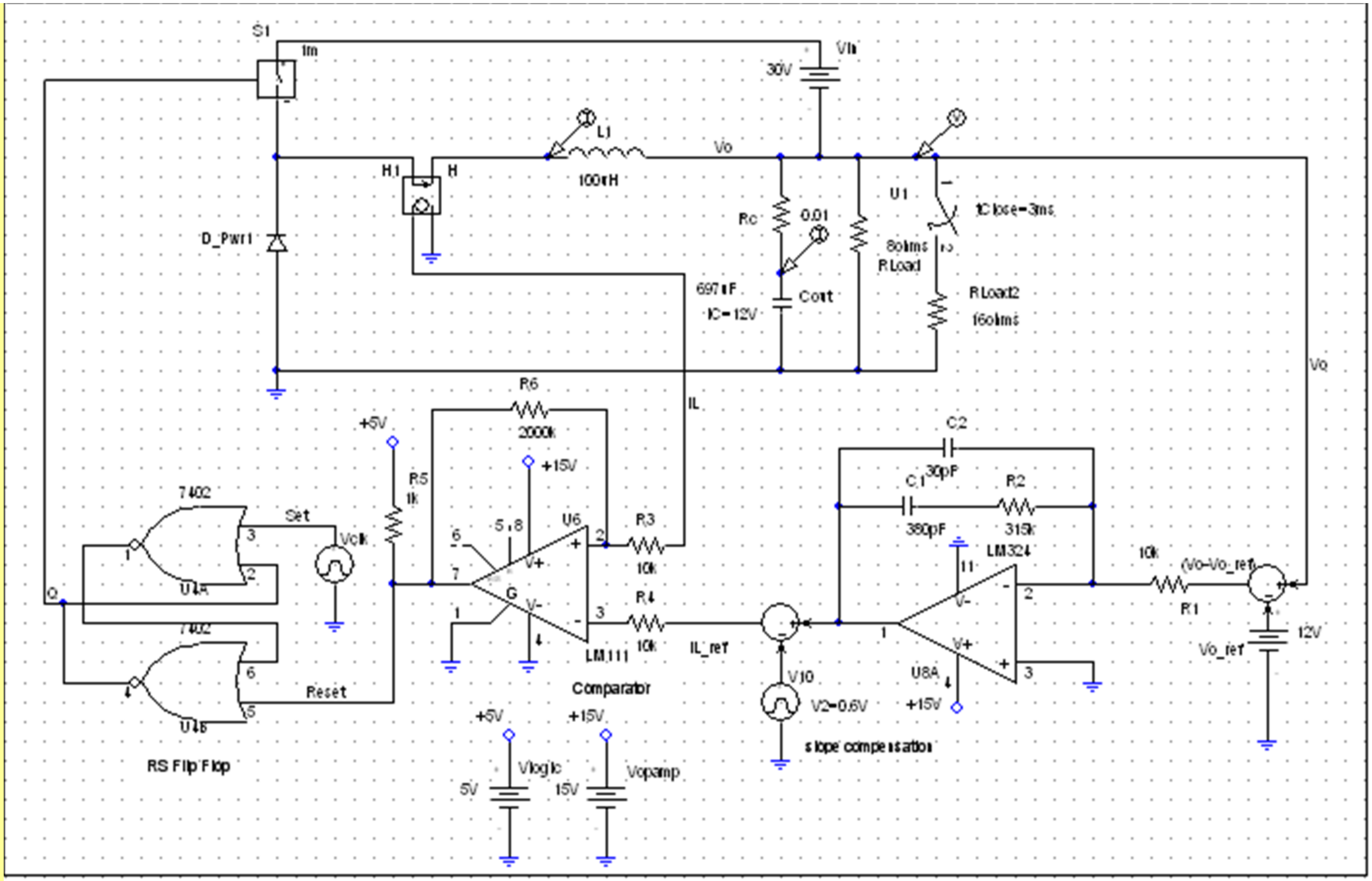


$$R_1 = 10\,k\Omega$$

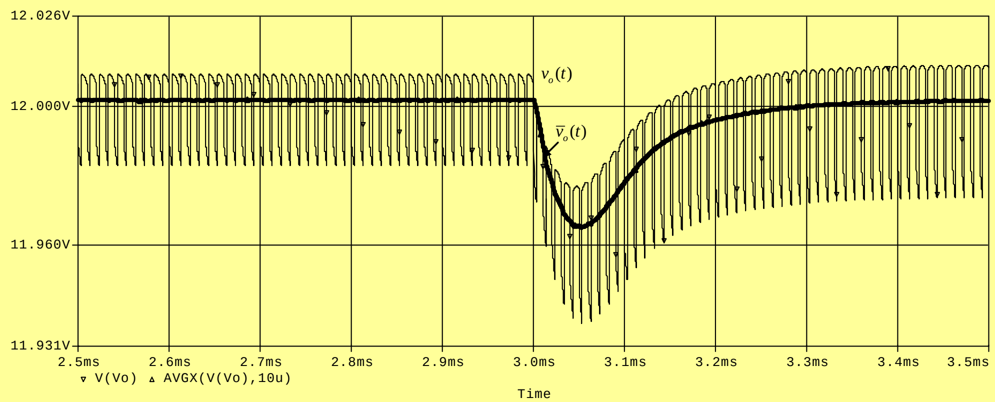
$$C_2 = \frac{\omega_z}{\omega_p R_1 k_c} = 30\ pF$$

$$C_1 = C_2\left(\omega_p / \omega_z - 1\right) = 380\,pF$$

$$R_2 = 1/(\omega_z C_1) = 315\,k\Omega$$



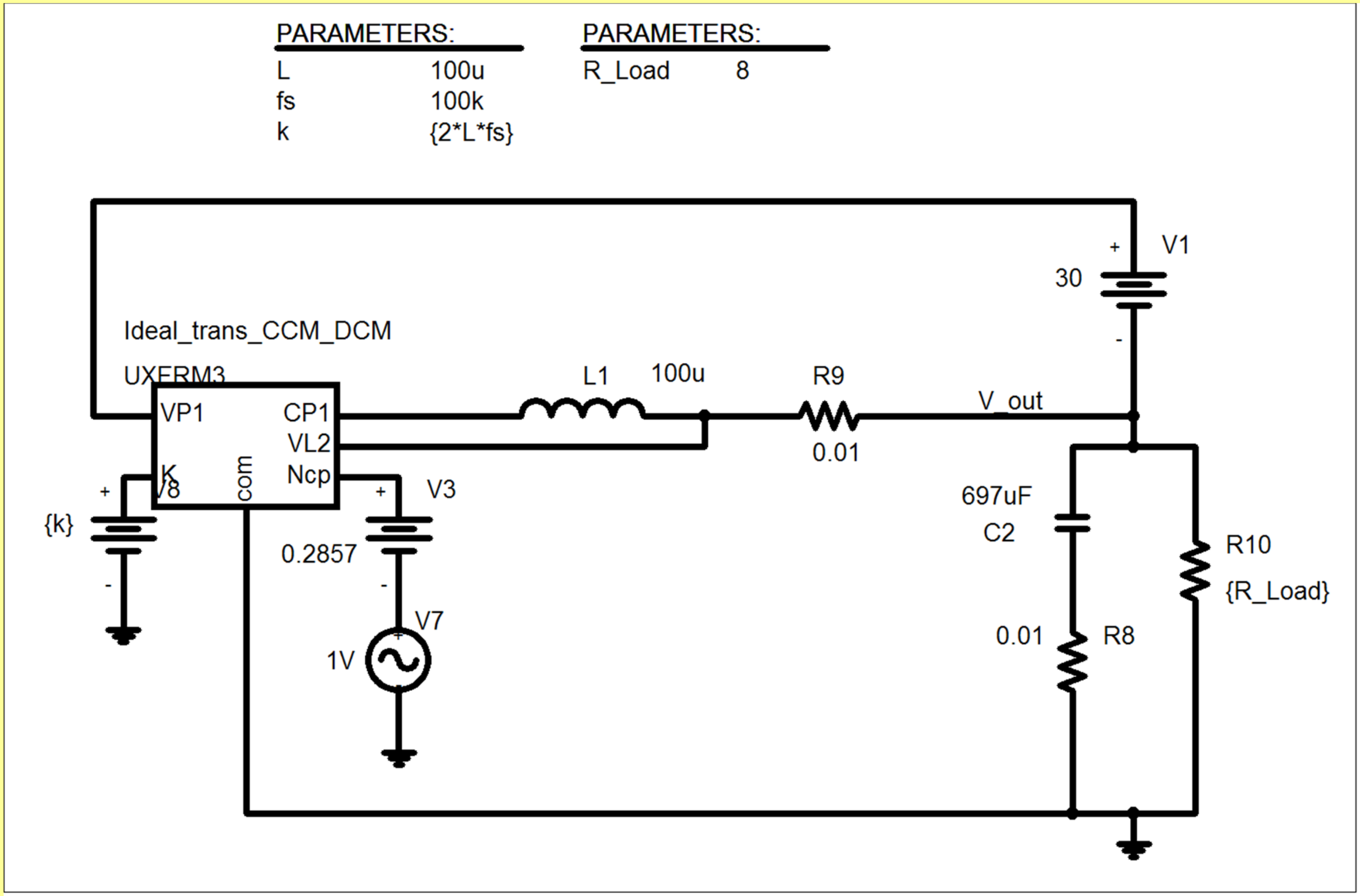
S1
1m
Vin
30V
L1
100uH
Vo
H1
H
D_Pwr1
Rc
0.01
U1
tClose=3ms
8ohms
RLoad
RLoad2
16ohms
697uF
IC=12V
Cout
Vo
IL
R6
2000k
+5V
R5
1k
+15V
U6
R3
10k
R4
10k
IL_ref
LM111
Comparator
7402
Set
Vclk
U4A
U4B
Reset
RS Flip Flop
C2
30pF
C1
380pF
R2
315k
LM324
10k
R1
(Vo-Vo_ref)
12V
Vo_ref
V10
V2=0.6V
U8A
+15V
slope compensation
Vlogic
5V
Vopamp
15V



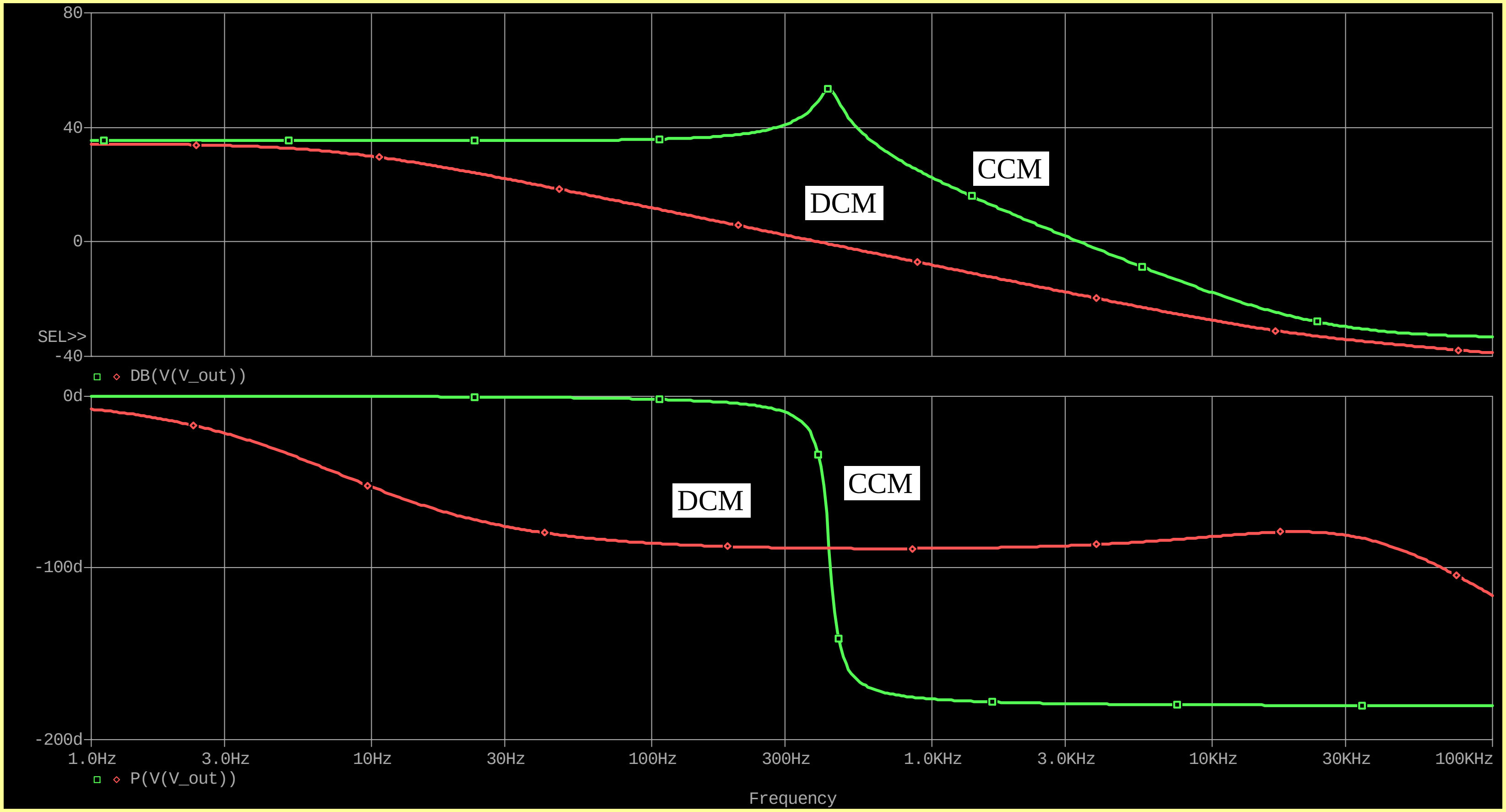
12.026V
12.000V
11.960V
11.931V
$v_o(t)$
$\bar{v}_o(t)$
2.5ms
2.6ms
2.7ms
2.8ms
2.9ms
3.0ms
3.1ms
3.2ms
3.3ms
3.4ms
3.5ms
V(Vo) AVGX(V(Vo),10u)
Time

FEEDBACK CONTROLLER DESIGN IN DCM

PSpice Modeling:



Simulation Results



Summary

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