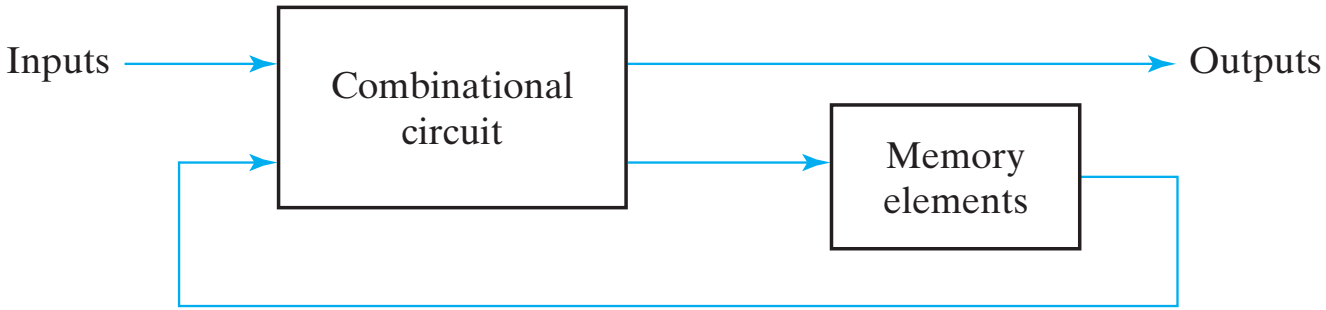
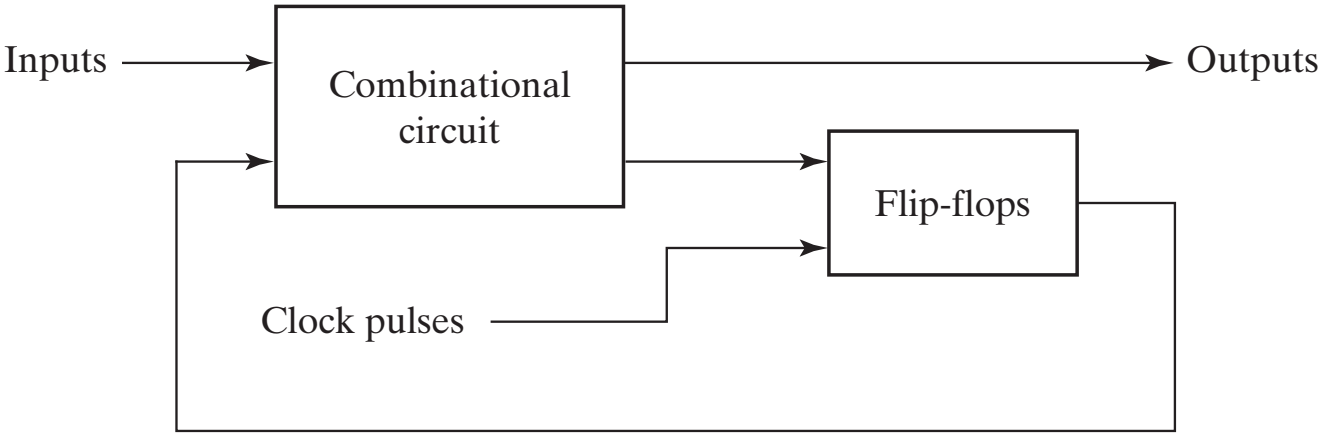


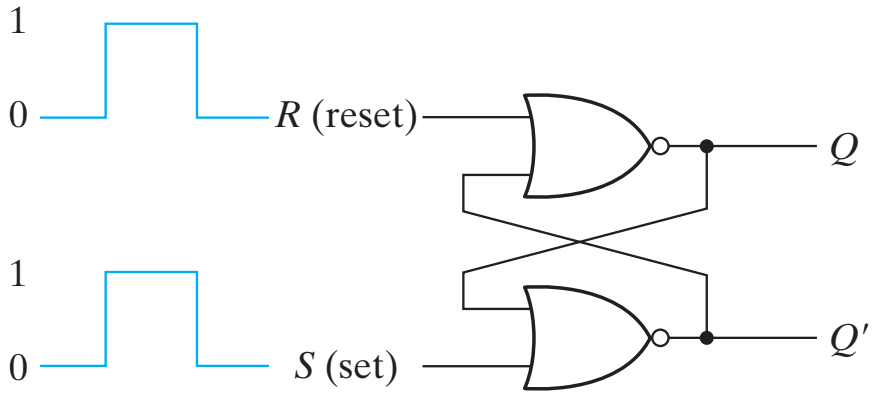
Fig. 5-1 Block Diagram of Sequential Circuit



(a) Block diagram

(b) Timing diagram of clock pulses

Fig. 5-2 Synchronous Clocked Sequential Circuit

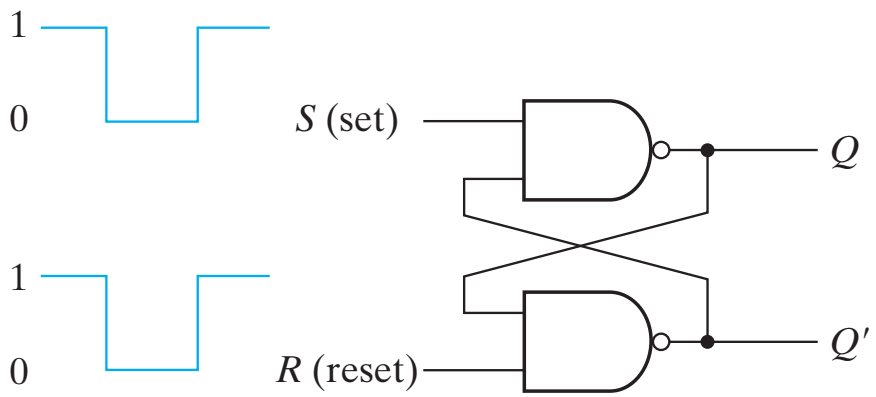


(a) Logic diagram

S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after $S = 1, R = 0$)
0	1	0	1	
0	0	0	1	(after $S = 0, R = 1$)
1	1	0	0	

(b) Function table

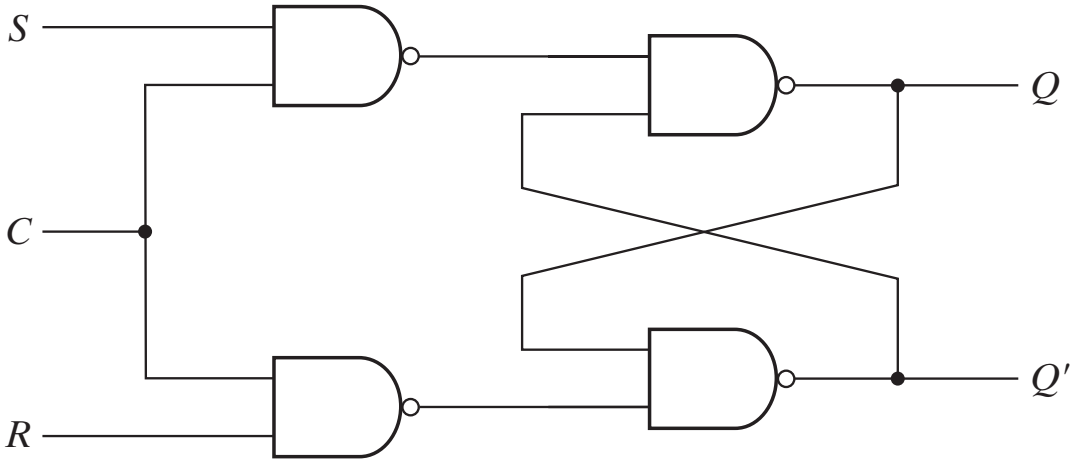
Fig. 5-3 *SR* Latch with NOR Gates



S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	

(a) Logic diagram (b) Function table

Fig. 5-4 *SR* Latch with NAND Gates

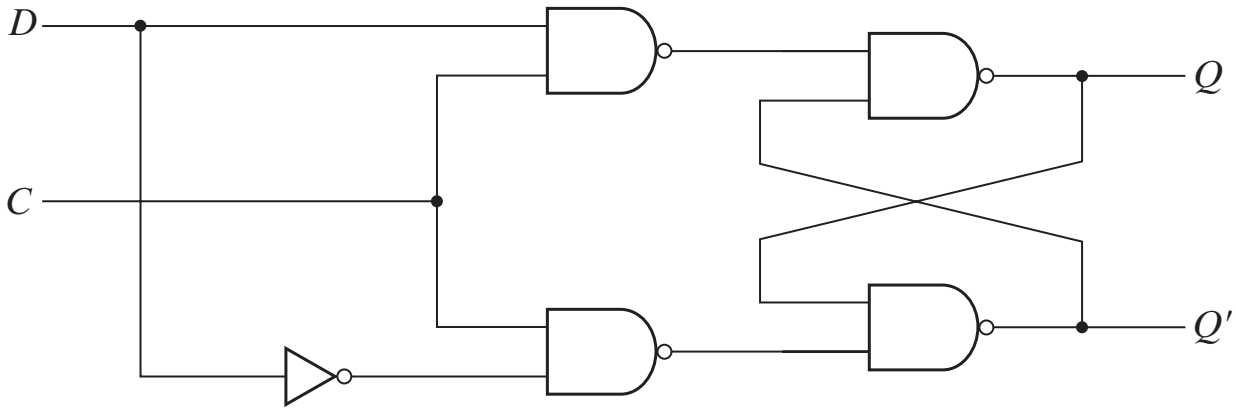


(a) Logic diagram

C	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$; Reset state
1	1	0	$Q = 1$; set state
1	1	1	Indeterminate

(b) Function table

Fig. 5-5 SR Latch with Control Input

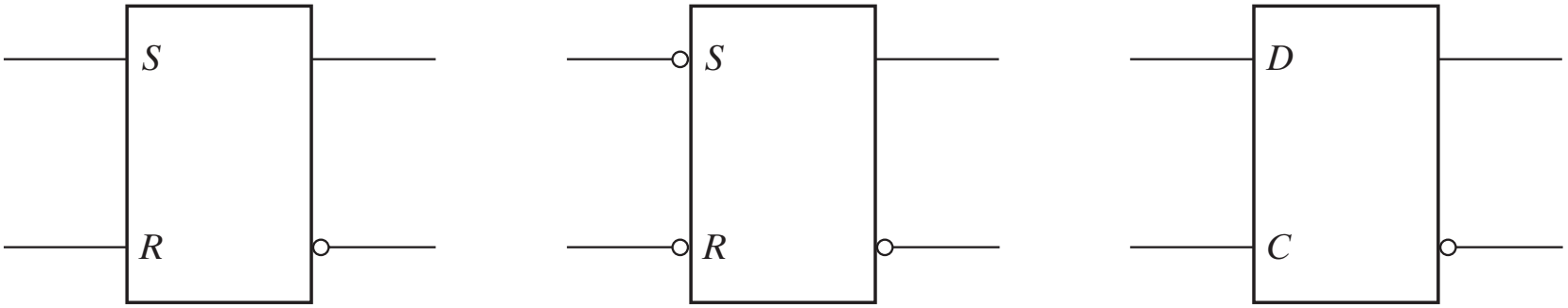


(a) Logic diagram

C	D	Next state of Q
0	X	No change
1	0	Q = 0; Reset state
1	1	Q = 1; Set state

(b) Function table

Fig. 5-6 D Latch

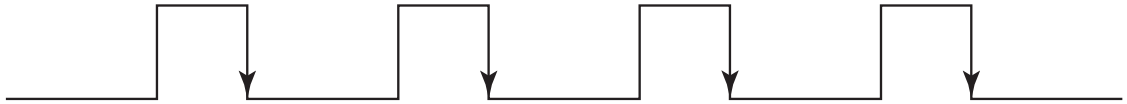


SR $\overline{S}\overline{R}$ *D*

Fig. 5-7 Graphic Symbols for Latches

(a) Response to positive level

(b) Positive-edge response



(c) Negative-edge response

Fig. 5-8 Clock Response in Latch and Flip-Flop

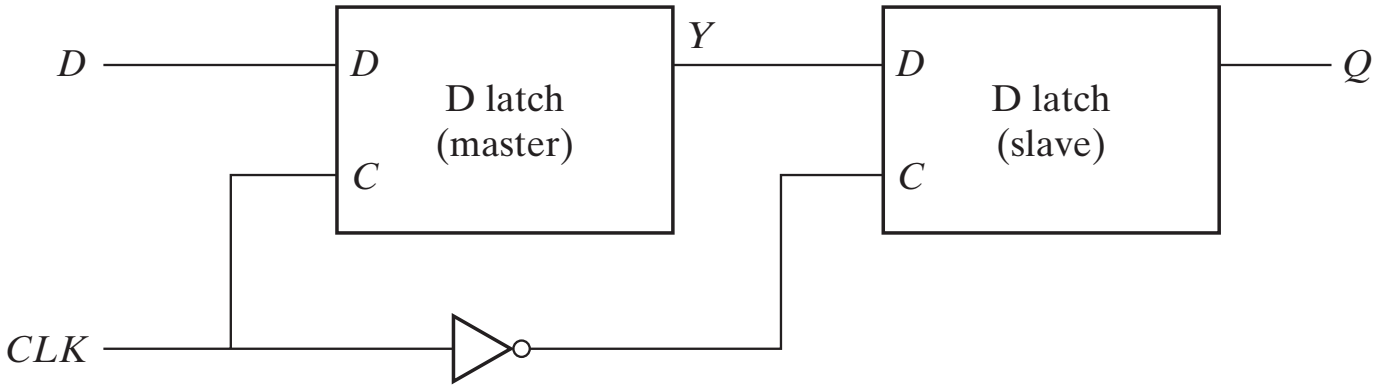


Fig. 5-9 Master-Slave *D* Flip-Flop

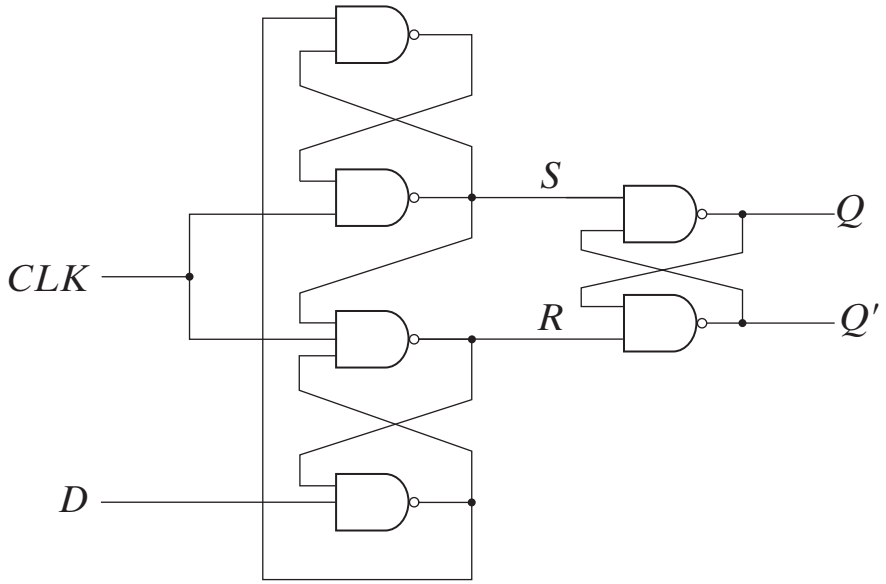
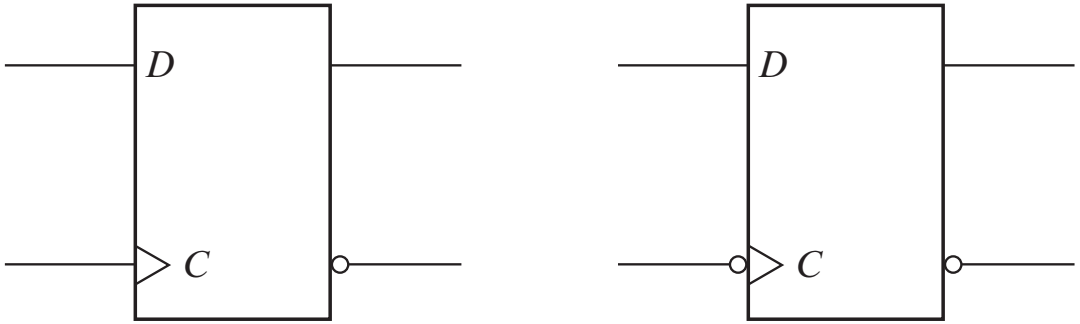
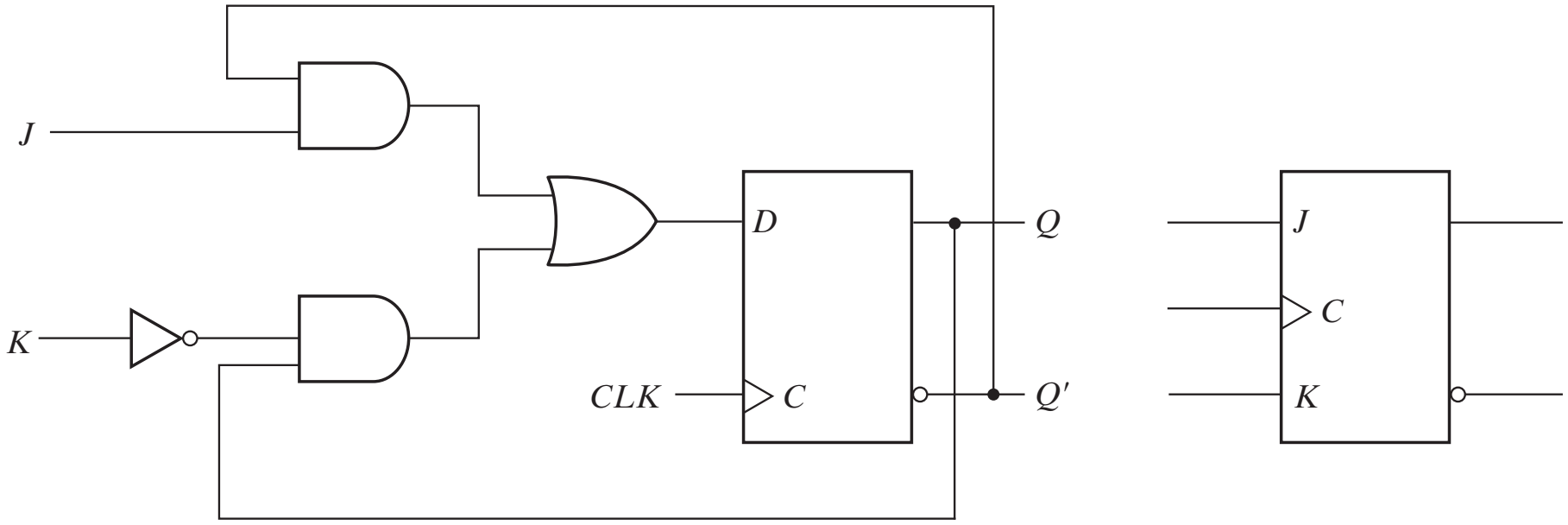


Fig. 5-10 *D*-Type Positive-Edge-Triggered Flip-Flop



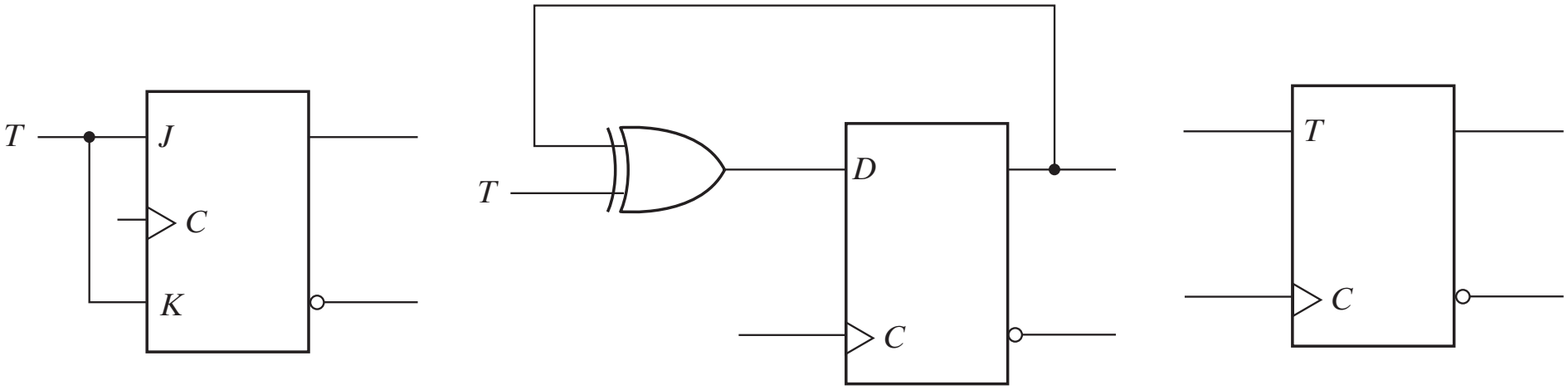
(a) Positive-edge (a) Negative-edge

Fig. 5-11 Graphic Symbol for Edge-Triggered *D* Flip-Flop



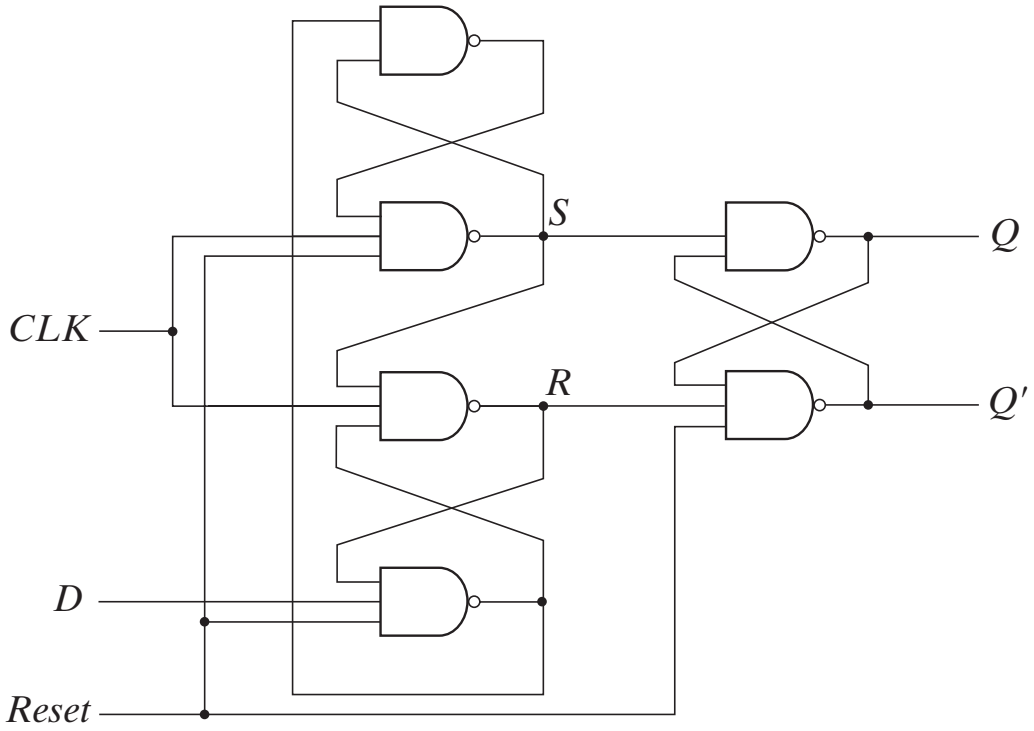
(a) Circuit diagram (b) Graphic symbol

Fig. 5-12 *JK* Flip-Flop

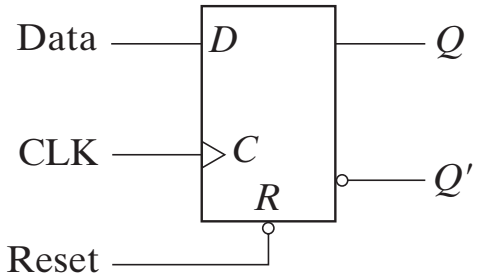


(a) From *JK* flip-flop (b) From *D* flip-flop (c) Graphic symbol

Fig. 5-13 T Flip-Flop



(a) Circuit diagram



(b) Graphic symbol

R	C	D	Q	Q′
0	X	X	0	1
1	↑	0	0	1
1	↑	1	1	0

(b) Function table

Fig. 5-14 *D* Flip-Flop with Asynchronous Reset

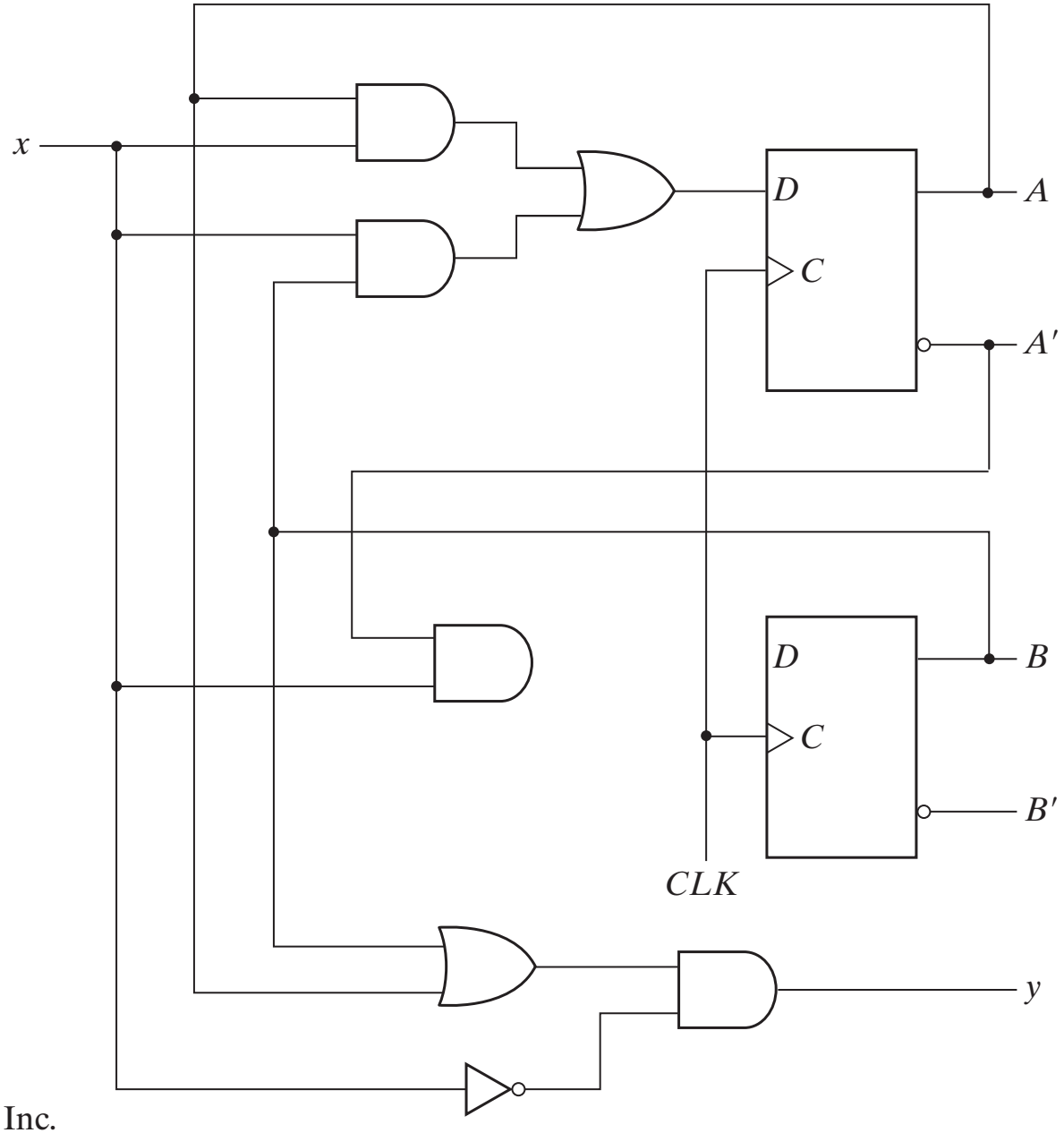


Fig. 5-15 Example of Sequential Circuit

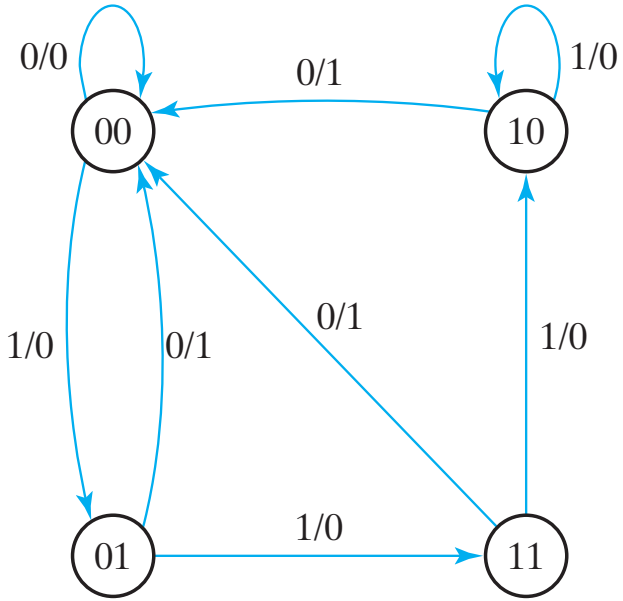
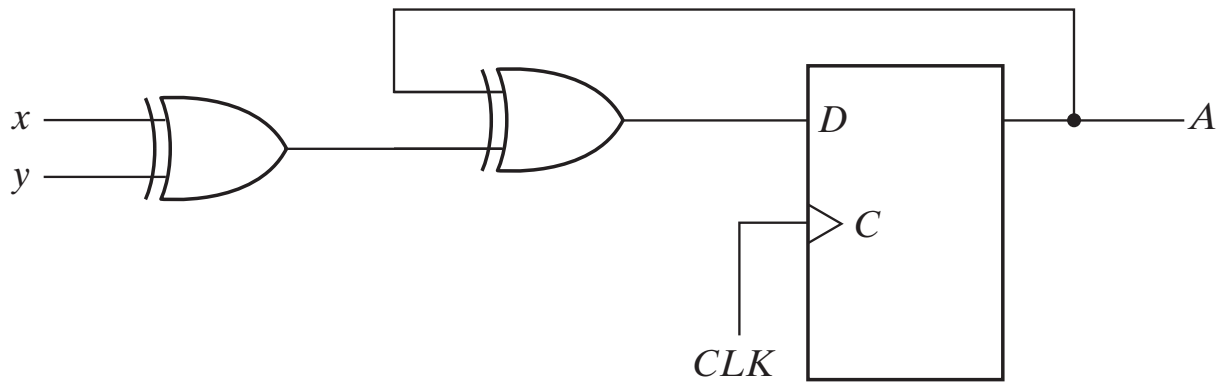


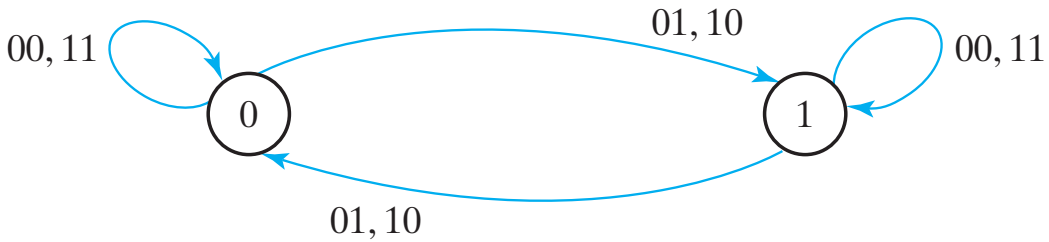
Fig. 5-16 State Diagram of the Circuit of Fig. 5-15



(a) Circuit diagram

Present state	Inputs		Next state
A	*x*	*y*	*A*
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

(b) State table



(c) State diagram

Fig. 5-17 Sequential Circuit with *D* Flip-Flop

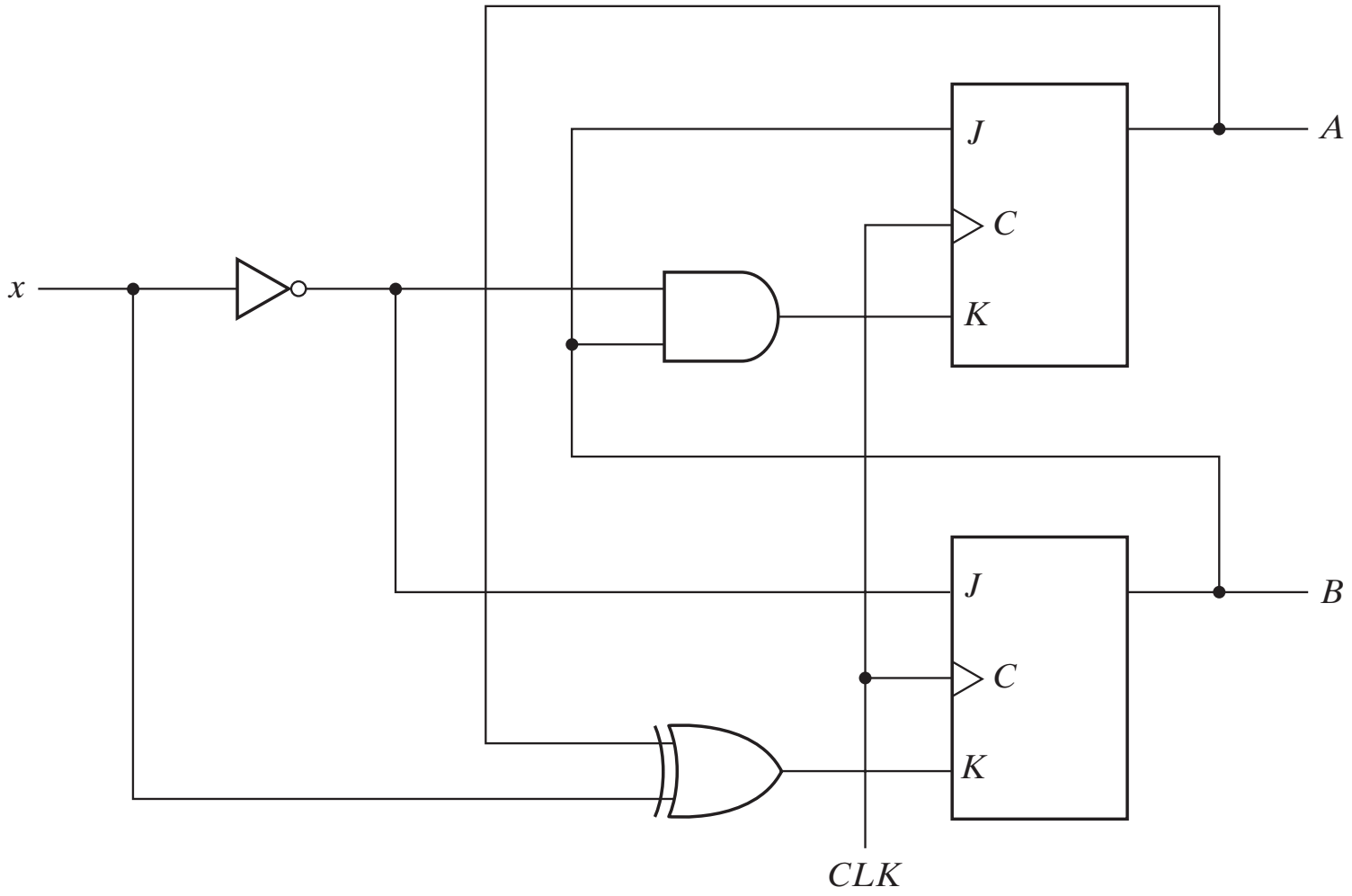


Fig. 5-18 Sequential Circuit with *JK* Flip-Flop

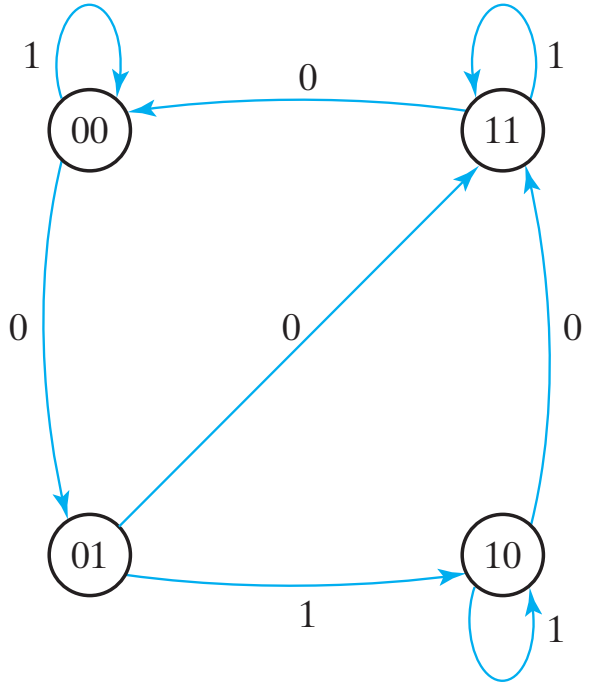
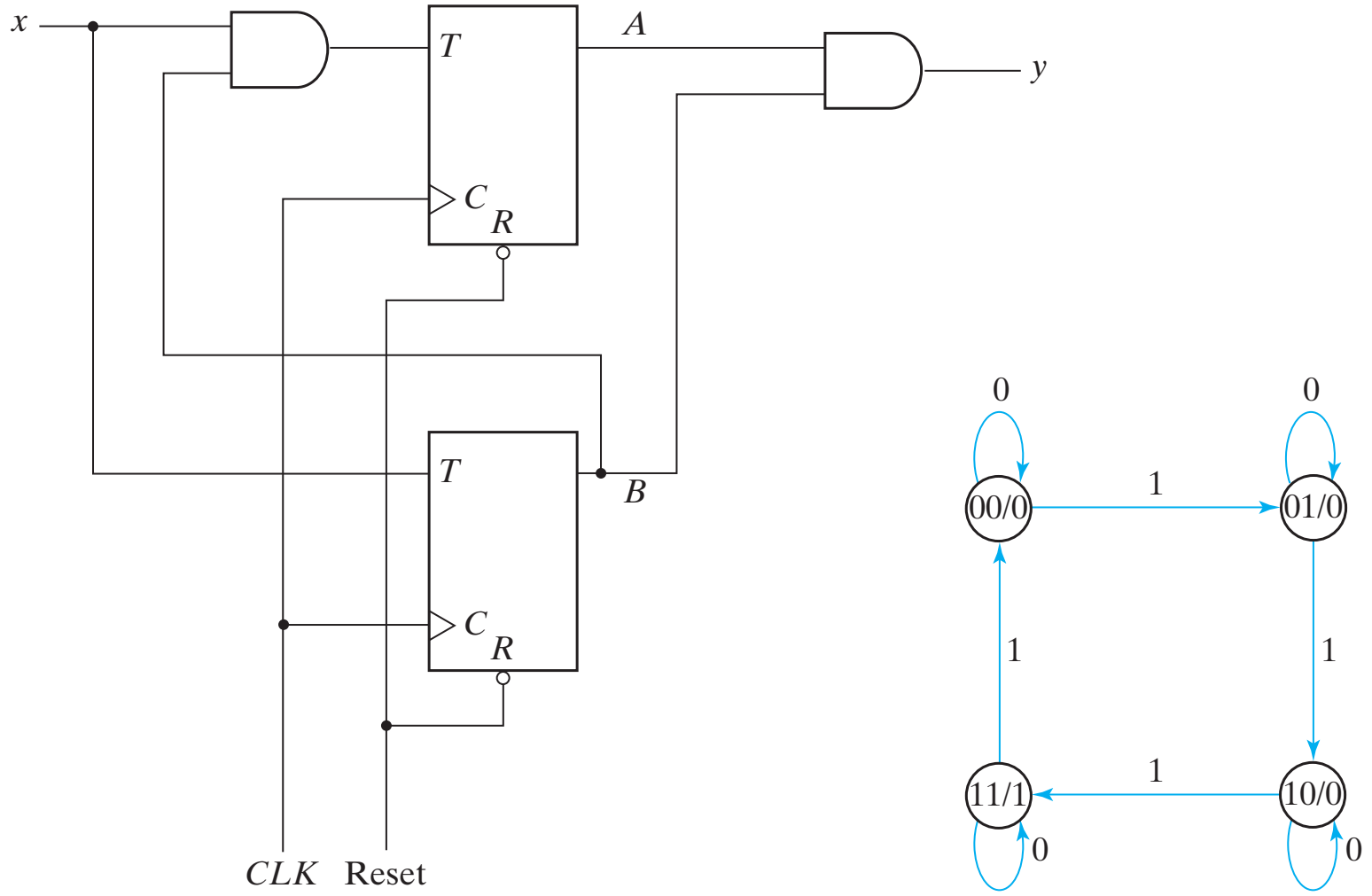


Fig. 5-19 State Diagram of the Circuit of Fig. 5-18



(a) Circuit diagram

(b) State diagram

Fig. 5-20 Sequential Circuit with *T* Flip-Flops

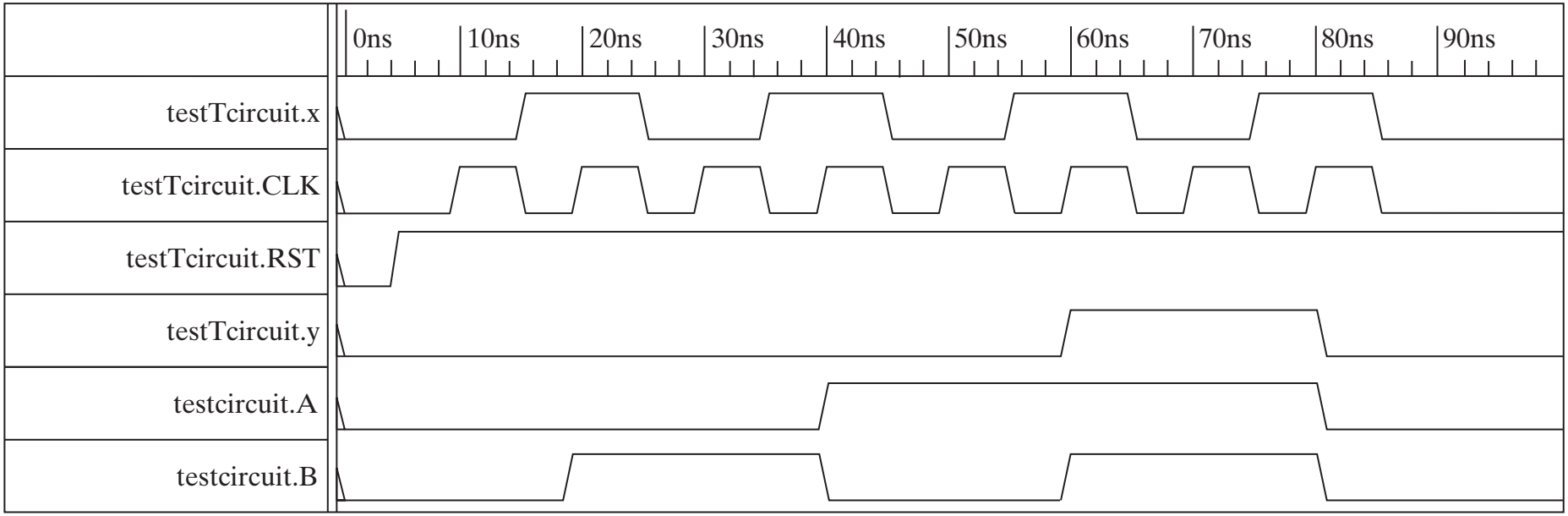


Fig. 5-21 Simulation Output of HDL Example 5-7

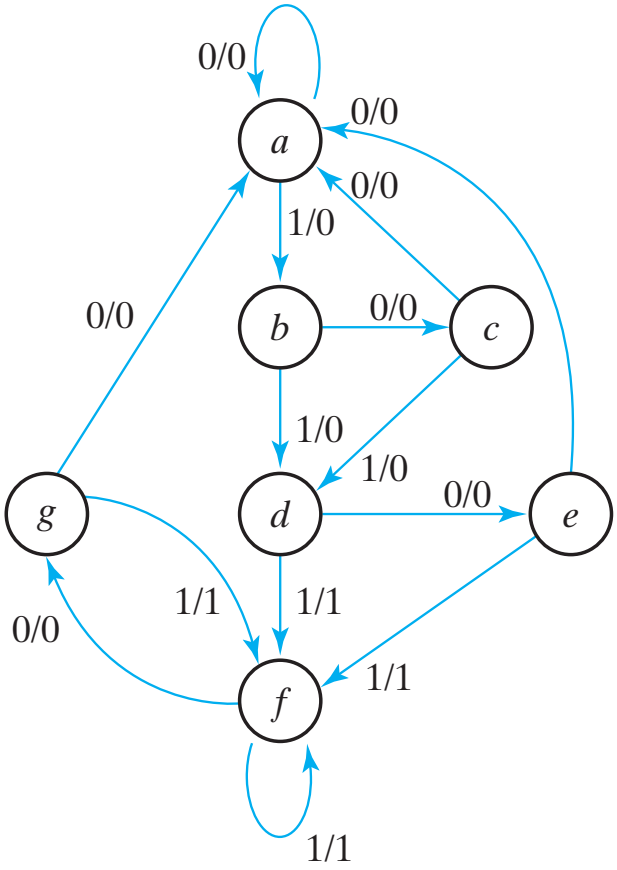


Fig. 5-22 State Diagram

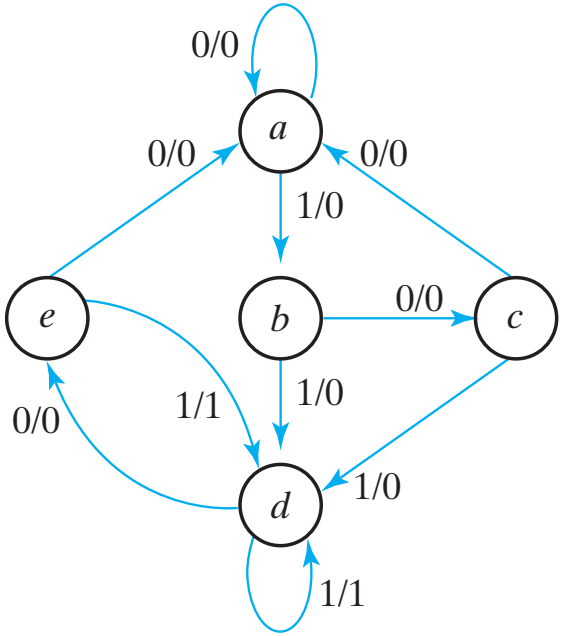


Fig. 5-23 Reduced State Diagram

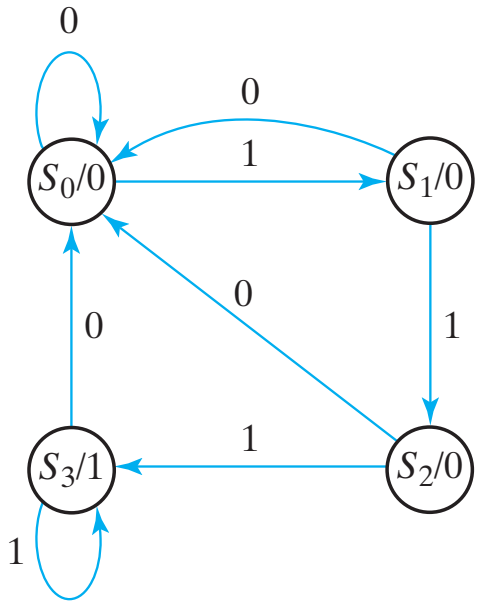
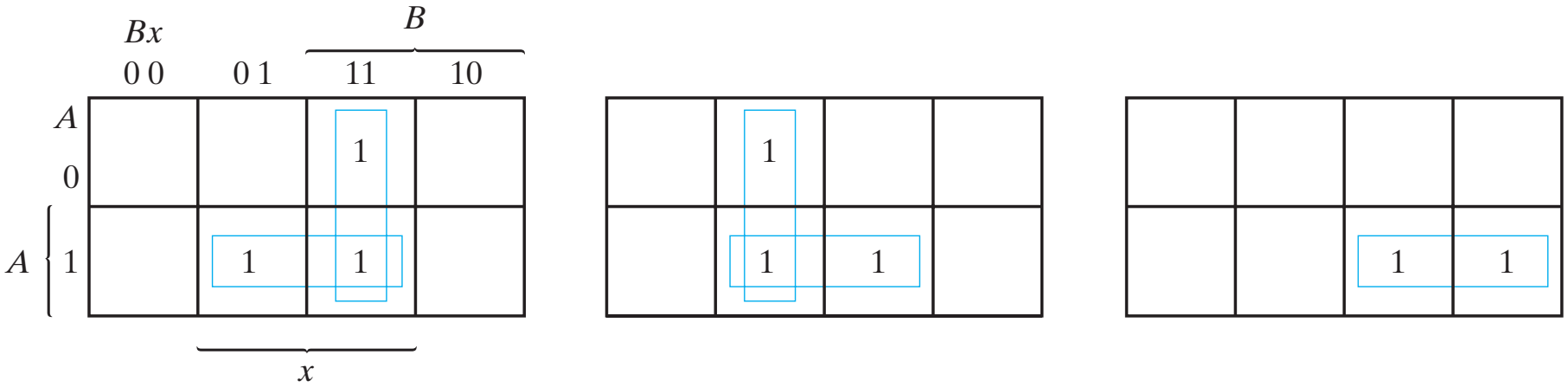


Fig. 5-24 State Diagram for Sequence Detector



$D_A = Ax + Bx$ $D_B = Ax + B'x$ $y = AB$

Fig. 5-25 Maps for Sequence Detector

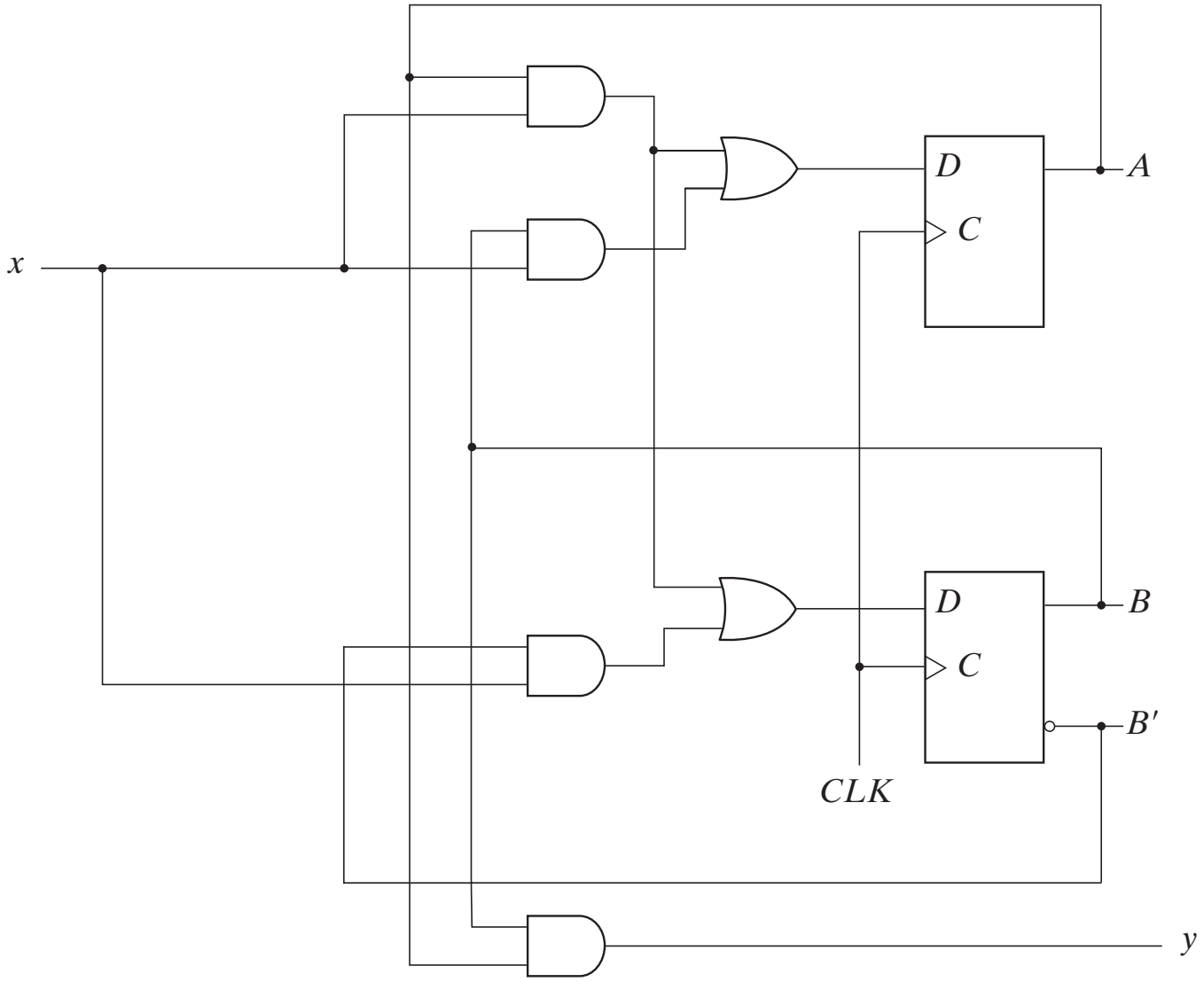


Fig. 5-26 Logic Diagram of Sequence Detector

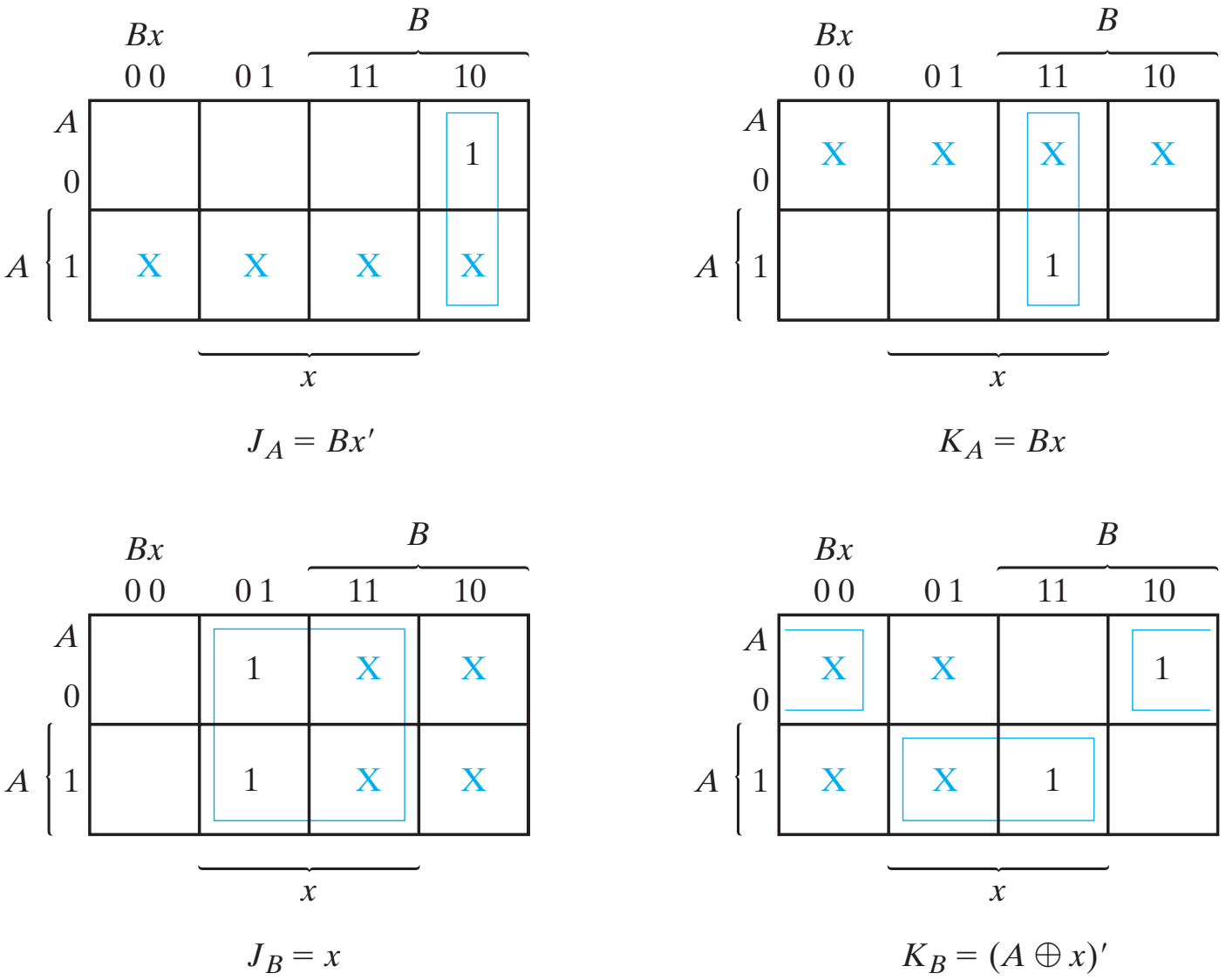


Fig. 5-27 Maps for J and K Input Equations

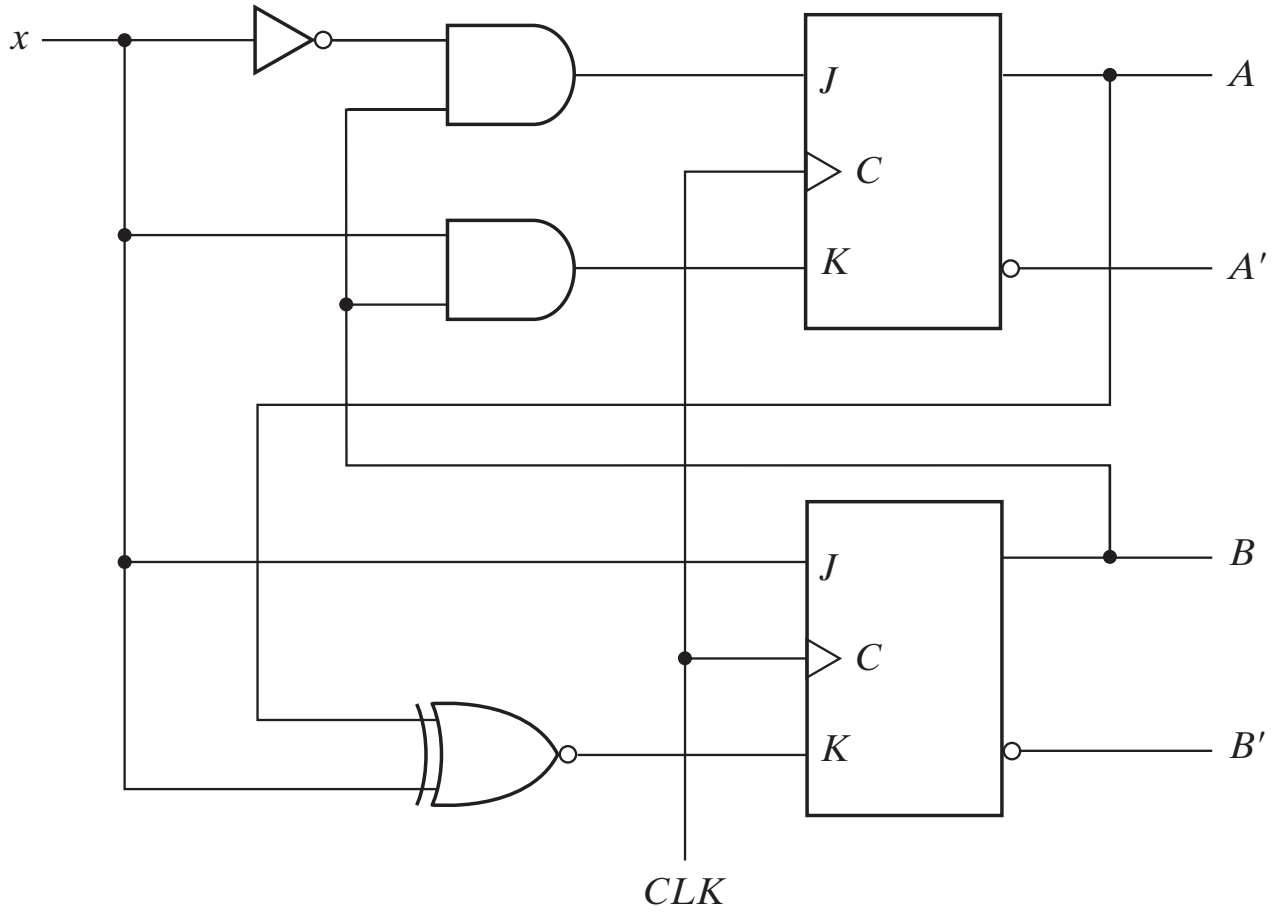


Fig. 5-28 Logic Diagram for Sequential Circuit with *JK* Flip-Flops

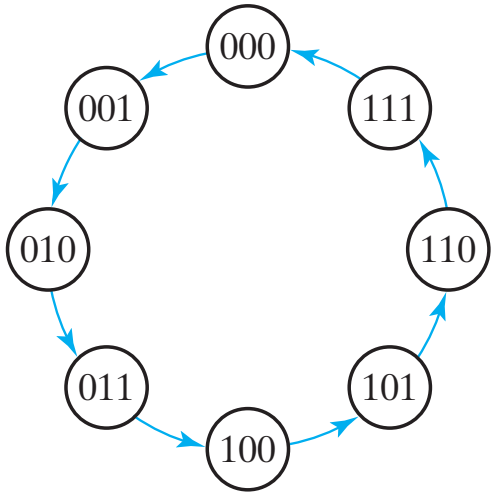


Fig. 5-29 State Diagram of 3-Bit Binary Counter

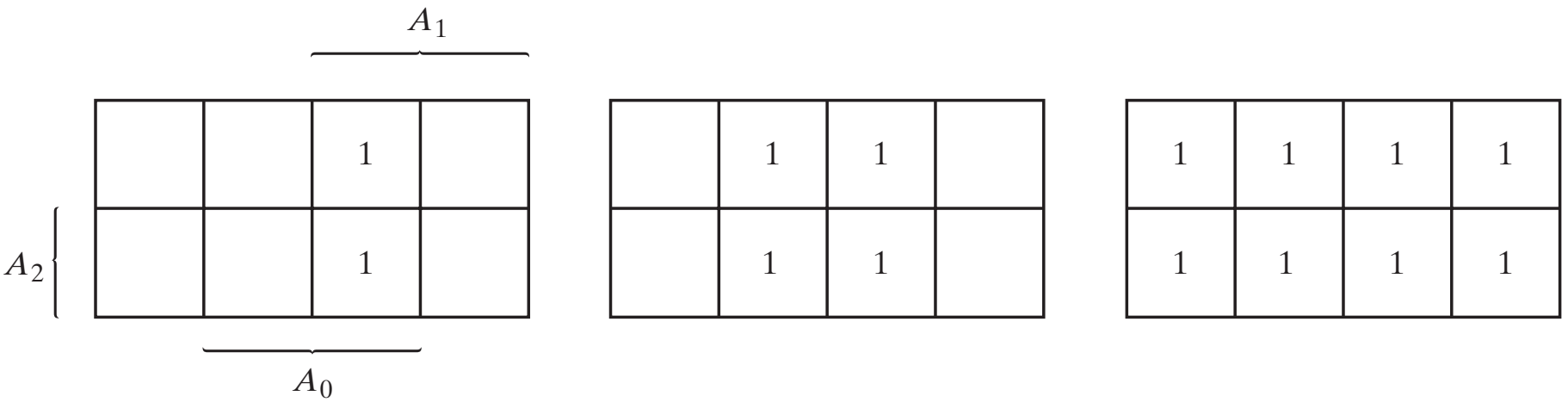


Fig. 5-30 Maps for 3-Bit Binary Counter

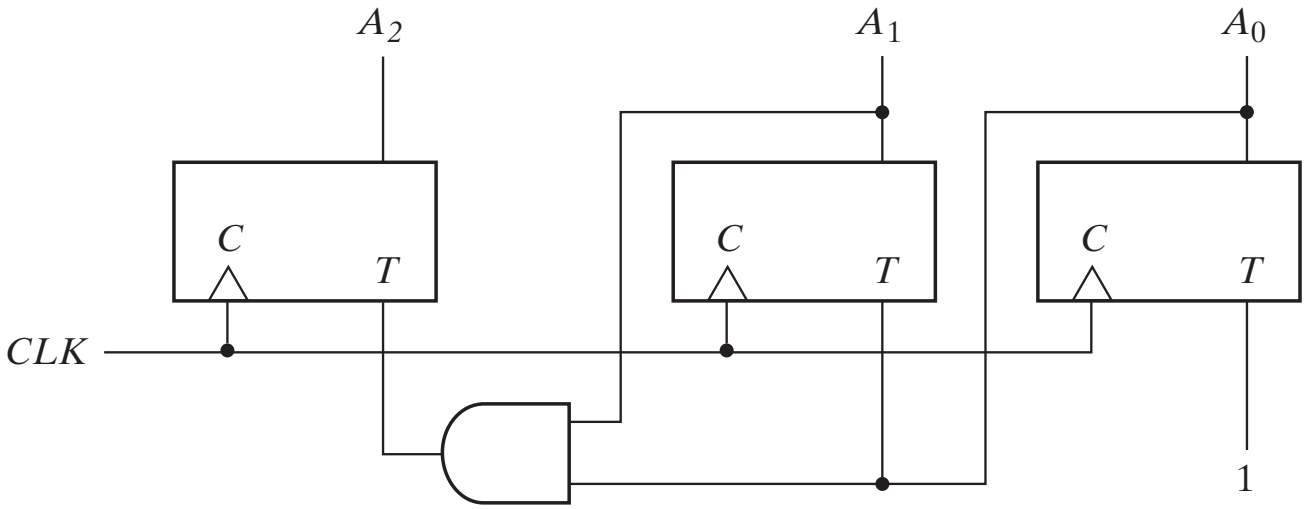


Fig. 5-31 Logic Diagram of 3-Bit Binary Counter

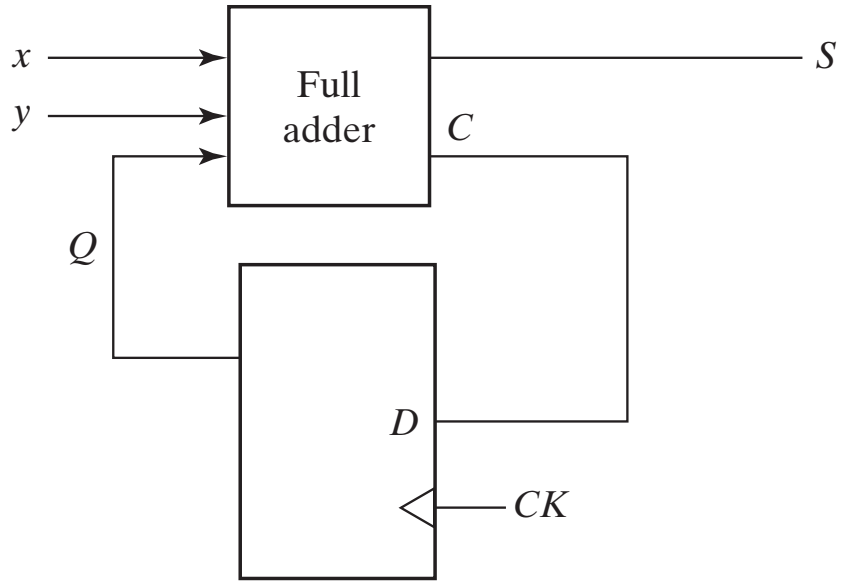


Fig. P5-7

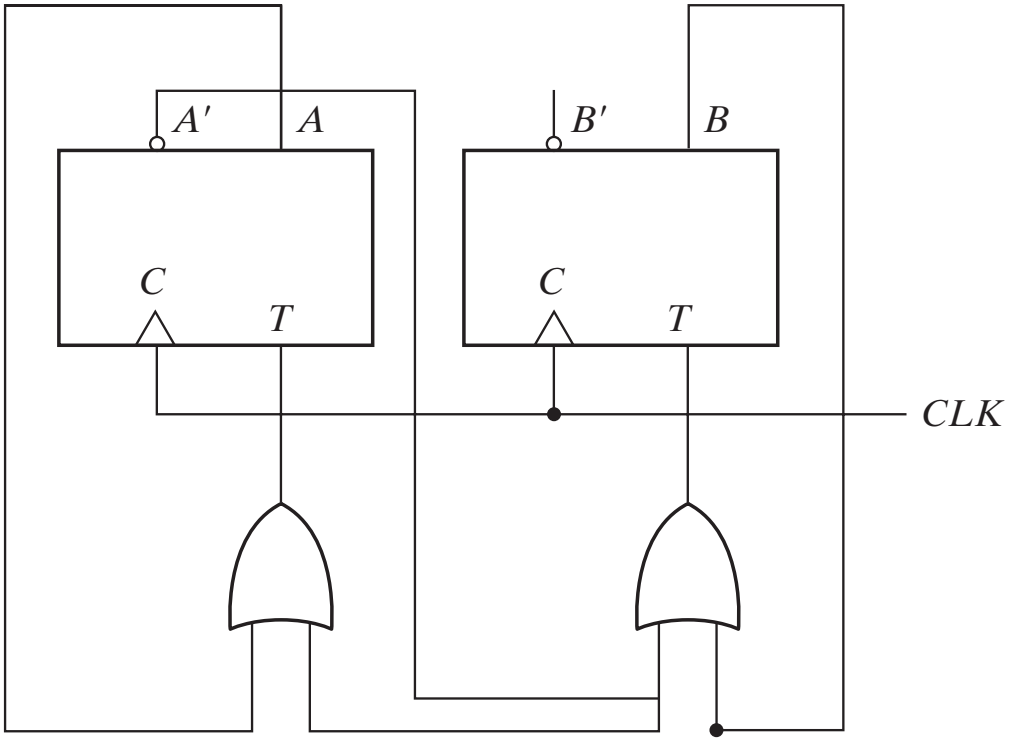


Fig. P5-8

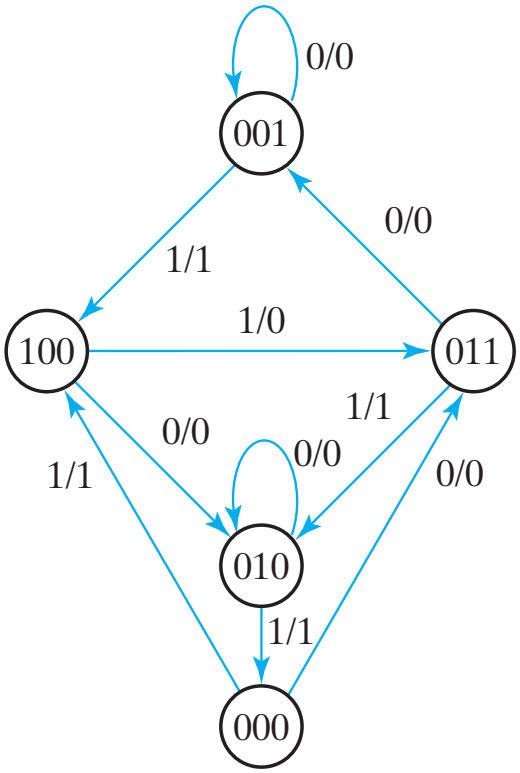


Fig. P5-19