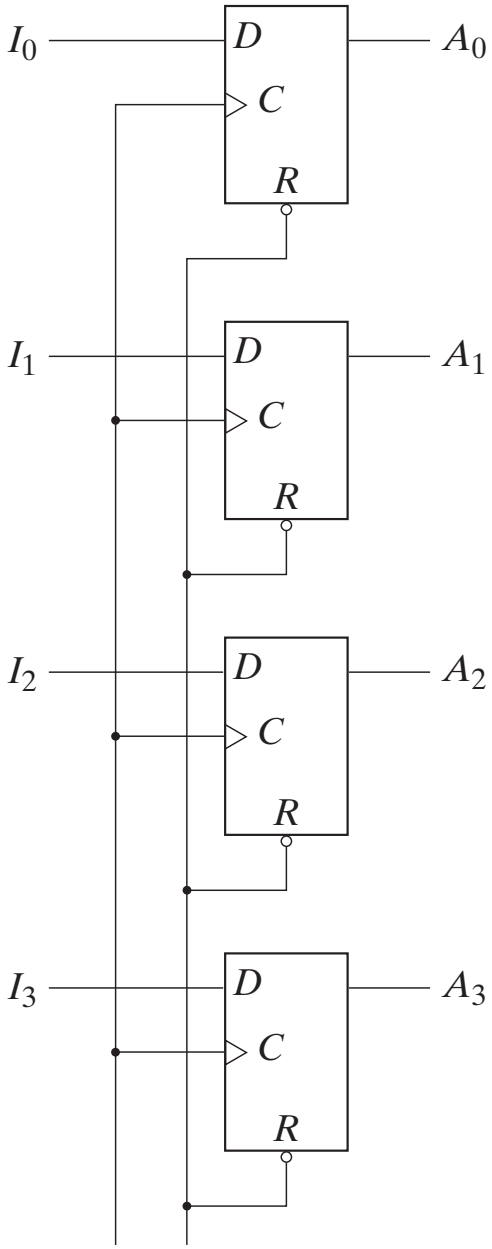

Fig. 6-1 4-Bit Register

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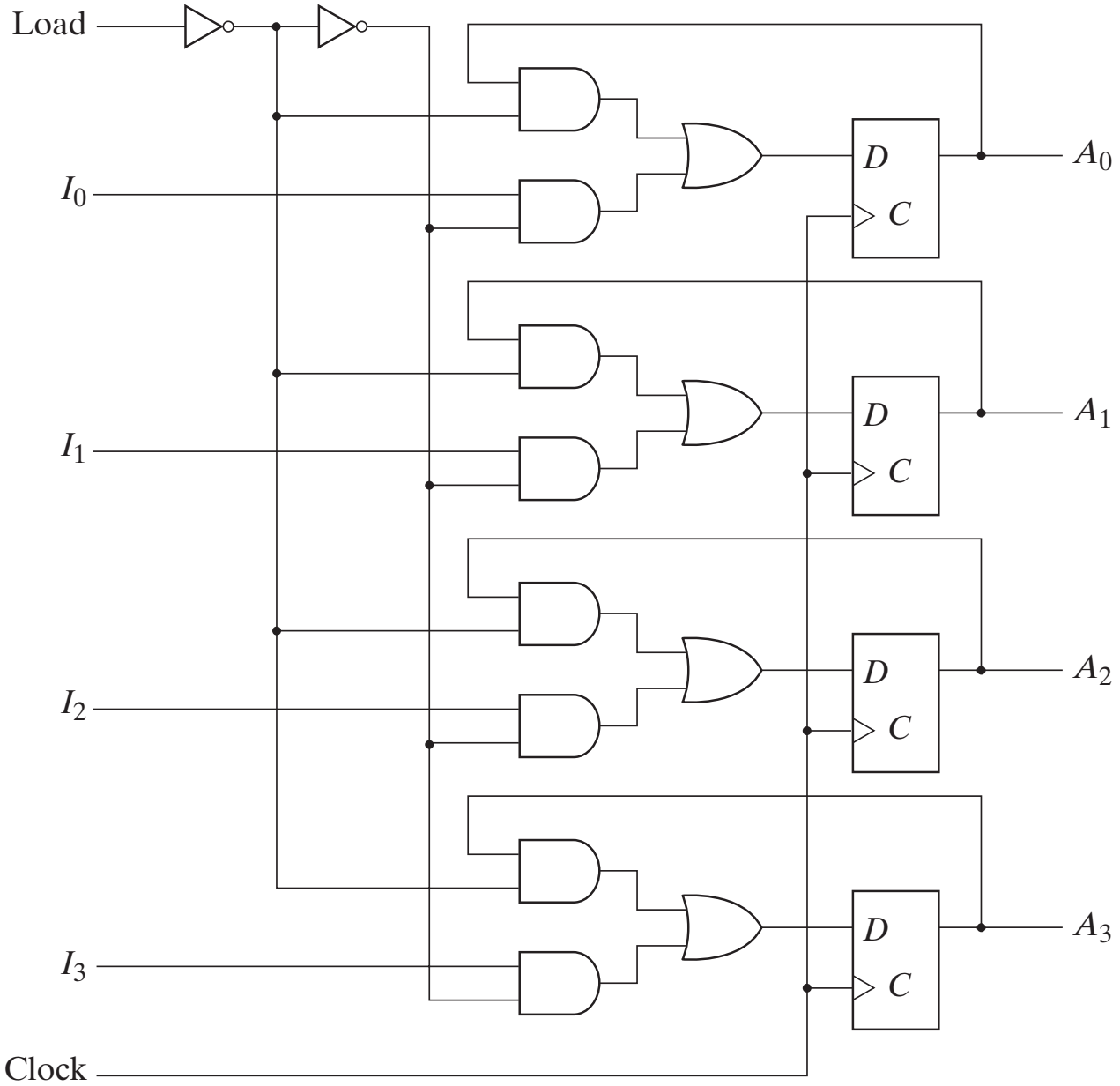

Fig. 6-2 4-Bit Register with Parallel Load

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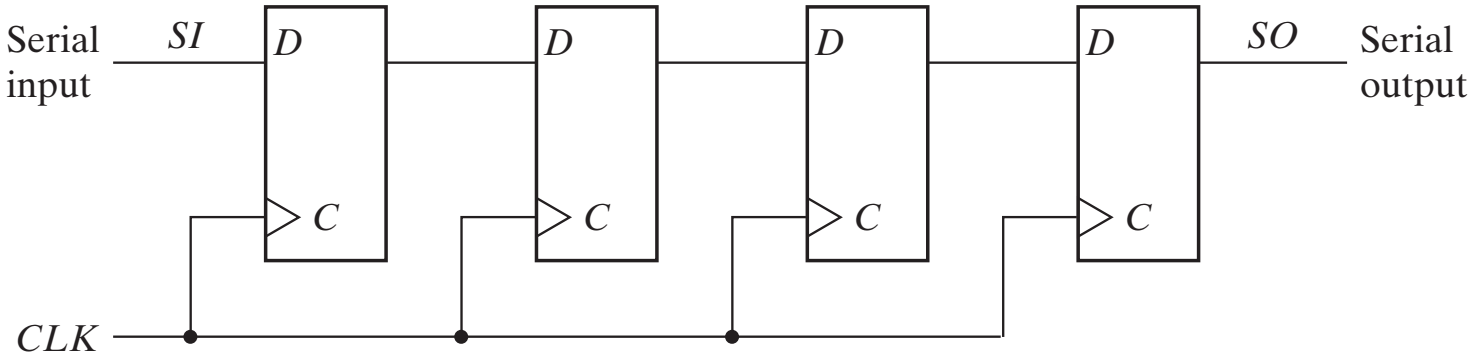

Fig. 6-3 4-Bit Shift Register

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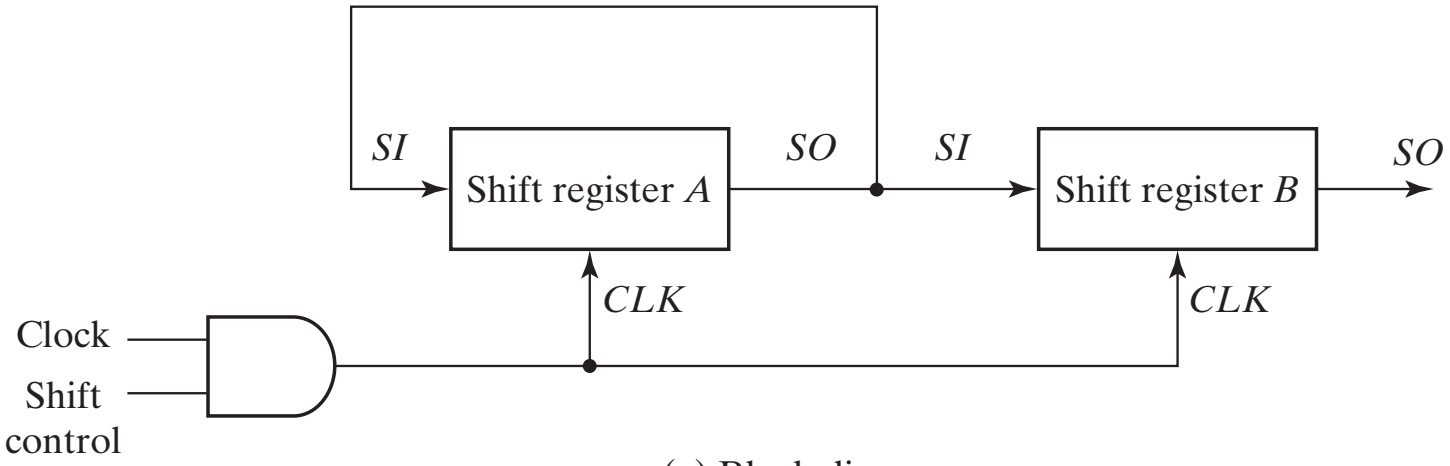
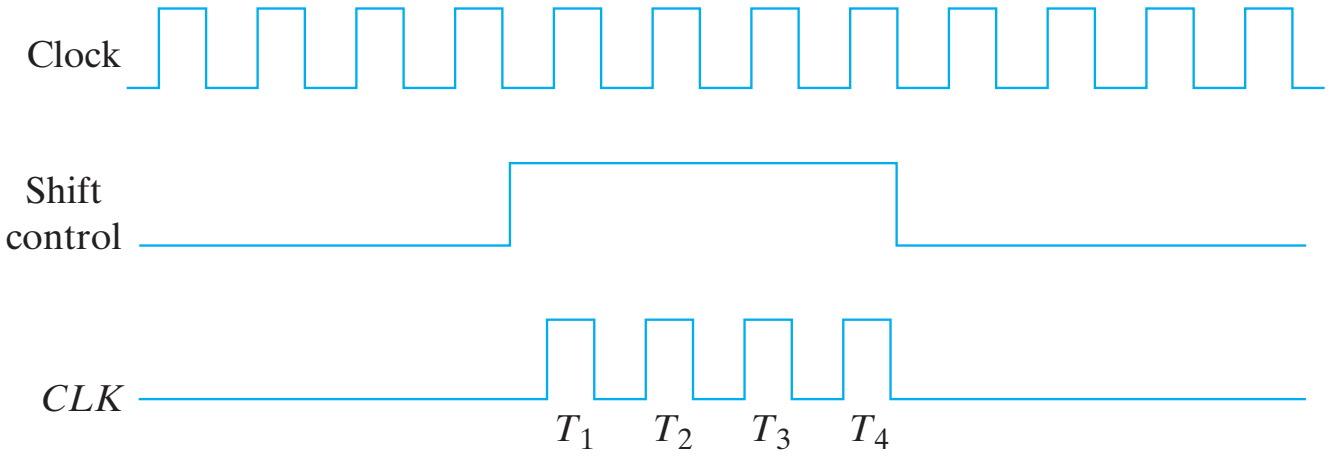


(a) Block diagram



(b) Timing diagram

Fig. 6-4 Serial Transfer from Register *A* to register *B*

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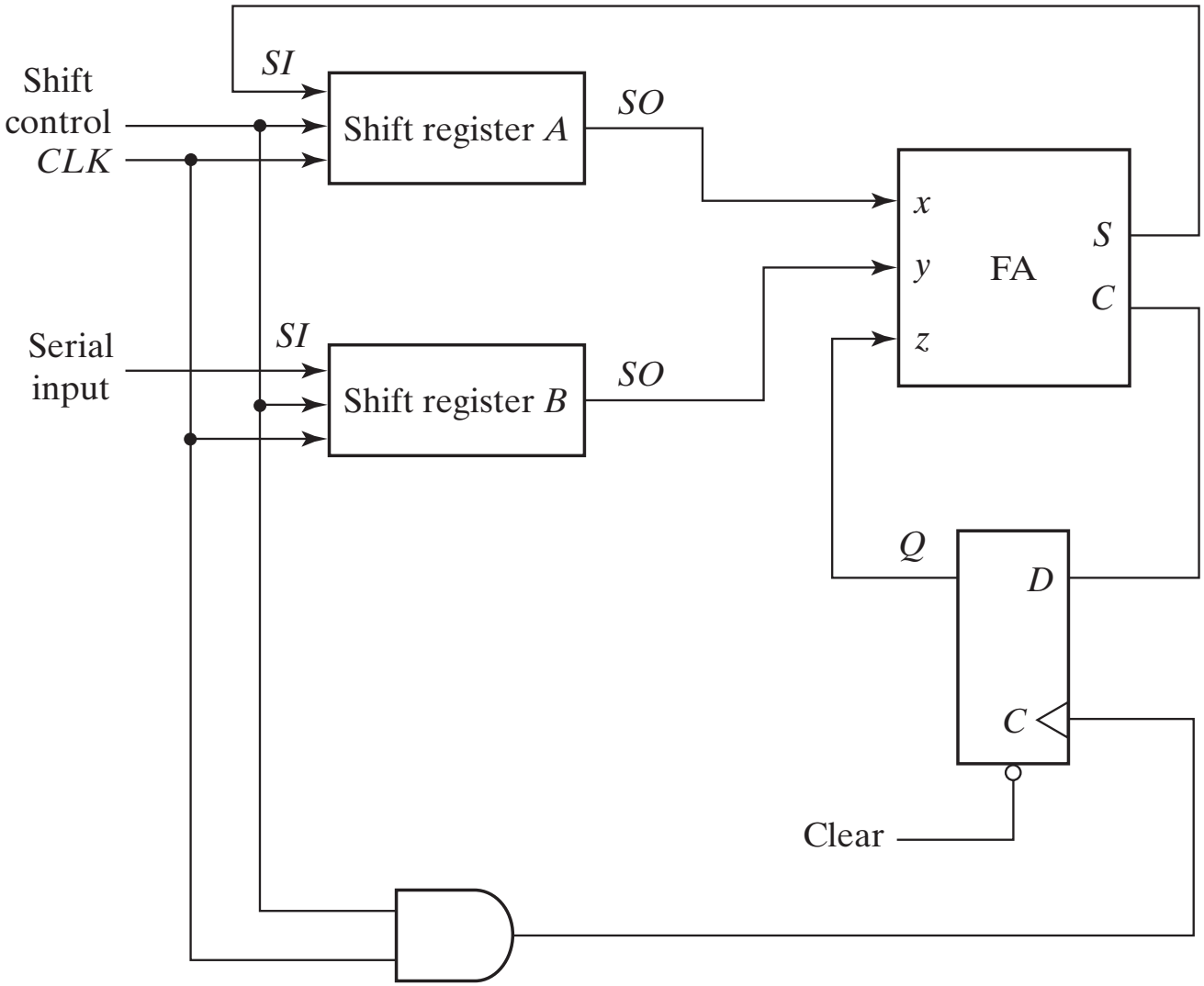

Fig. 6-5 Serial Adder

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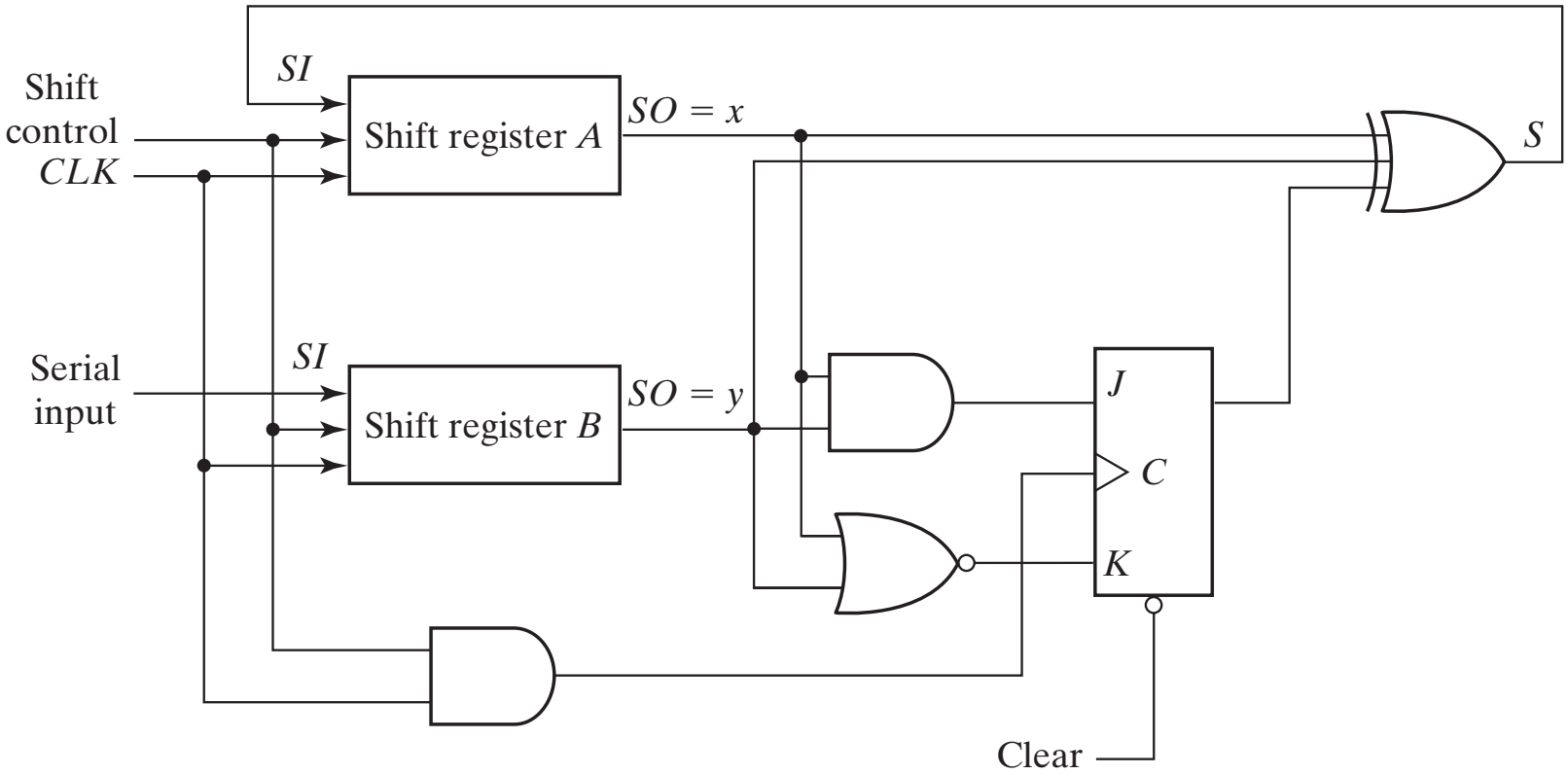

Fig. 6-6 Second form of Serial Adder

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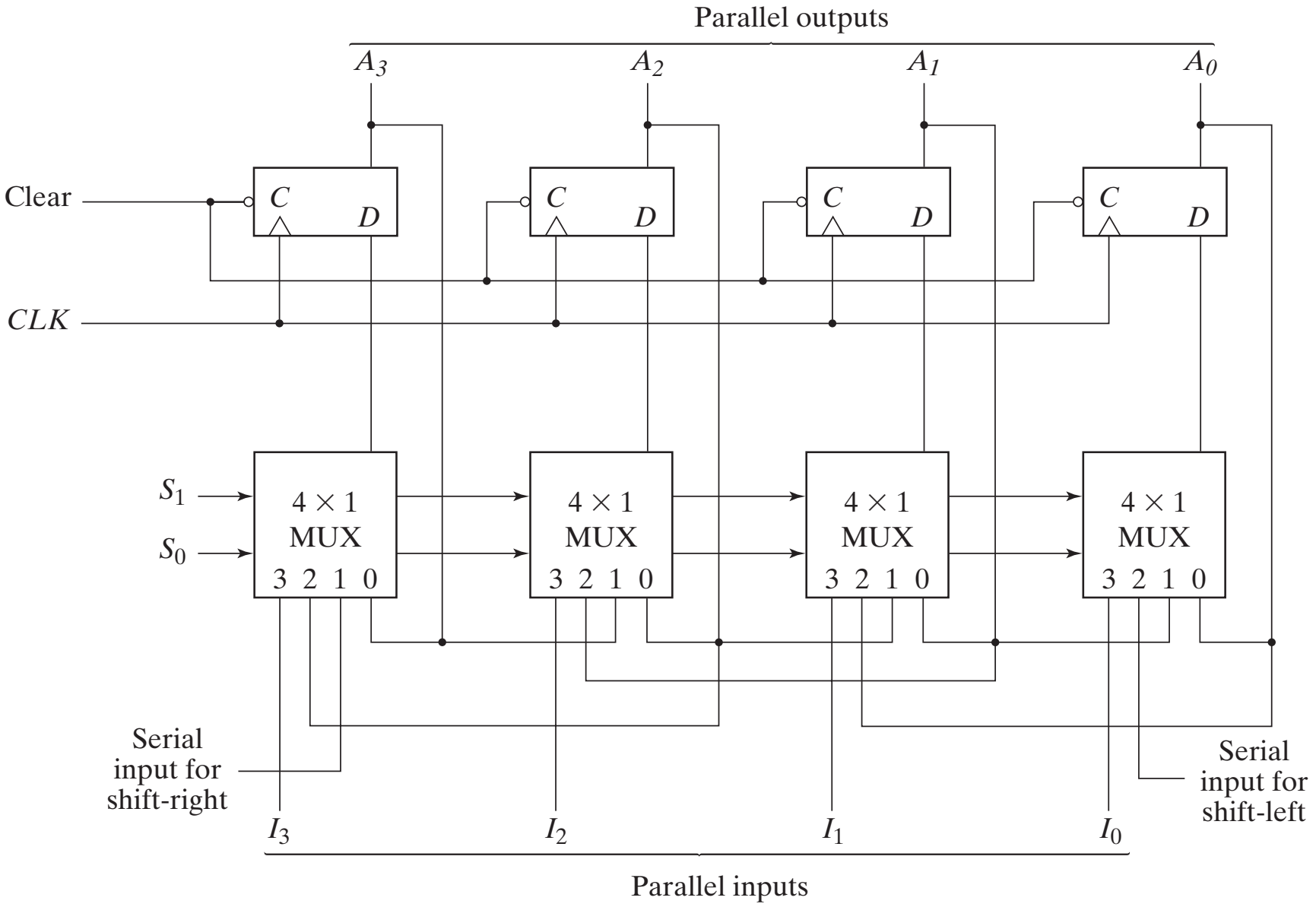

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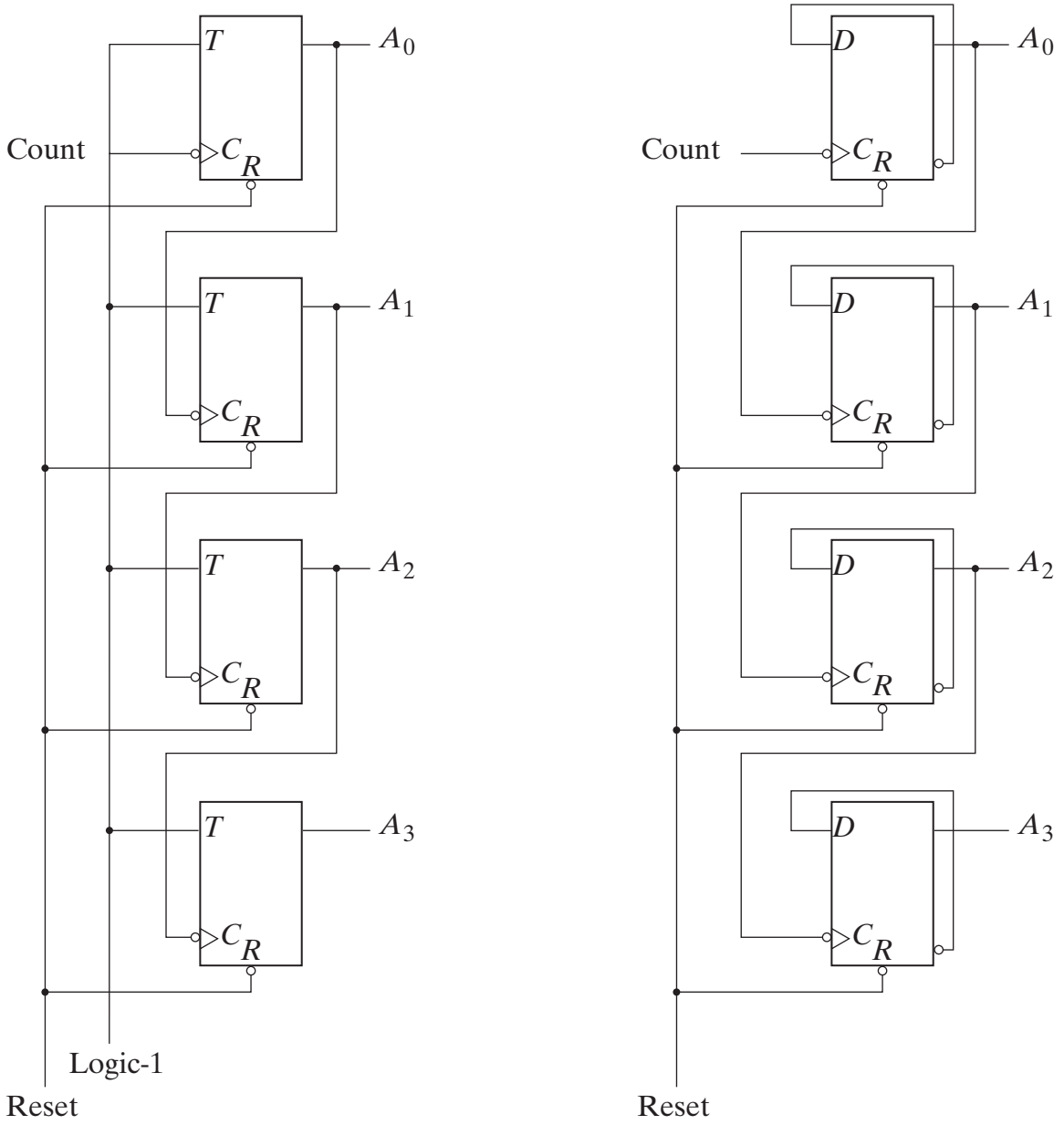
Fig. 6-7 4-Bit Universal Shift Register



(a) With T flip-flops

(b) With D flip-flops

Fig. 6-8 4-Bit Binary Ripple Counter

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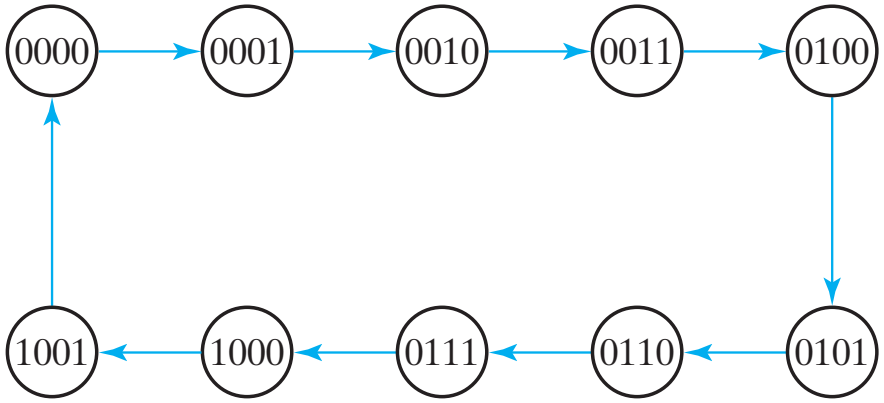

Fig. 6-9 State Diagram of a Decimal BCD-Counter

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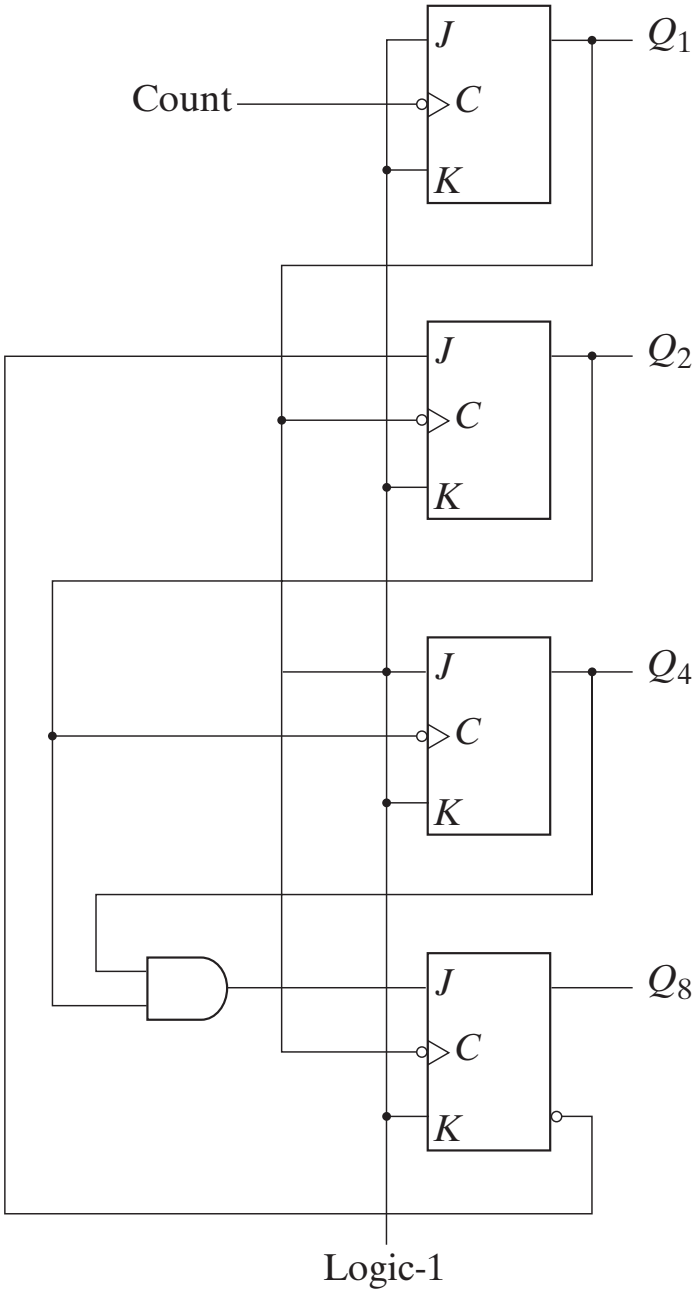

Fig. 6-10 BCD Ripple Counter

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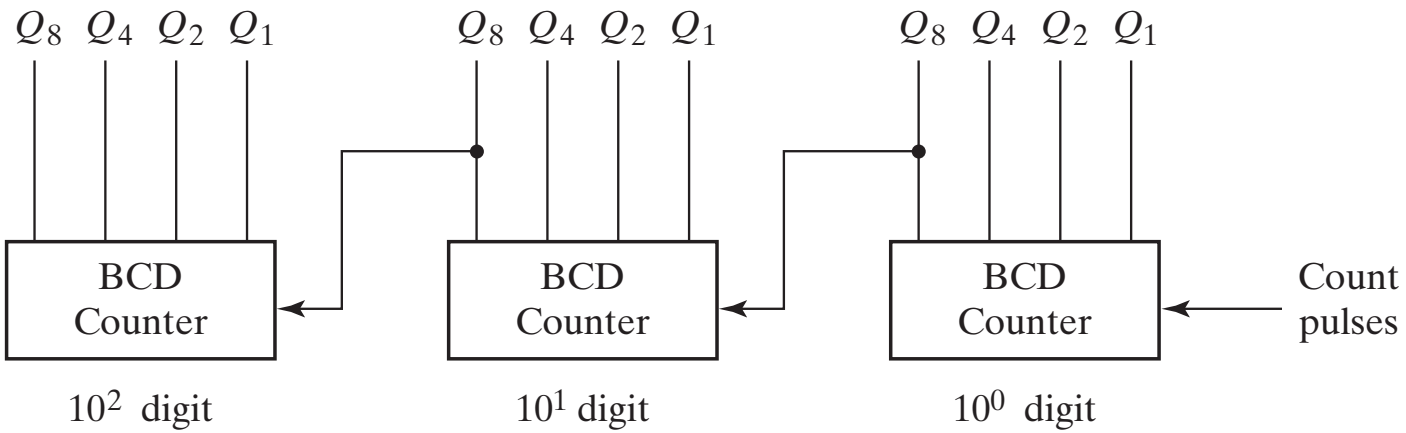

Fig. 6-11 Block Diagram of a Three-Decade Decimal BCD Counter

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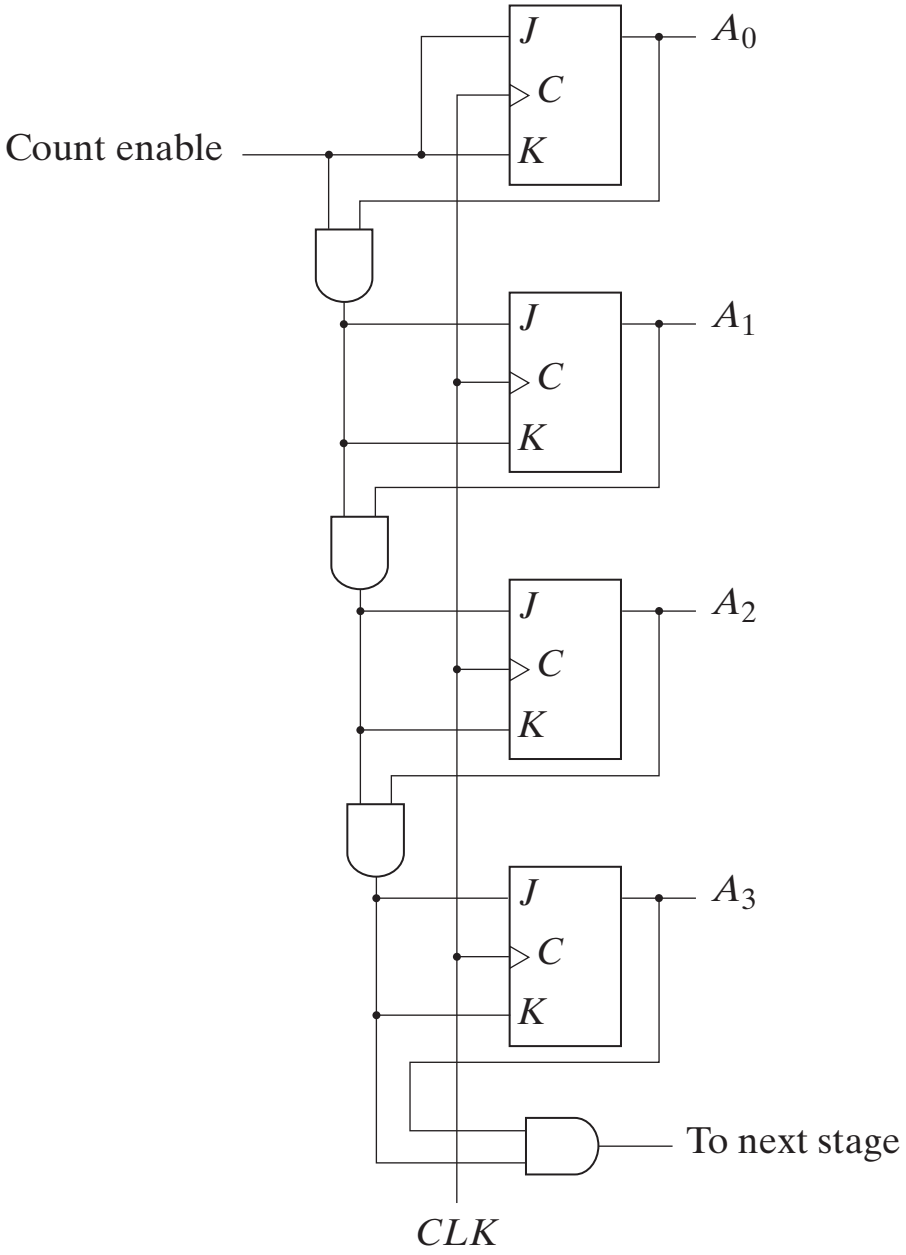

Fig. 6-12 4-Bit Synchronous Binary Counter

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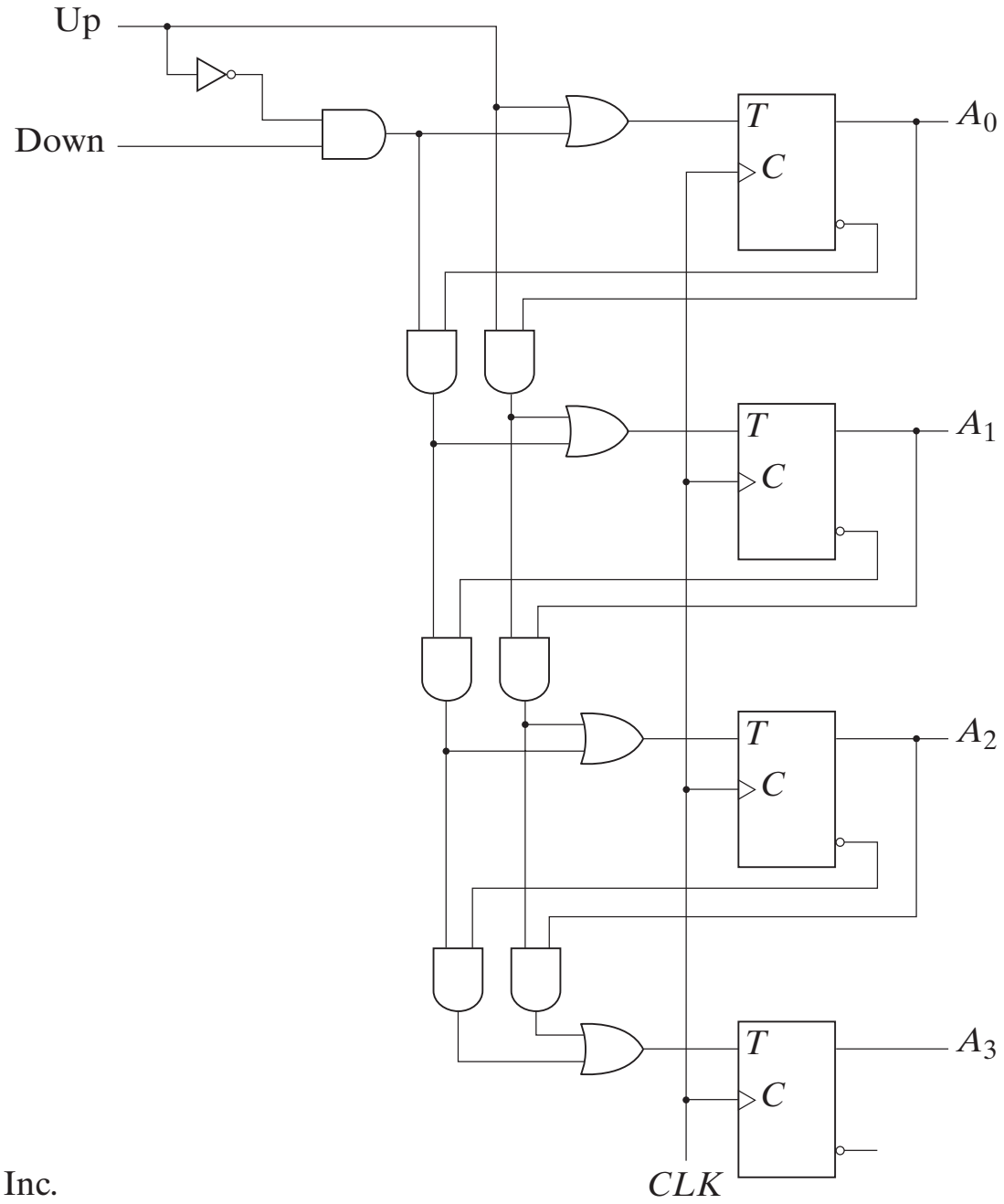

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Fig. 6-13 4-Bit Up-Down Binary Counter

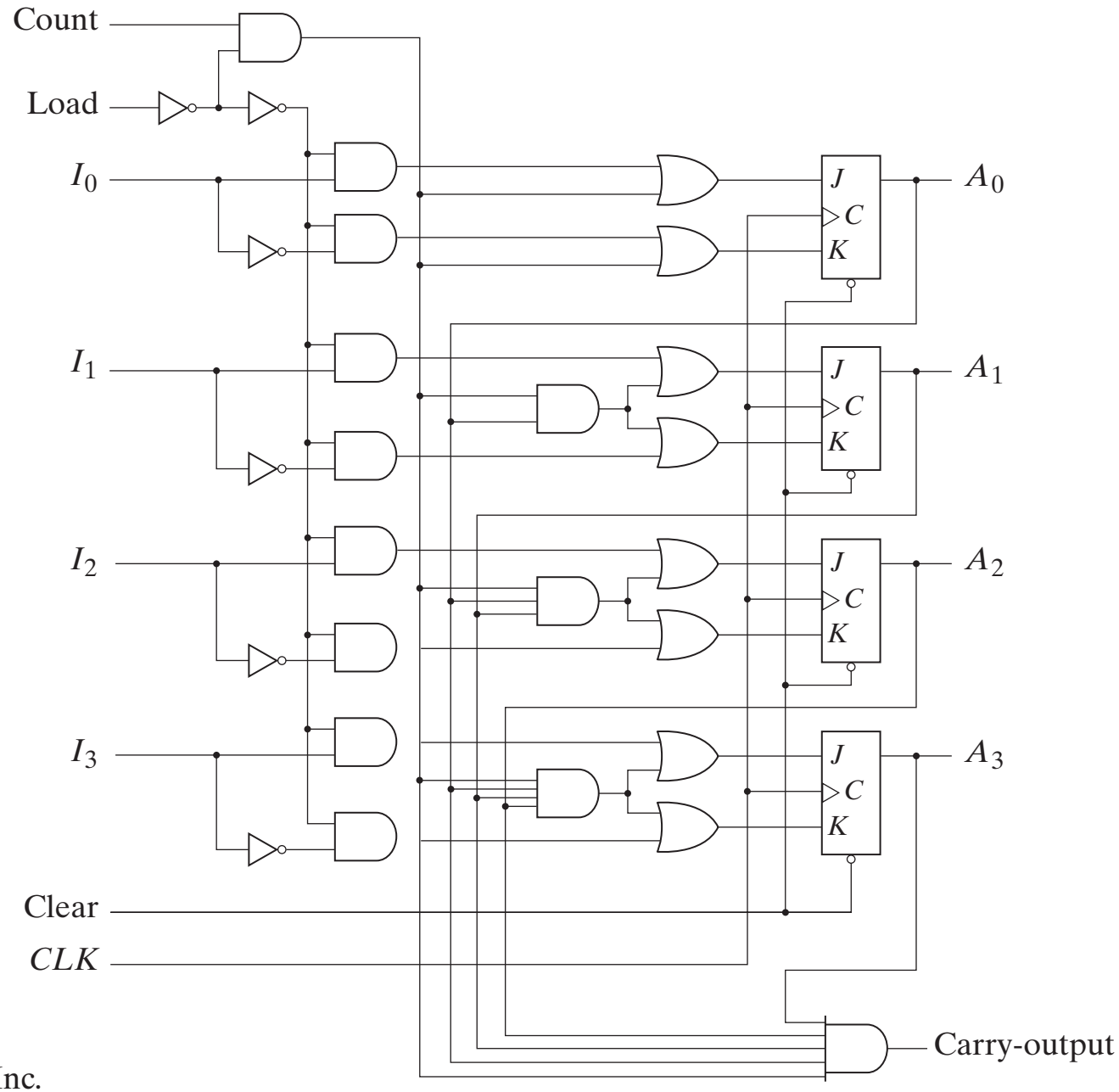

Fig. 6-14 4-Bit Binary Counter with Parallel Load

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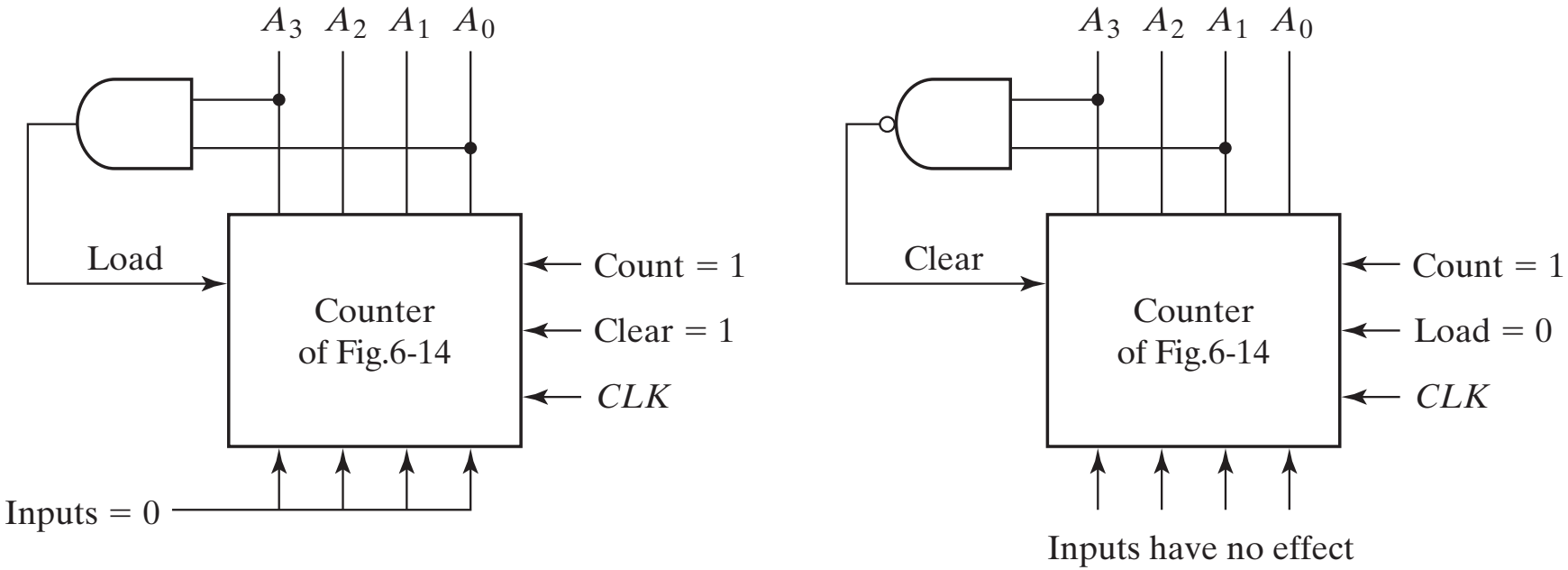

Fig. 6-15 Two ways to Achieve a BCD Counter Using a Counter with Parallel Load

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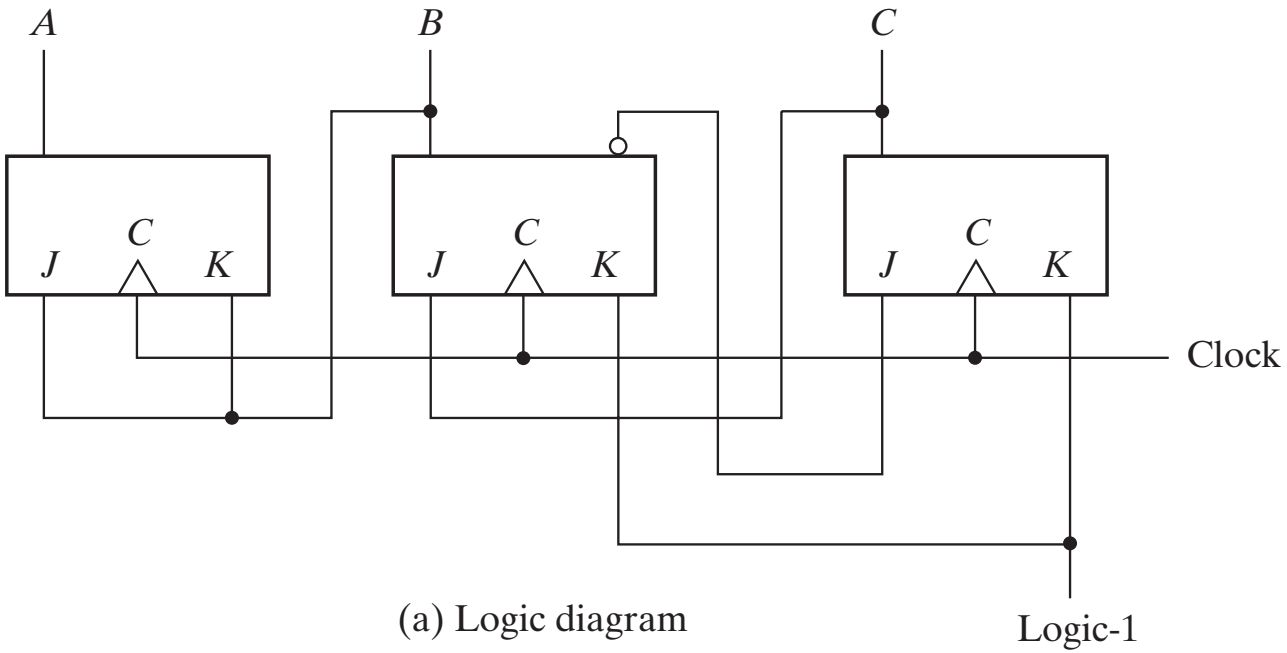
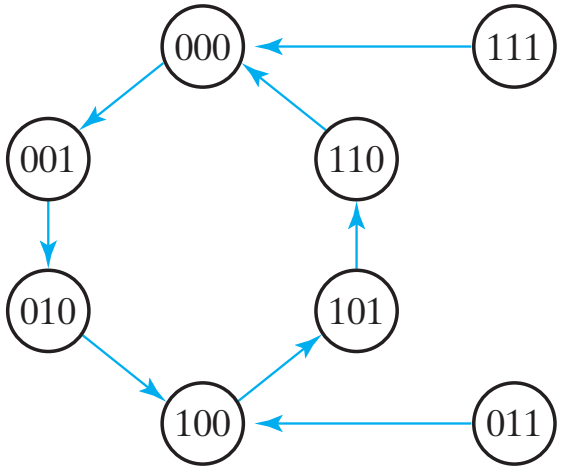


(a) Logic diagram



(b) State diagram

Fig. 6-16 Counter with Unused States

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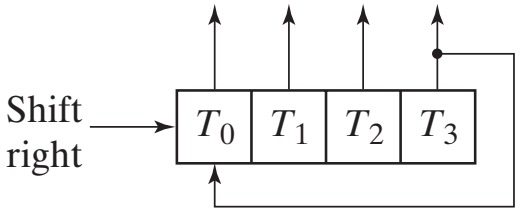
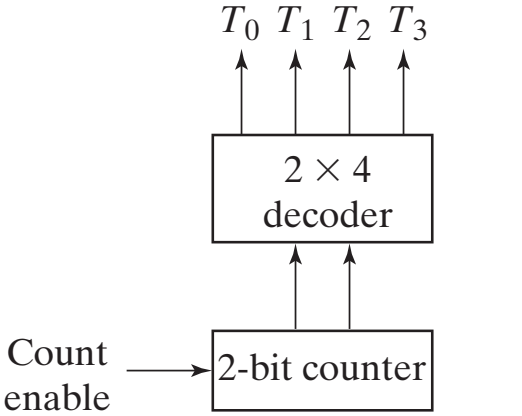
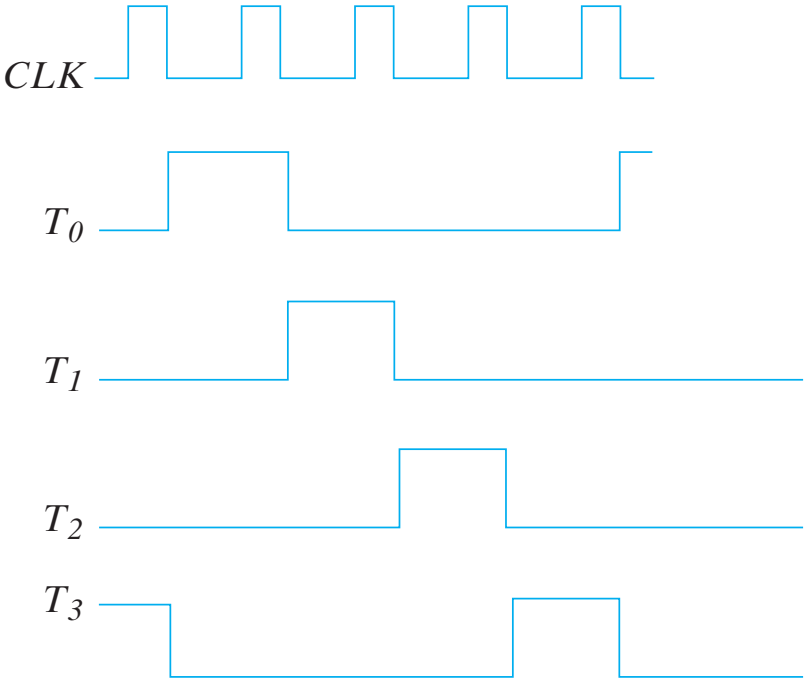


(a) Ring-counter (initial value = 1000)



(b) Counter and decoder



(c) Sequence of four timing signals

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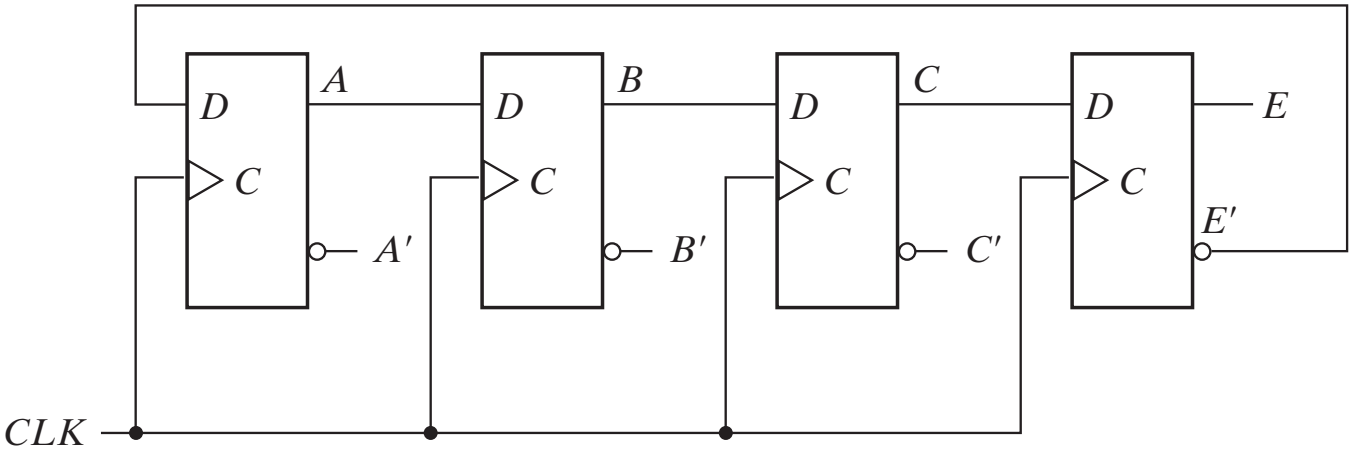
Fig. 6-17 Generation of Timing Signals



(a) Four-stage switch-tail ring counter

Sequence number	Flip-flop outputs				AND gate required for output
	A	*B*	*C*	*E*	
1	0	0	0	0	$A'E'$
2	1	0	0	0	AB'
3	1	1	0	0	BC'
4	1	1	1	0	CE'
5	1	1	1	1	AE
6	0	1	1	1	$A'B$
7	0	0	1	1	$B'C$
8	0	0	0	1	$C'E$

(b) Count sequence and required decoding

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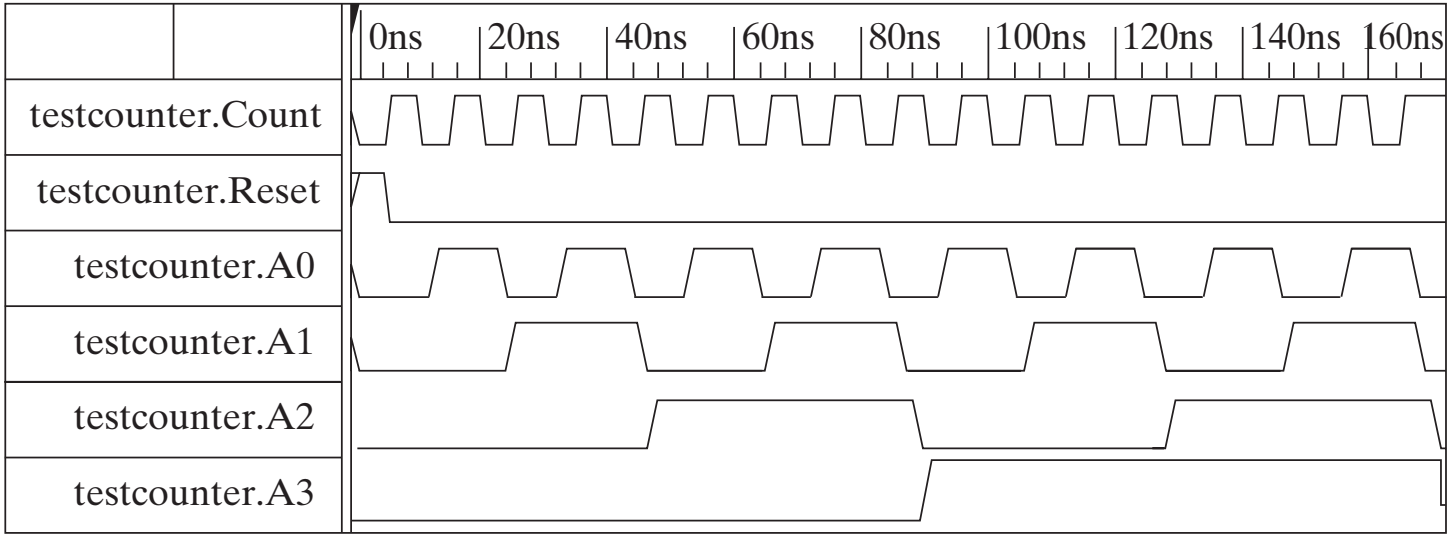
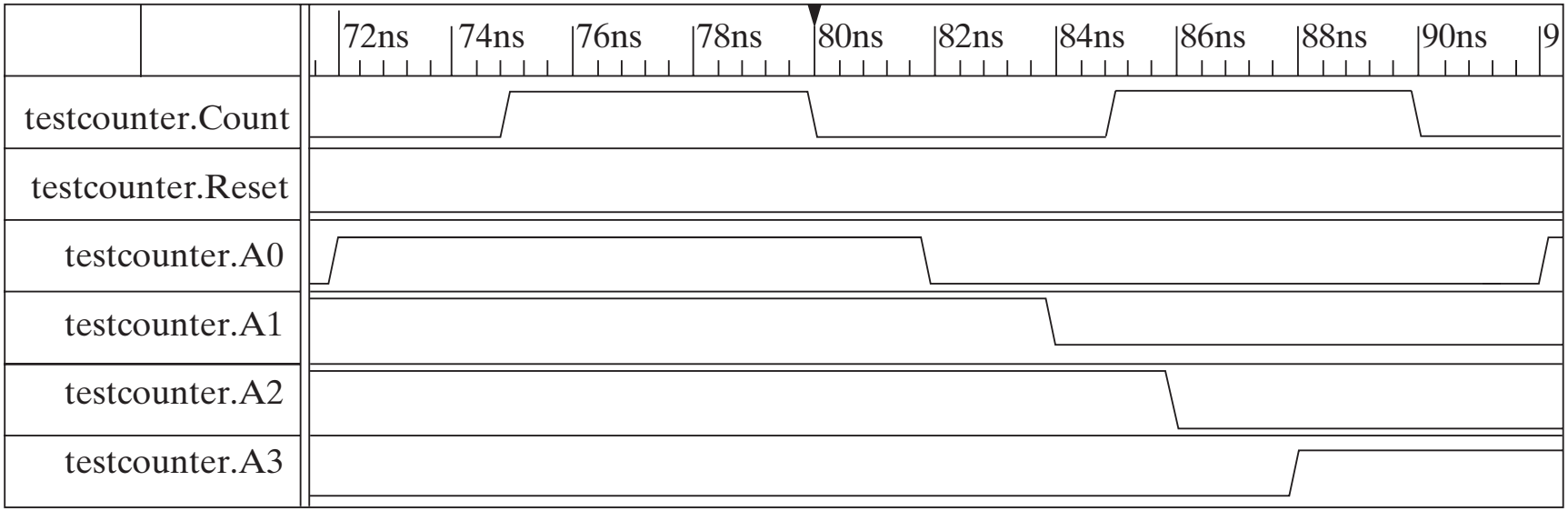
Fig. 6-18 Construction of a Johnson Counter



(a) From 0 to 170 ns



(b) From 70 to 92 ns

Fig. 6-19 Simulation Output of HDL Example 6-4

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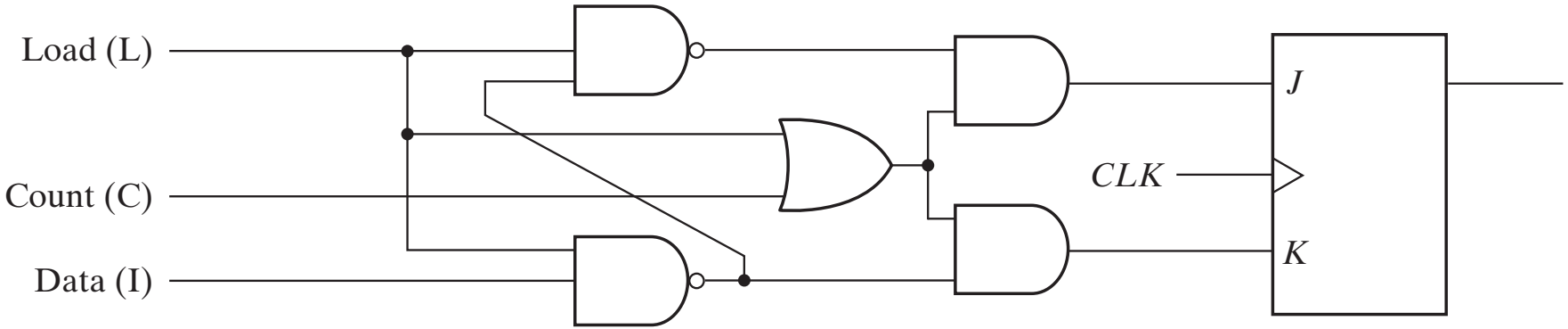

Fig. P6-21

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