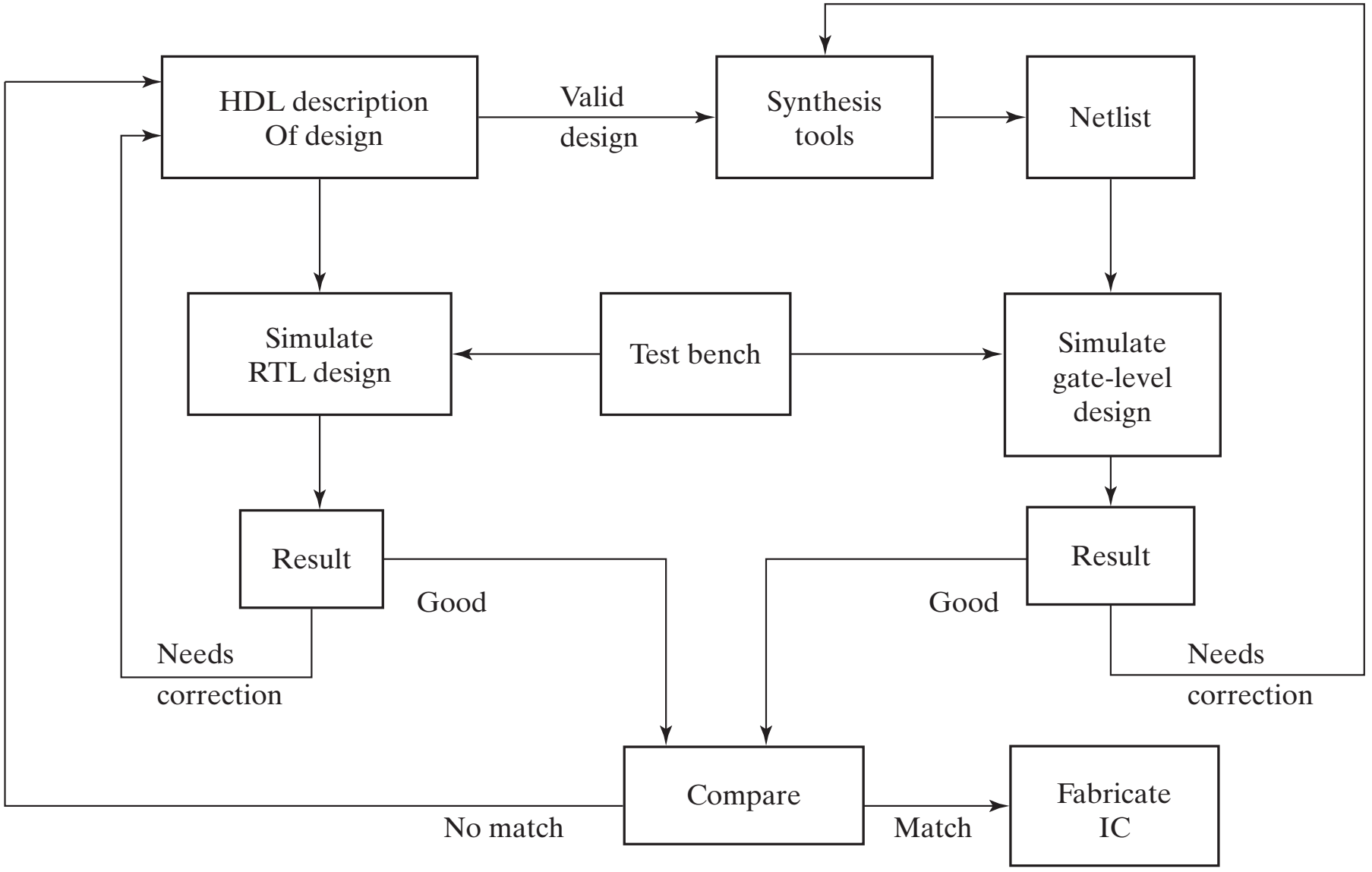


Fig. 8-1 Process of HDL Simulation and Synthesis

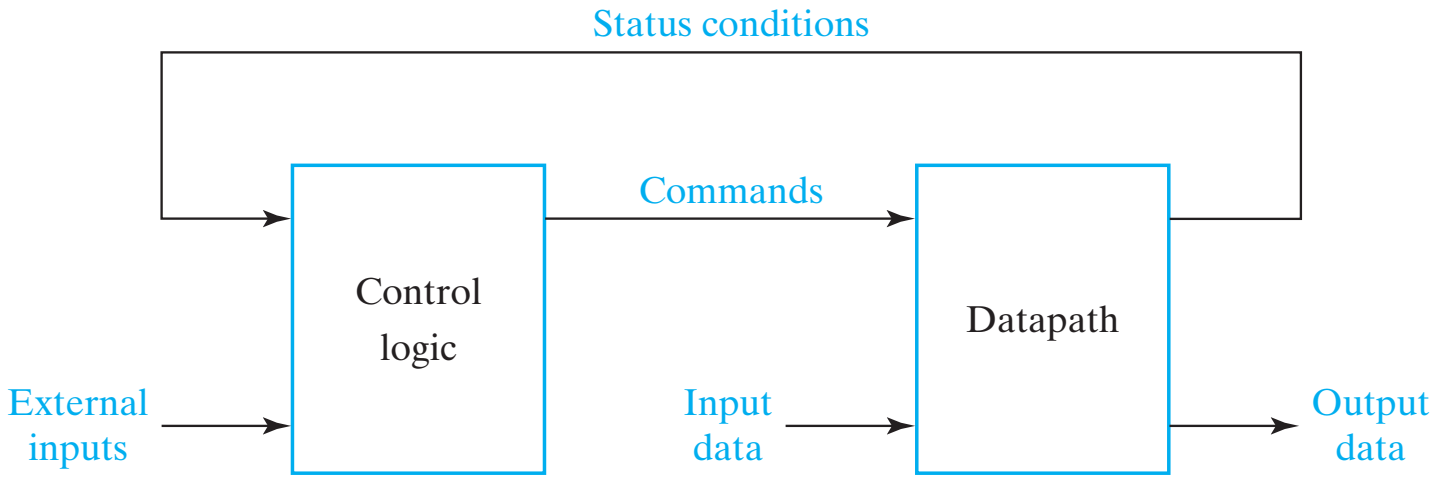


Fig. 8-2 Control and Datapath Interaction

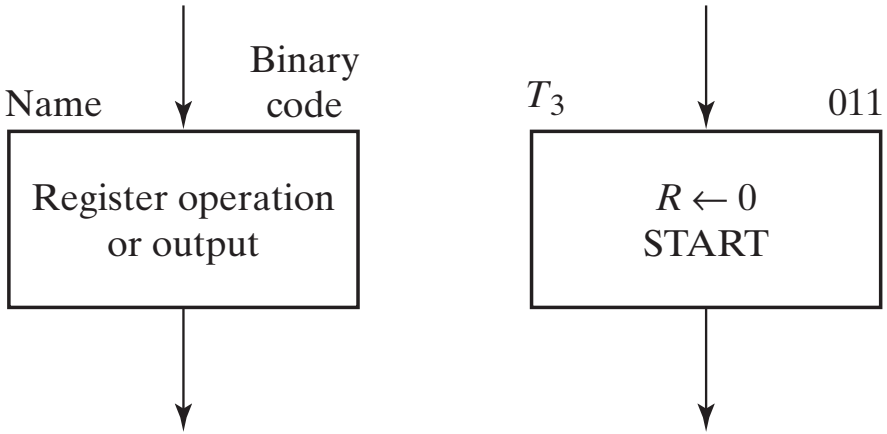


Fig. 8-3 State Box

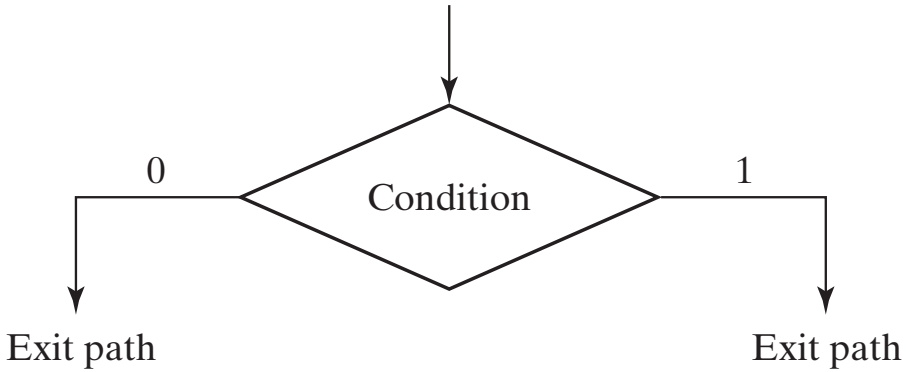
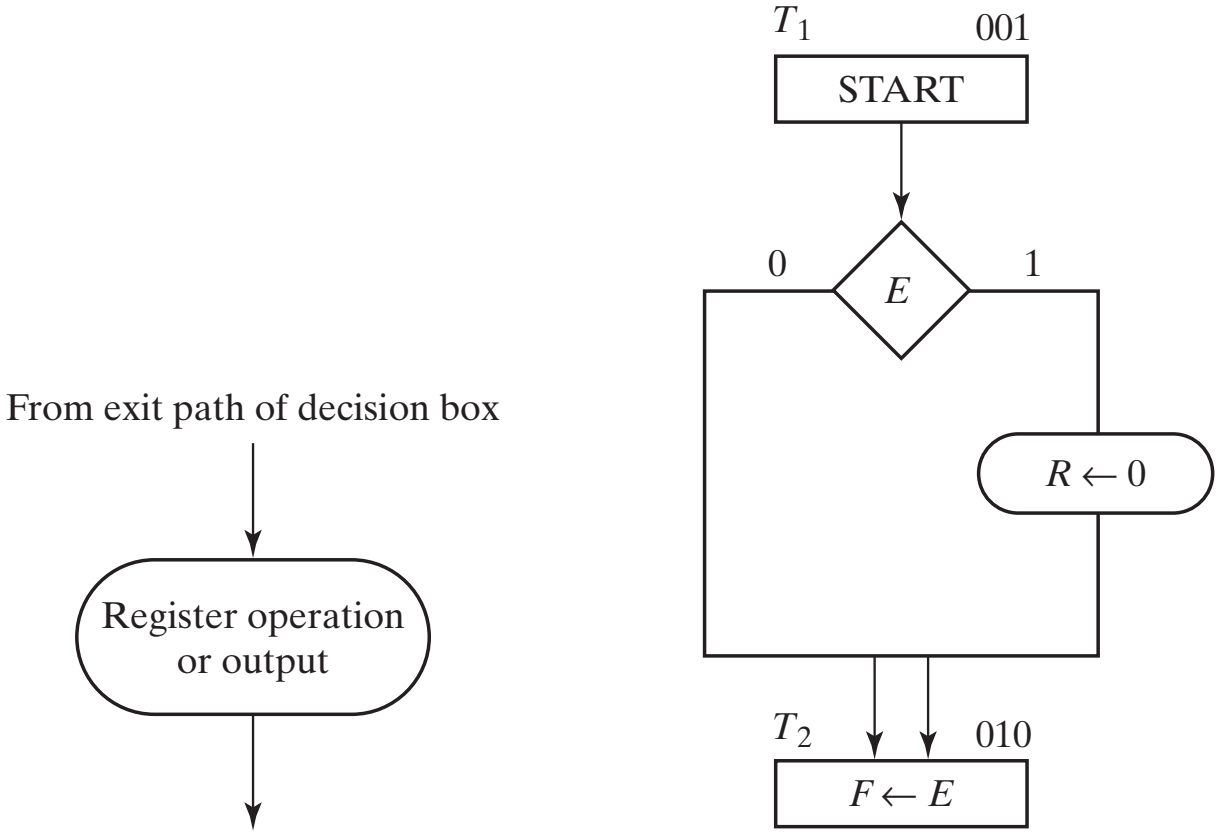


Fig. 8-4 Decision Box



(a) General description (b) Example with conditional box

Fig. 8-5 Conditional Box

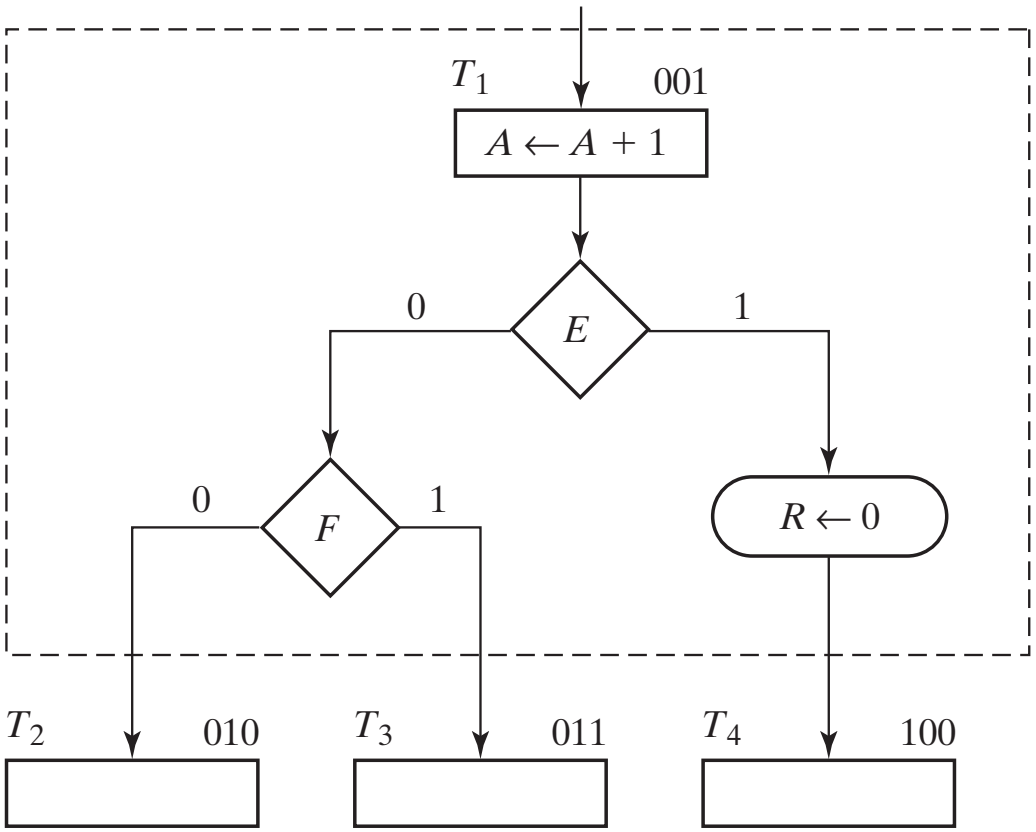


Fig. 8-6 ASM Block

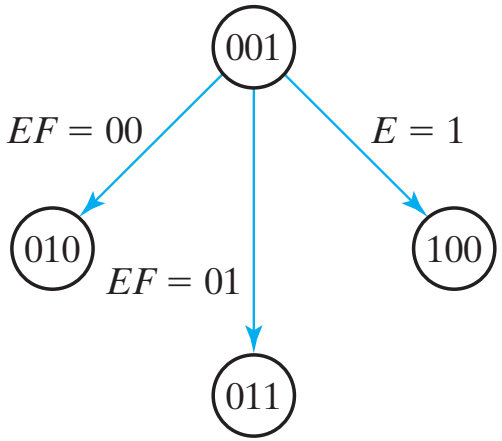


Fig. 8-7 State Diagram Equivalent to the ASM Chart of Fig. 8-6

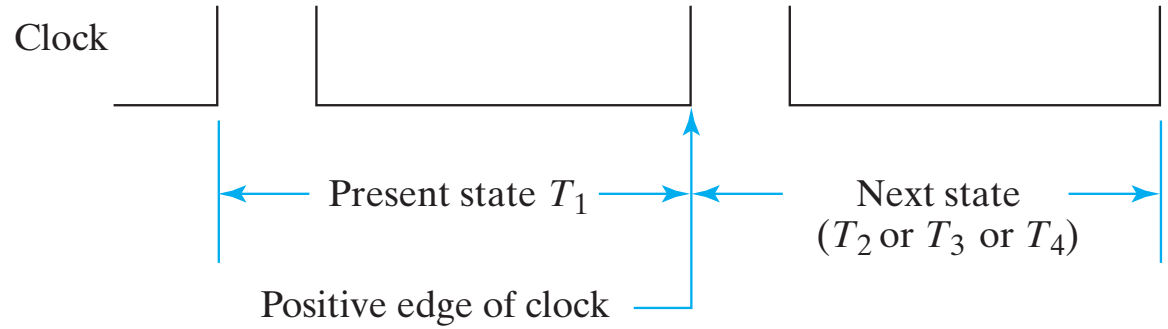


Fig. 8-8 Transition Between States

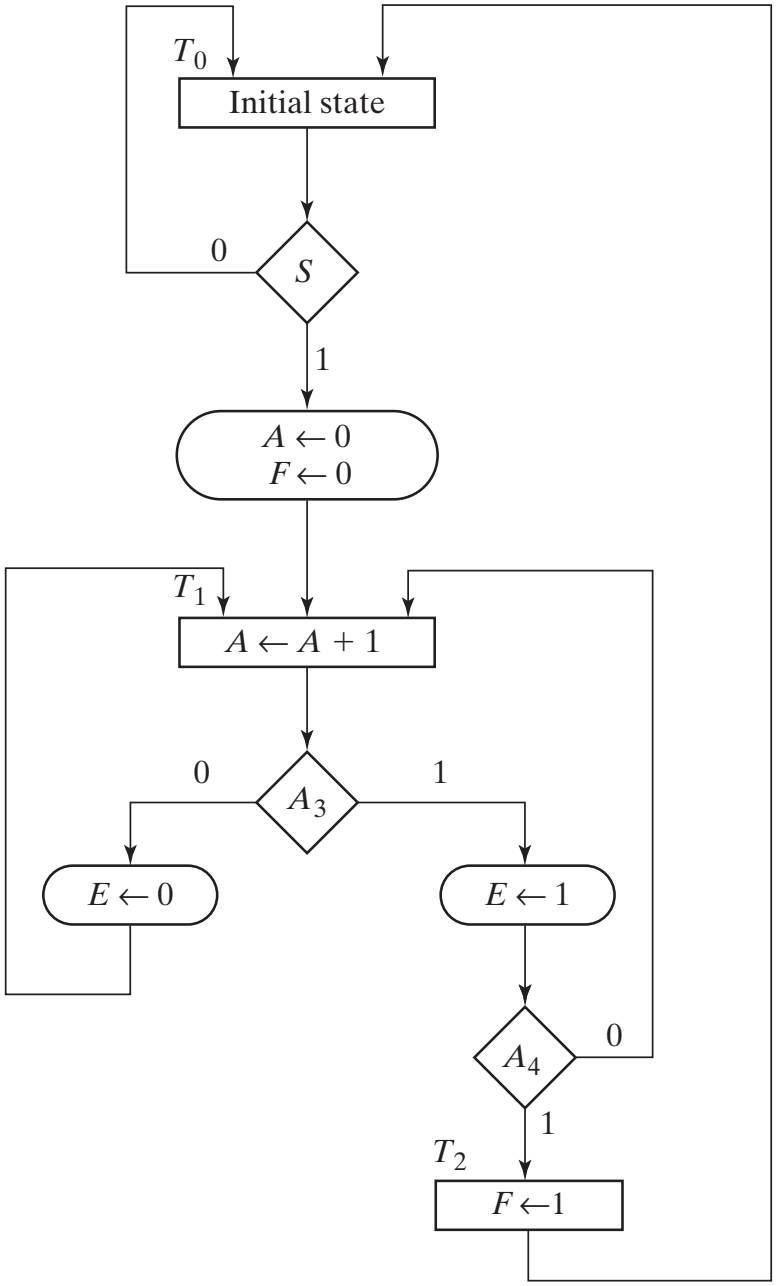


Fig. 8-9 ASM Chart for Design Example

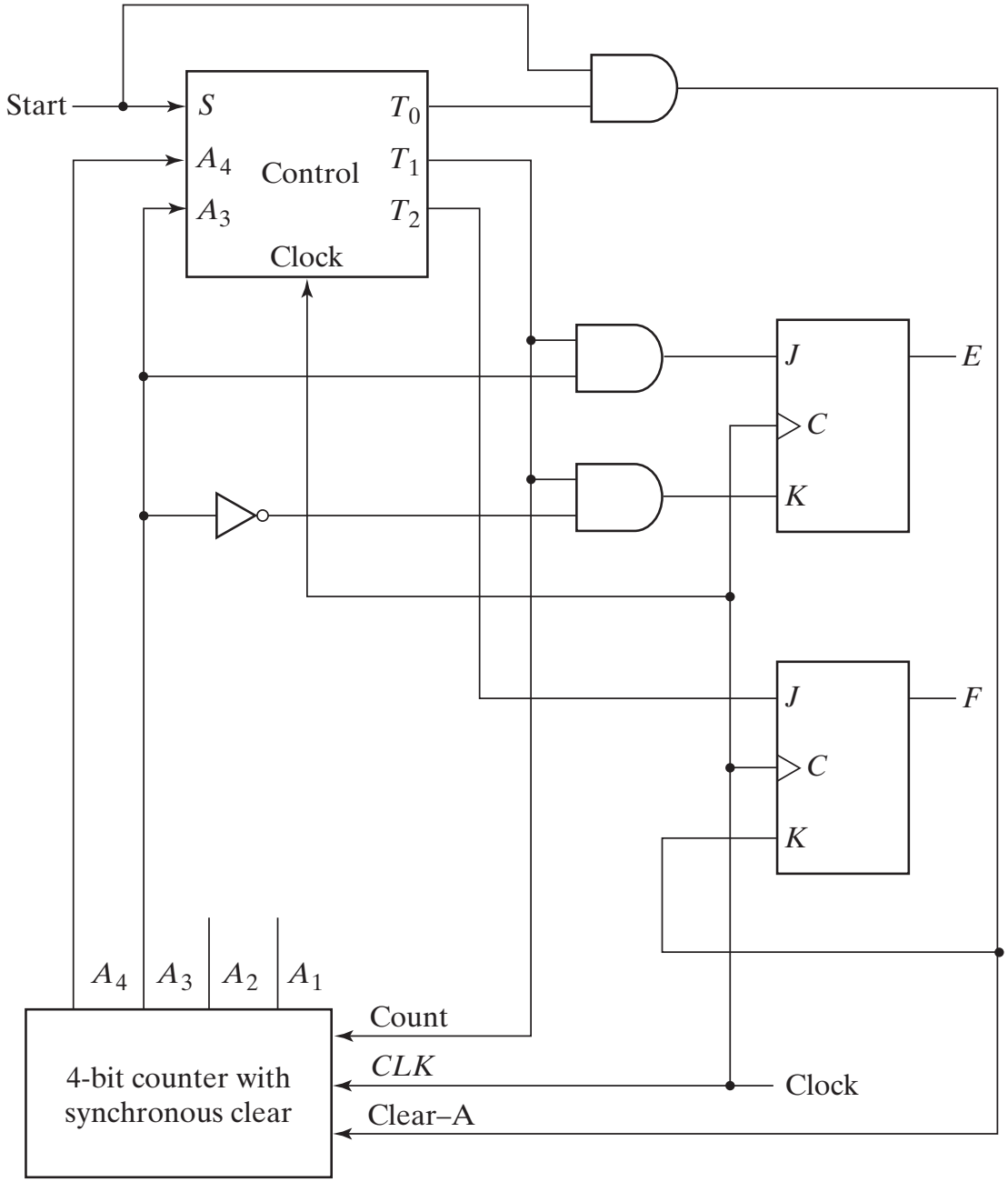
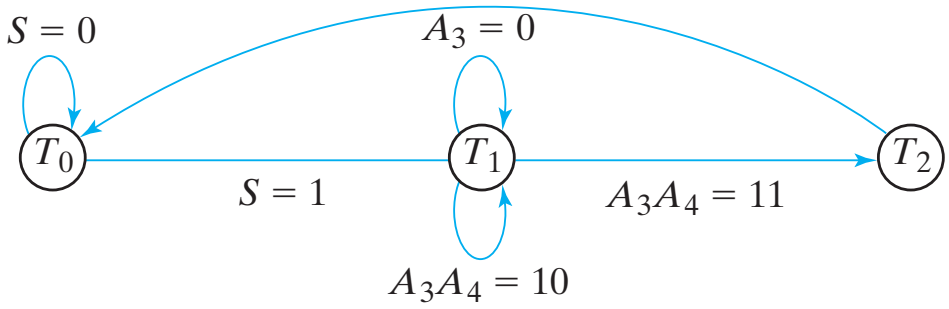


Fig. 8-10 Datapath for Design Example



(a) State diagram for control

T_0: if $(S = 1)$ then $A \leftarrow 0, F \leftarrow 0$

T_1: $A \leftarrow A + 1$

if $(A_3 = 1)$ then $E \leftarrow 1$

if $(A_3 = 0)$ then $E \leftarrow 0$

T_2: $F \leftarrow 1$

(a) Register transfer operations

Fig. 8-11 Register Transfer Level Description of Design Example

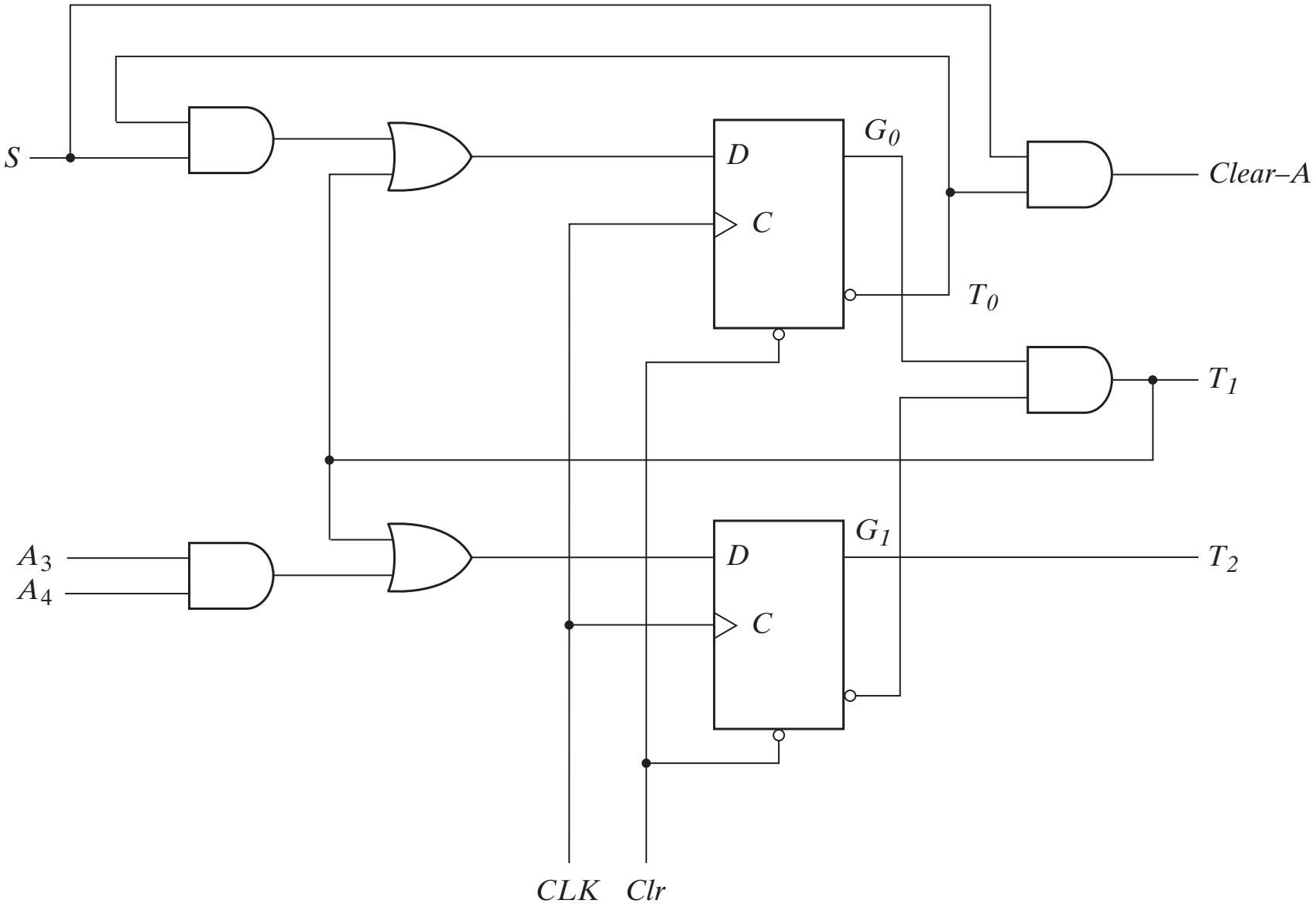


Fig. 8-12 Logic Diagram of Control

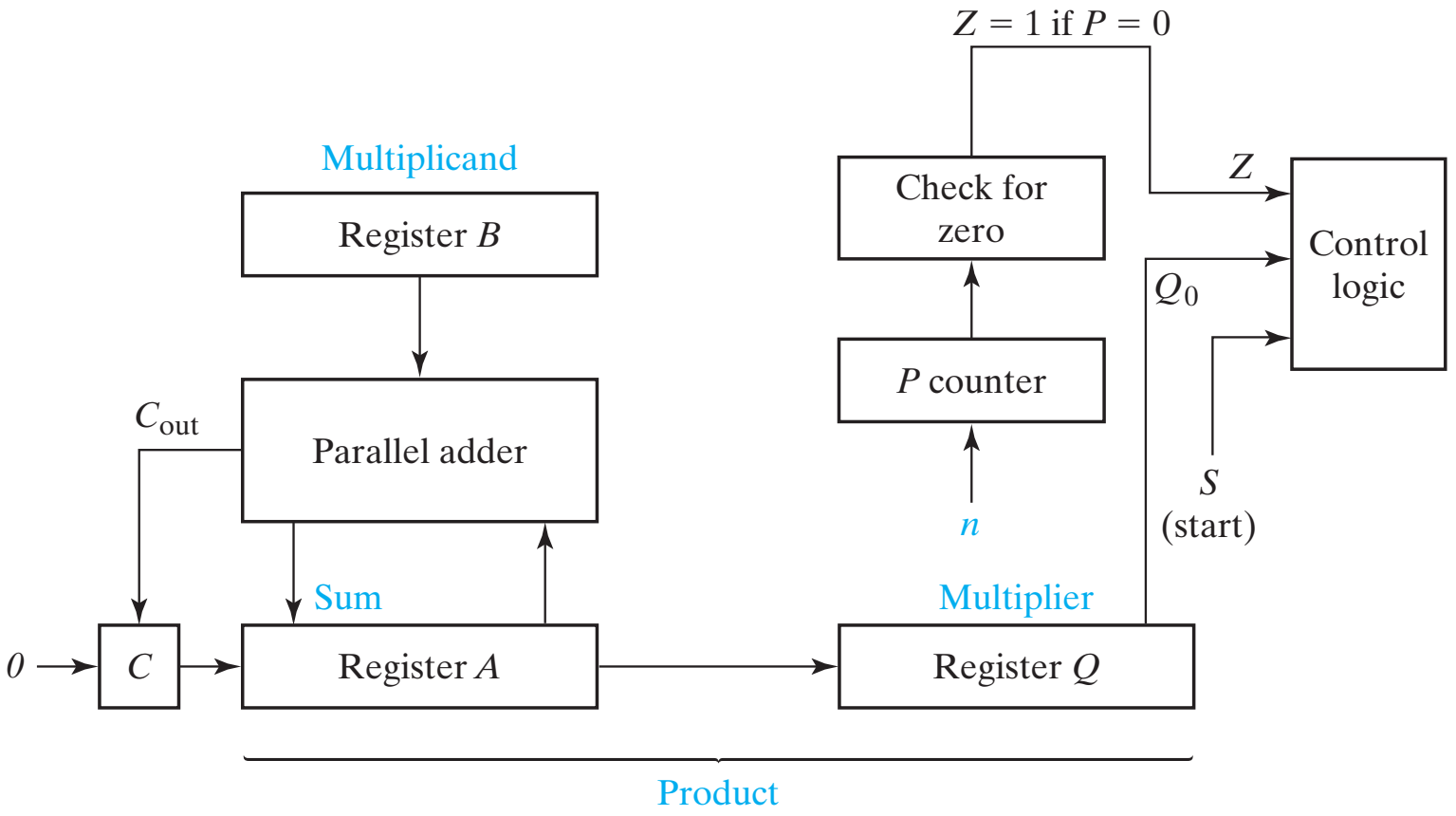


Fig. 8-13 Block Diagram of Binary Multiplier

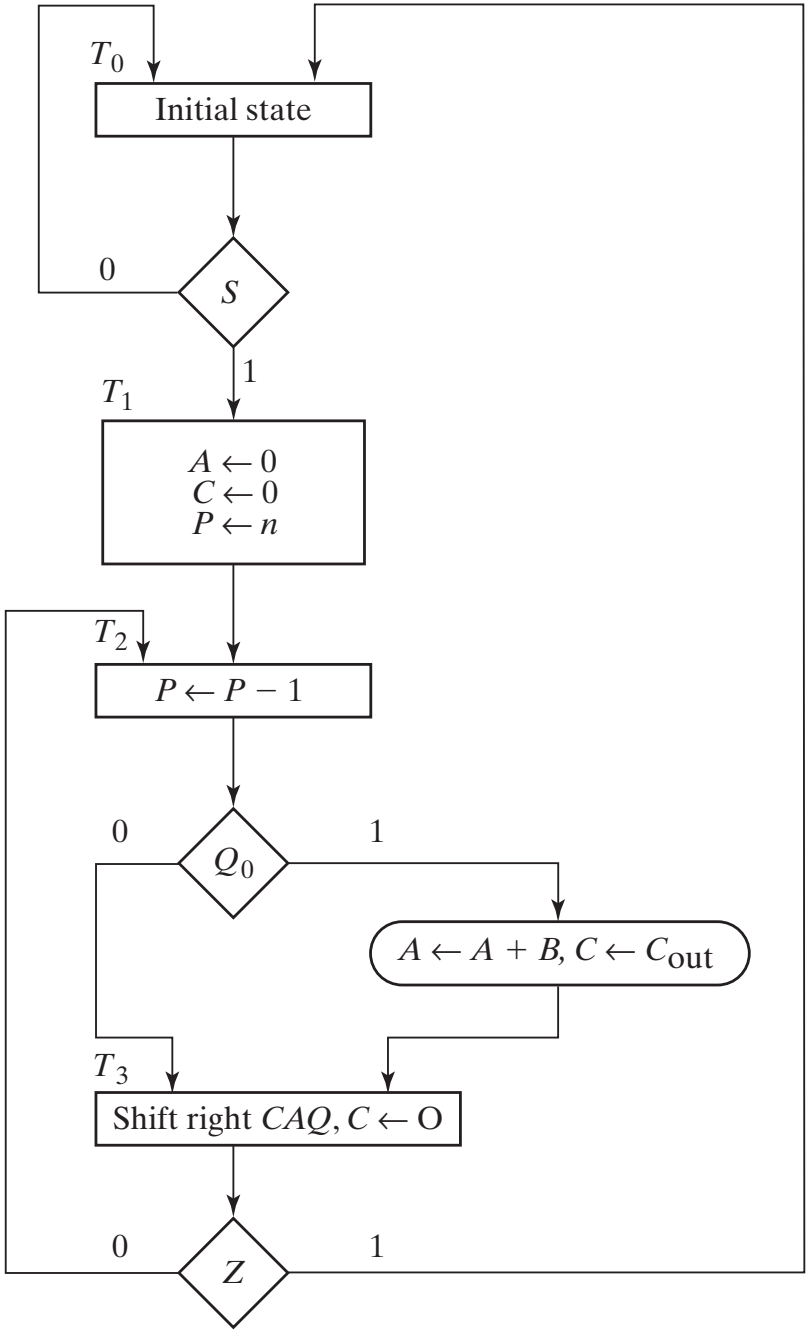
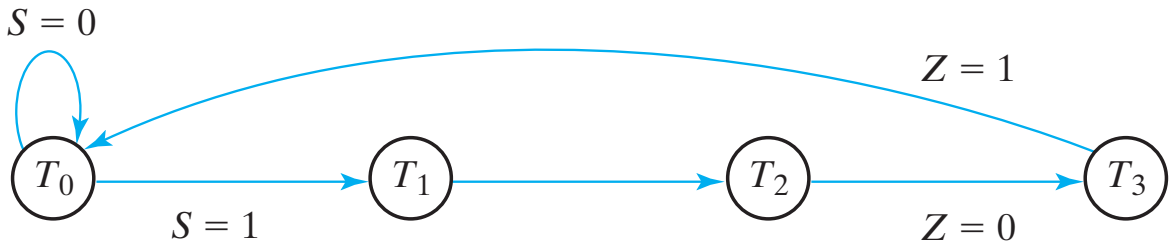


Fig. 8-14 ASM Chart for Binary Multiplier



(a) State diagram

T_0: Initial state

T_1: $A \leftarrow 0, C \leftarrow 0, P \leftarrow n$

T_2: $P \leftarrow P - 1$

if $(Q_0) = 1$ then $(A \leftarrow A + B, C \leftarrow C_{out})$

T_3: shift right CAQ, $C \leftarrow 0$

(b) Register transfer operations

Fig. 8-15 Control Specifications for Binary Multiplier

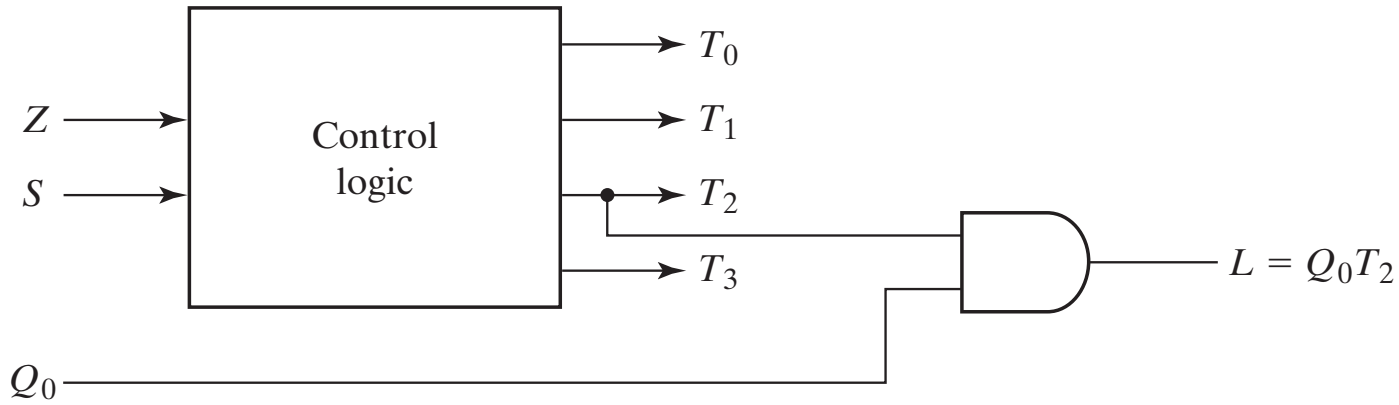


Fig. 8-16 Control Block Diagram

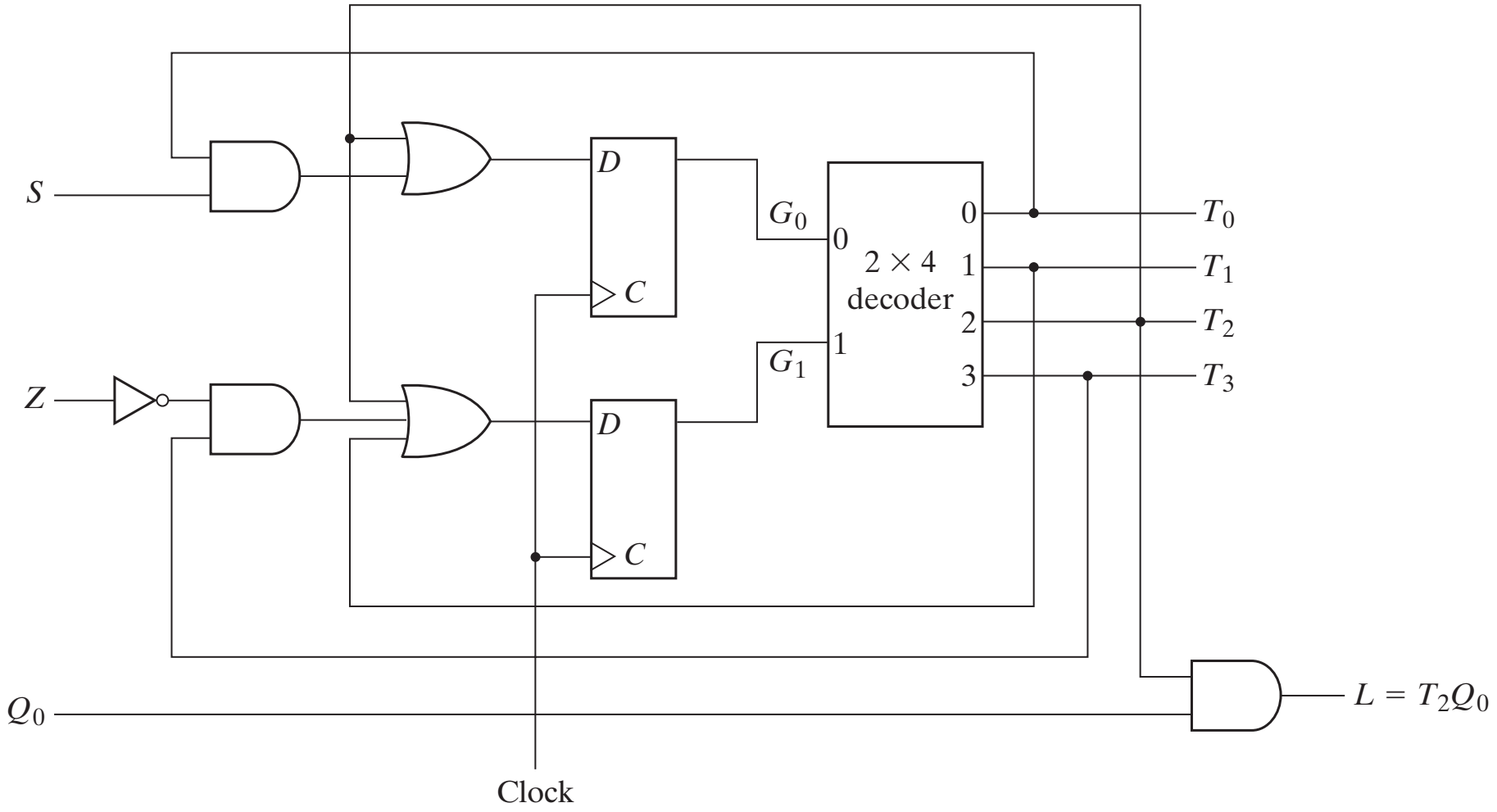


Fig. 8-17 Logic Diagram of Control for Binary Multiplier Using a Sequence Register and Decoder

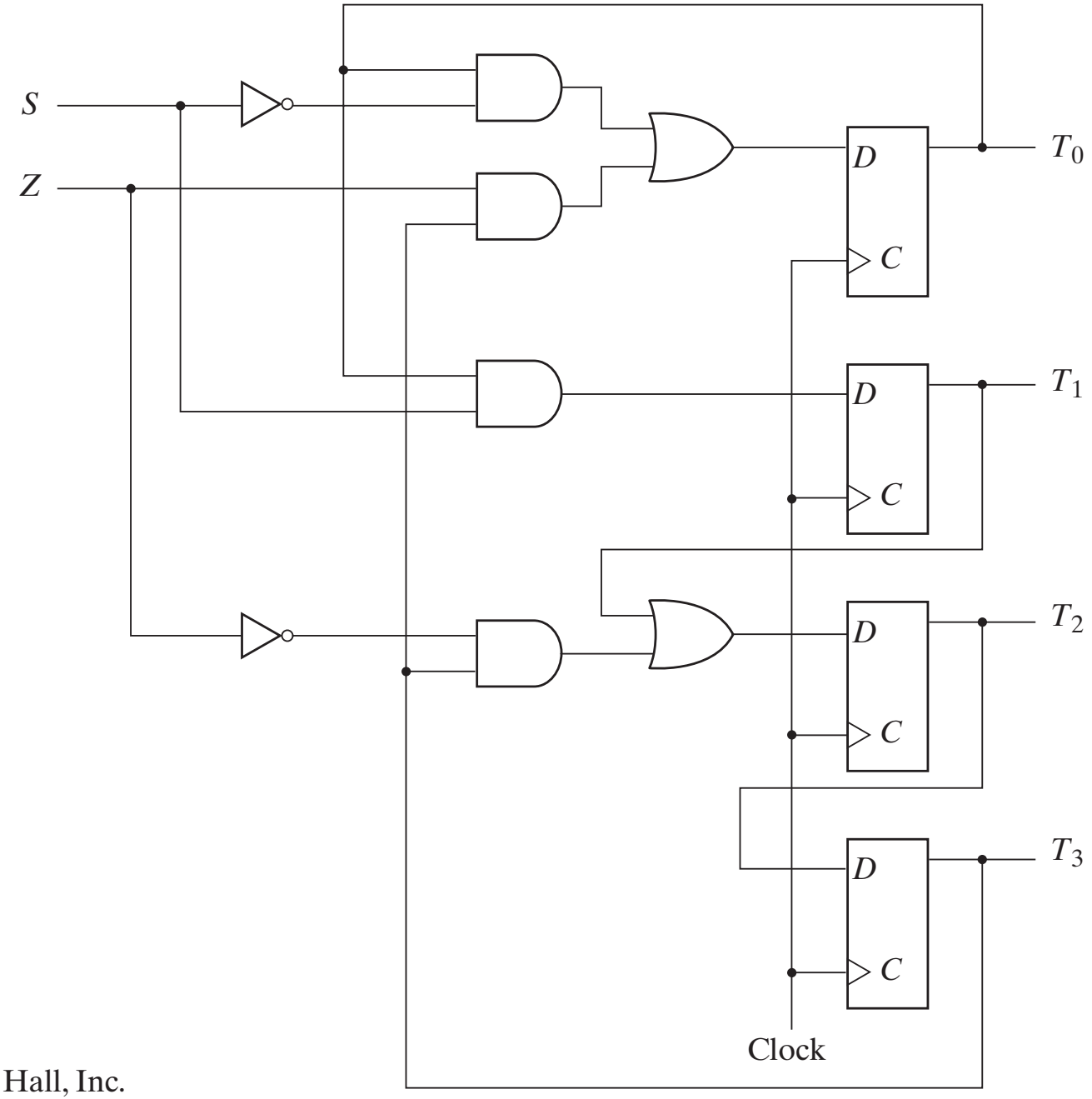


Fig. 8-18 One Flip-Flop Per State Controller

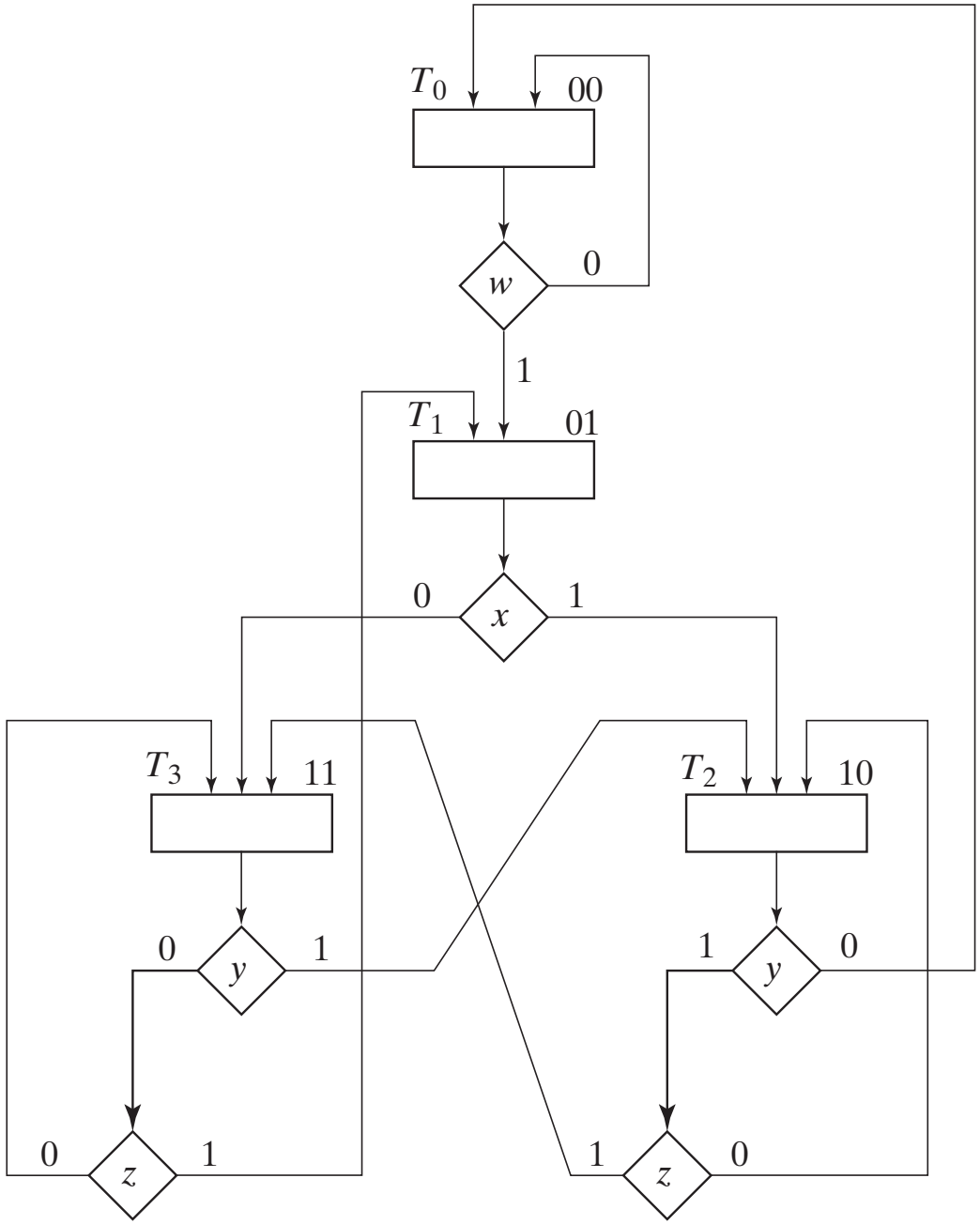


Fig. 8-19 Example of ASM Chart with Four Control Inputs

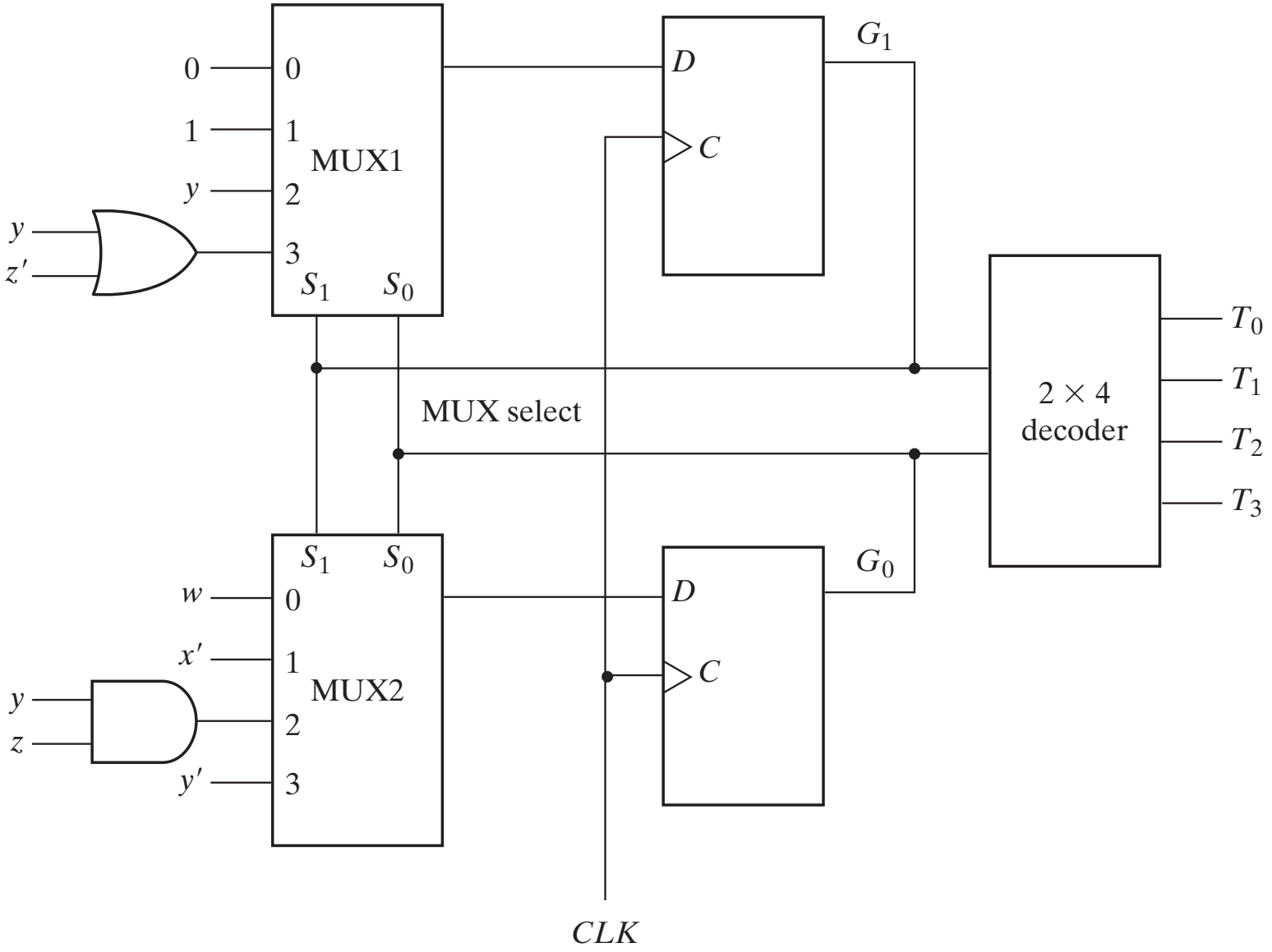


Fig. 8-20 Control Implementation with Multiplexers

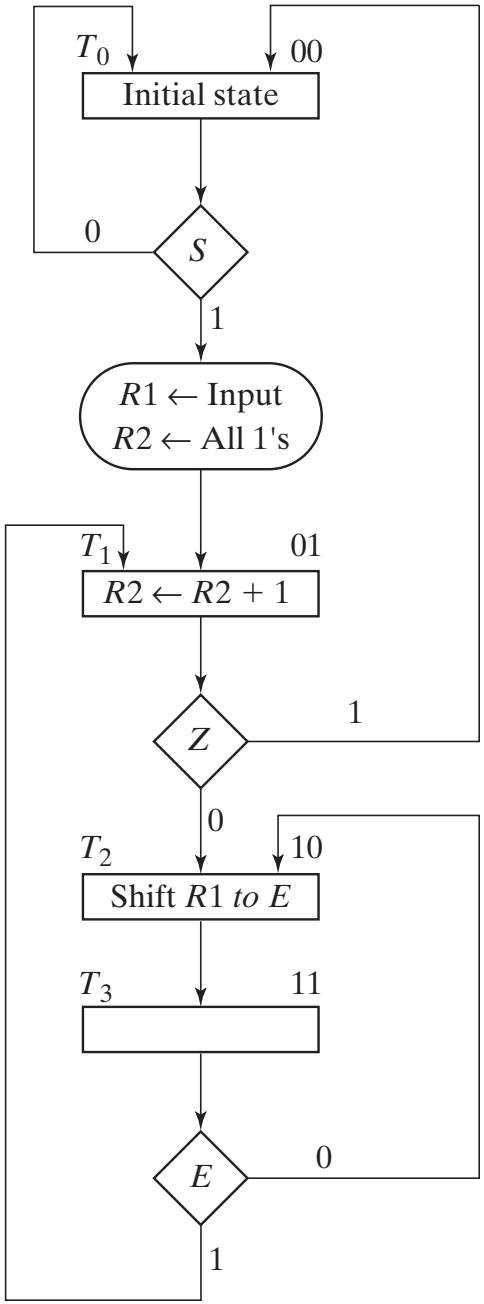


Fig. 8-21 ASM Chart for Count-of-Ones Circuit

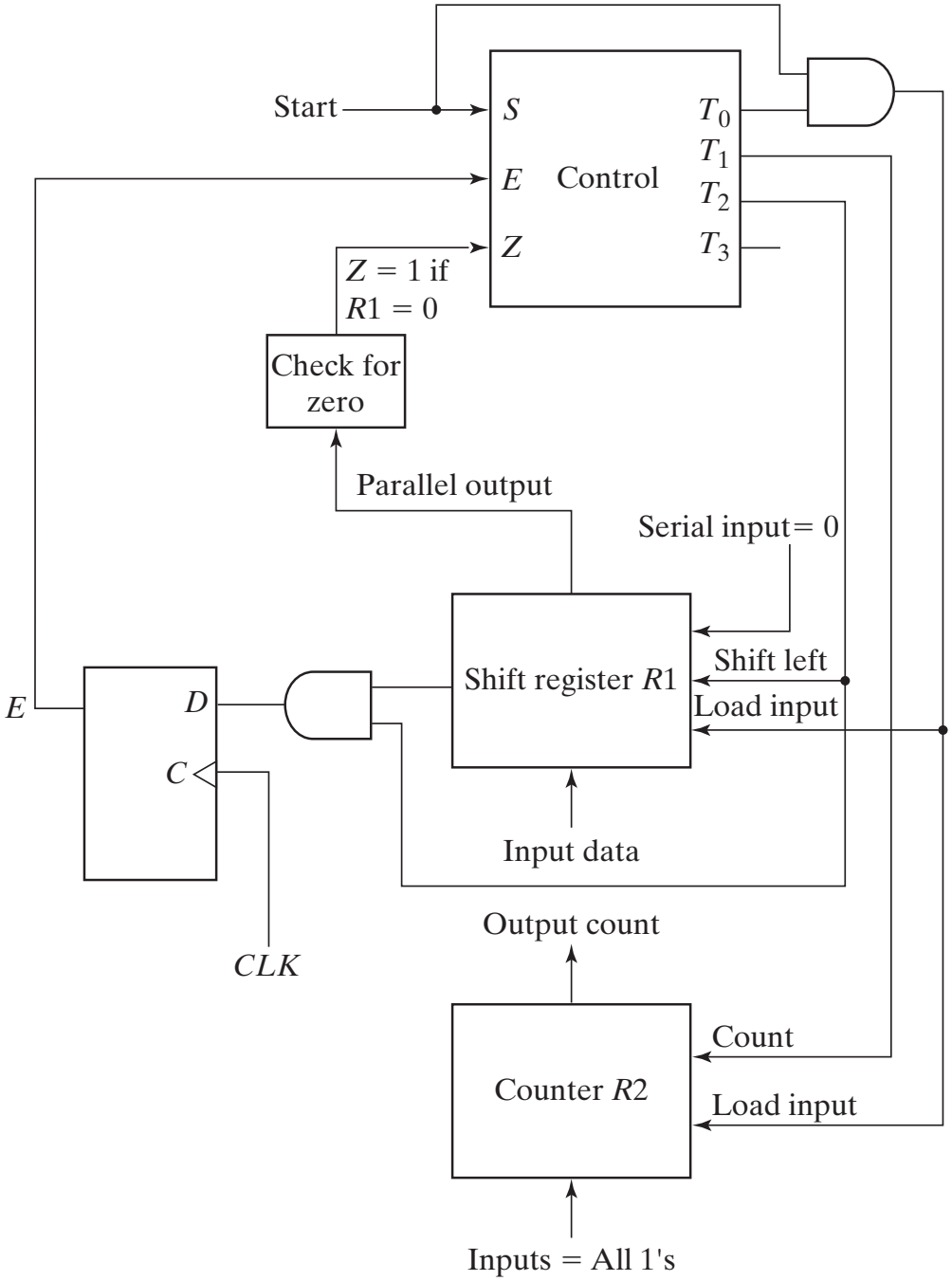


Fig. 8-22 Block Diagram for Count-of-Ones

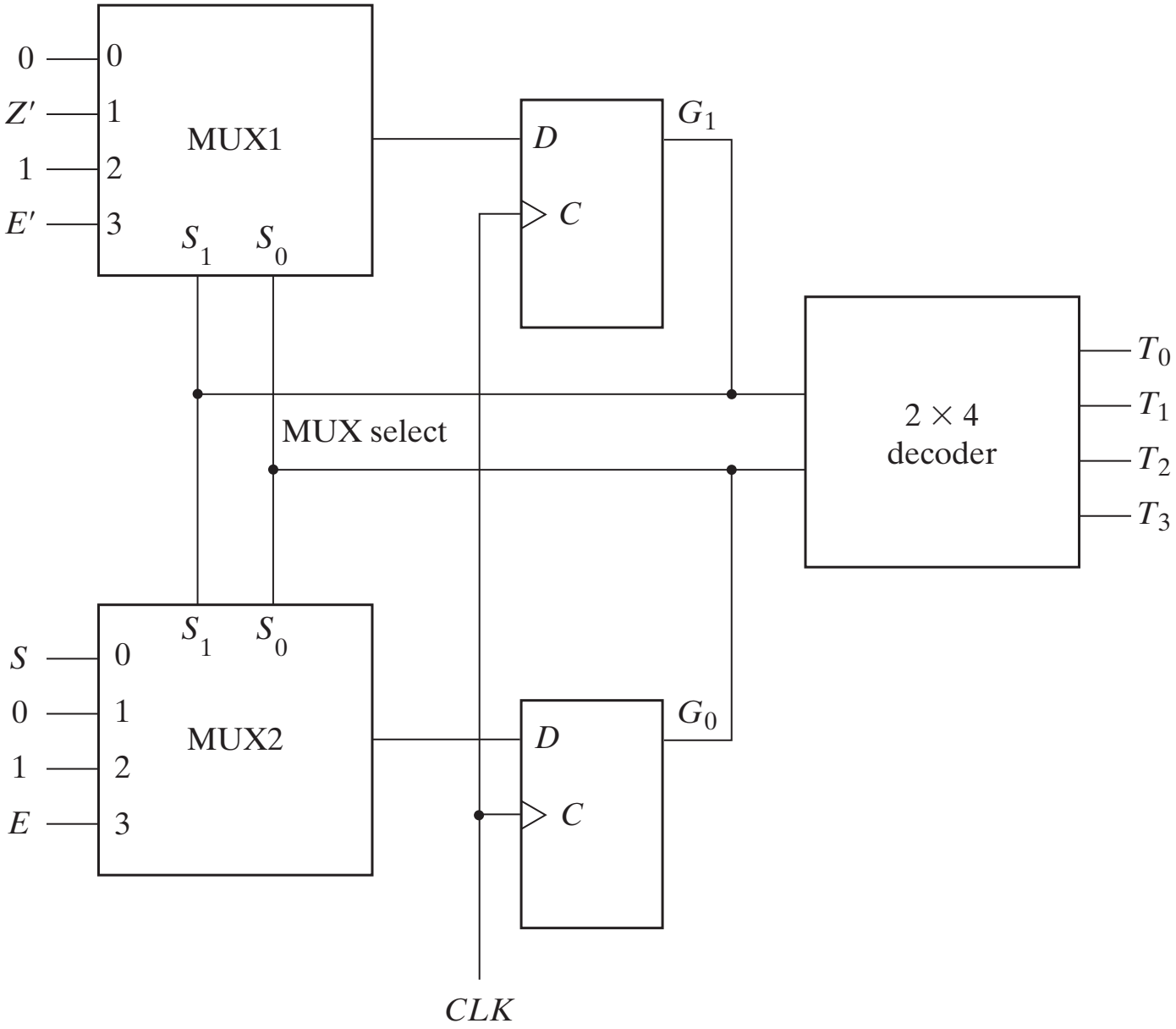


Fig. 8-23 Control Implementation for Count-of-Ones Circuit

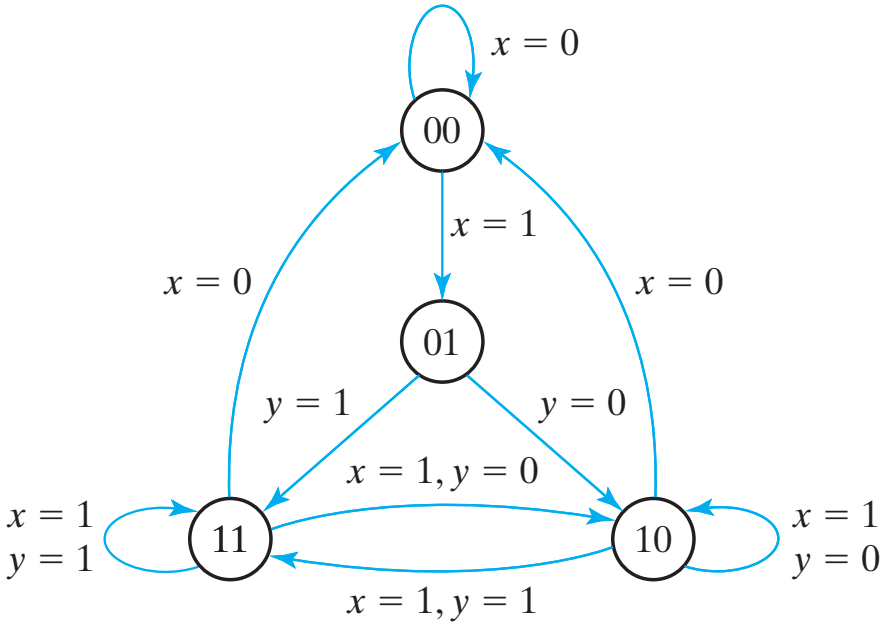


Fig. P8-10 Control State Diagram for Problems 8-10 and 8-11

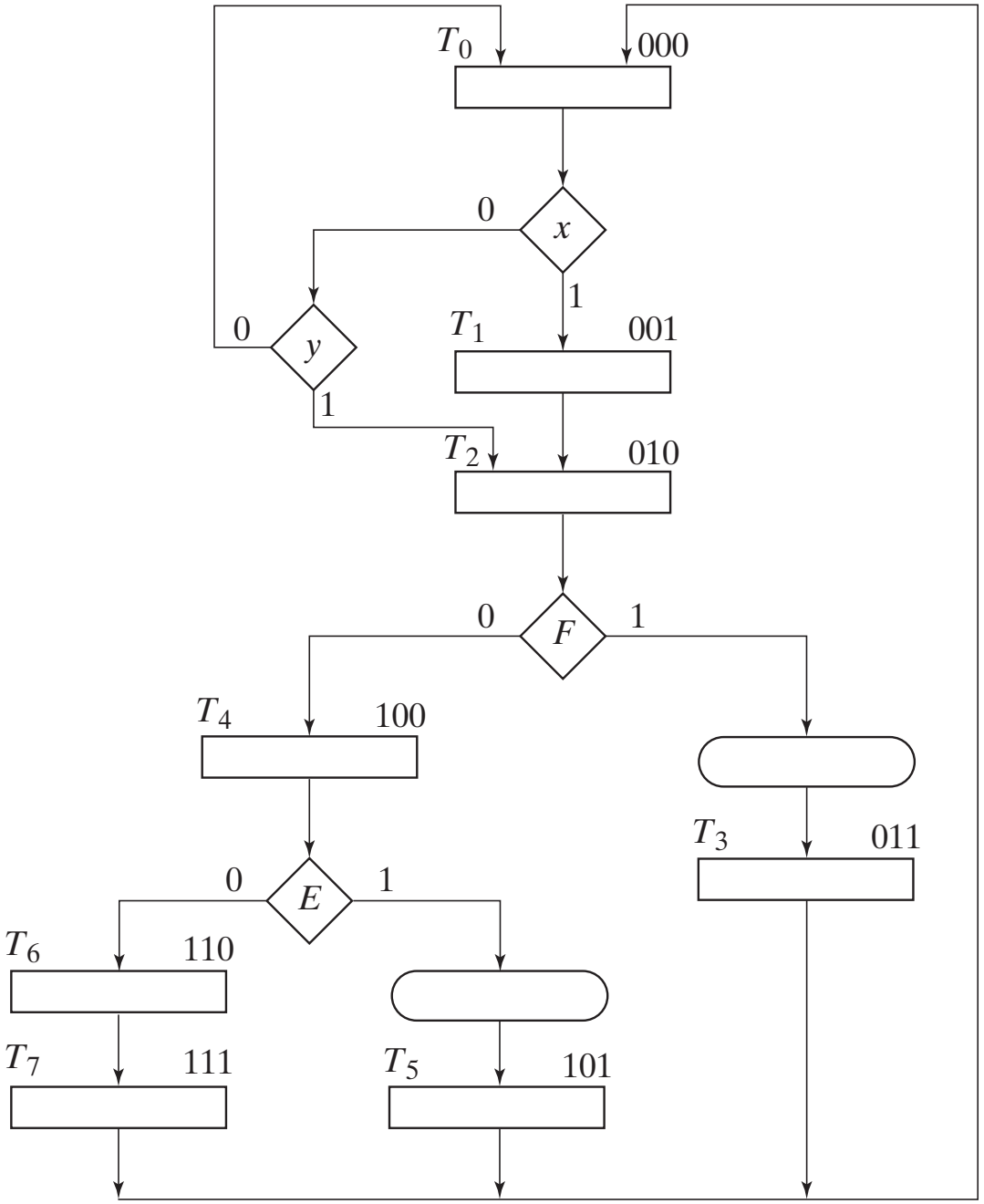


Fig. P8-20 ASM Chart for Problems 8-20