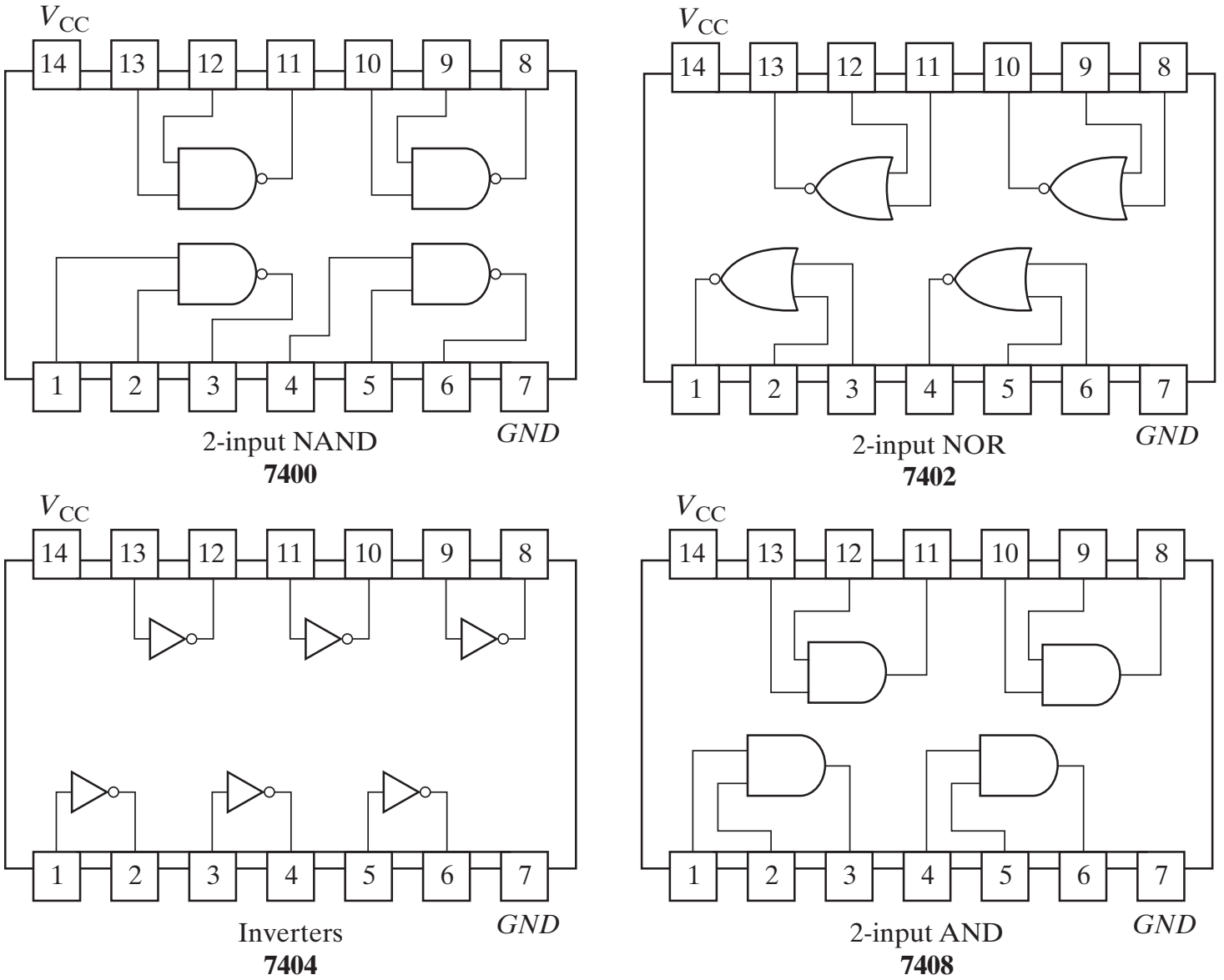


Fig. 11-1 Digital Gates in IC Packages with Identification Numbers and Pin Assignments

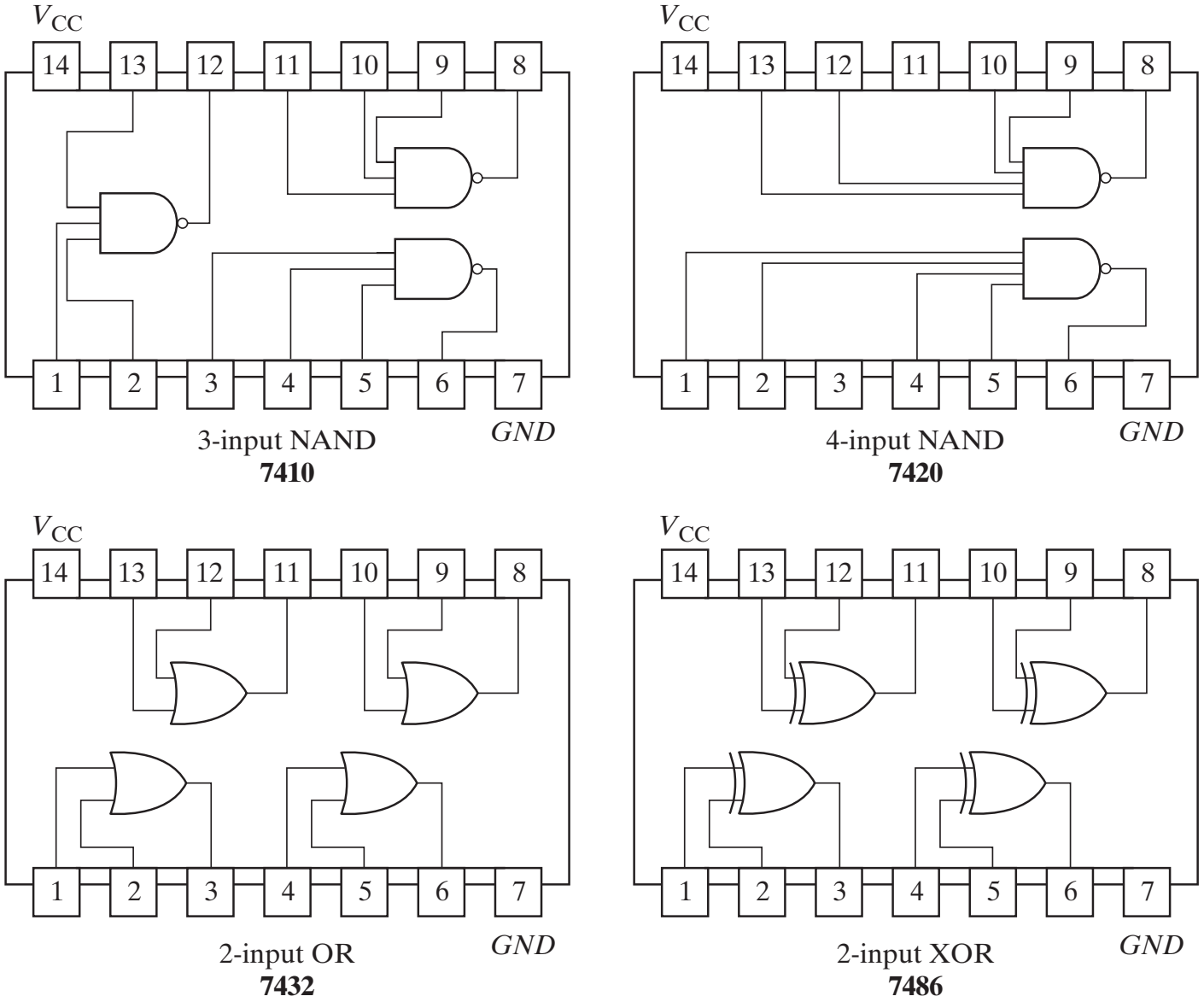
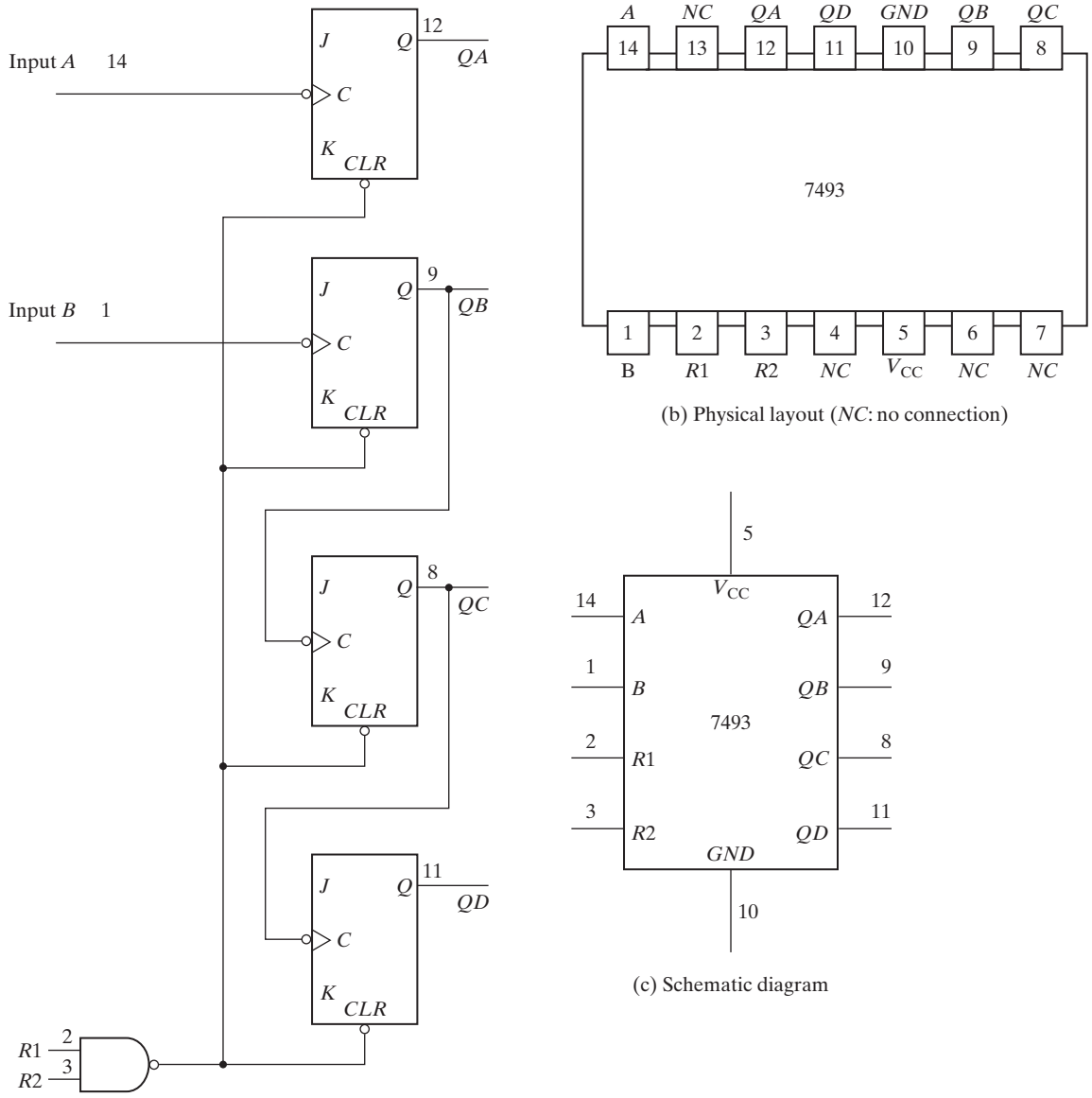


Fig. 11-1(cond) Digital Gates in IC Packages with Identification Numbers and Pin Assignments



(a) Internal circuit diagram

(b) Physical layout (*NC*: no connection)

(c) Schematic diagram

Fig. 11-2 IC Type 7493 Ripple Counter

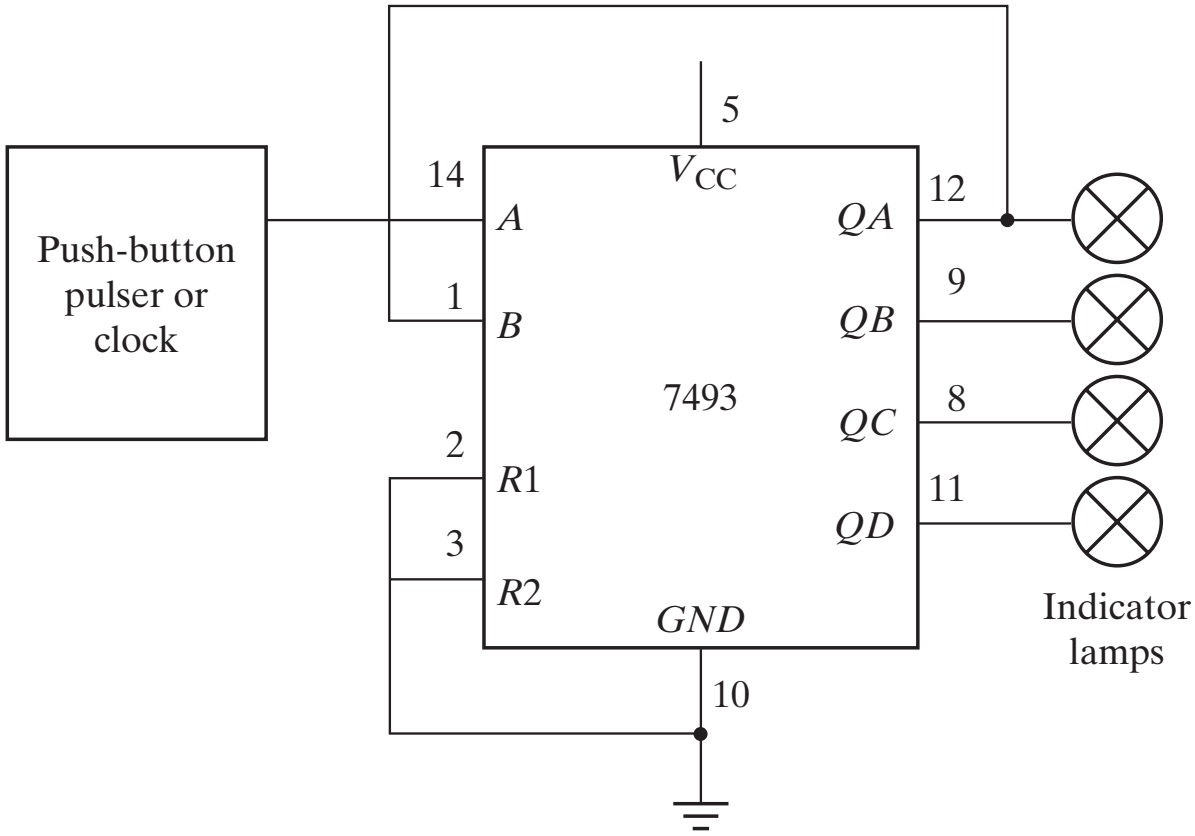


Fig. 11-3 Binary Counter

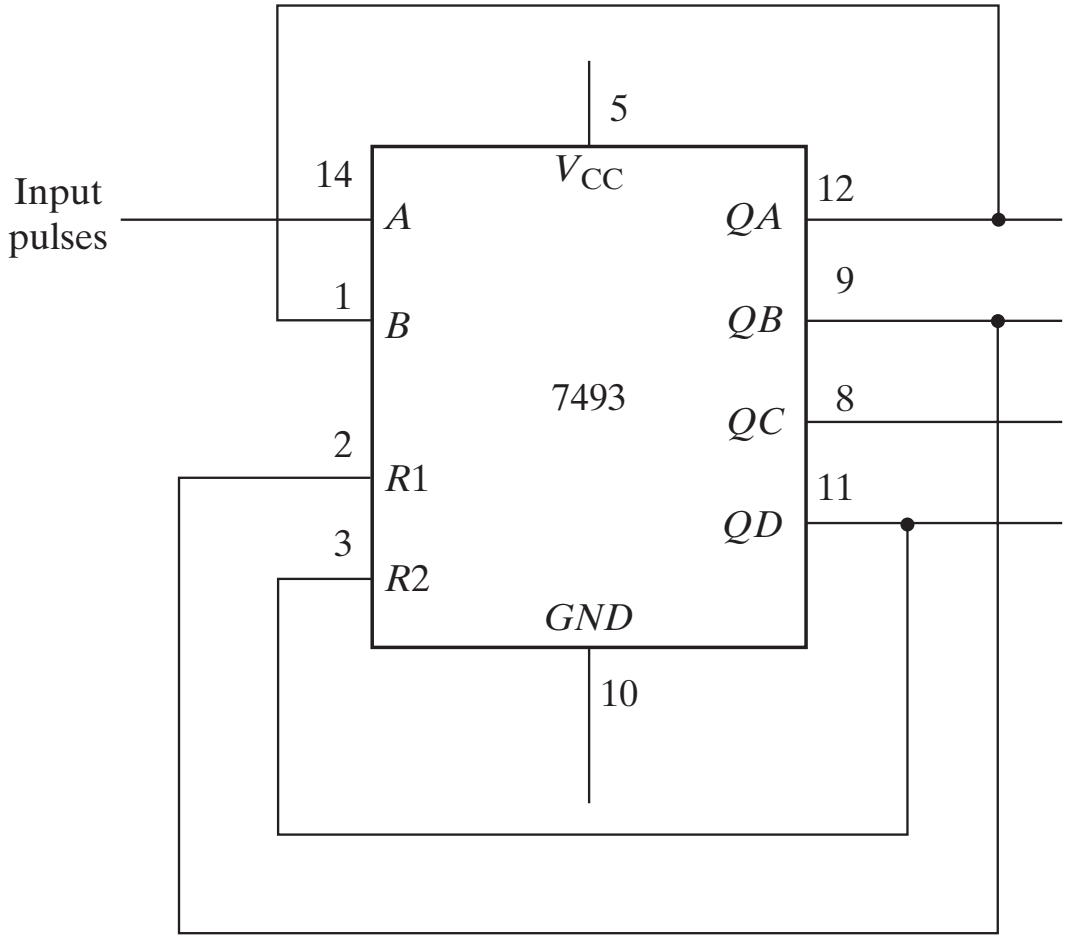
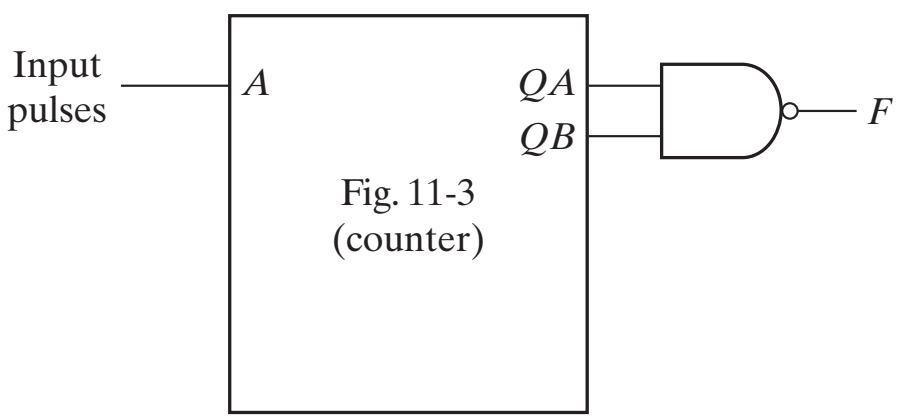


Fig. 11-4 BCD Counter



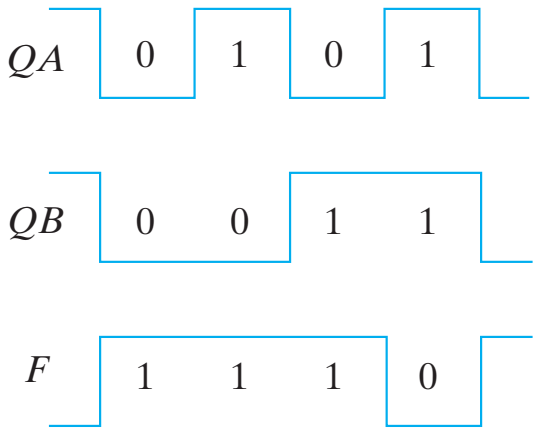


Fig. 11-5 Waveforms for NAND Gate

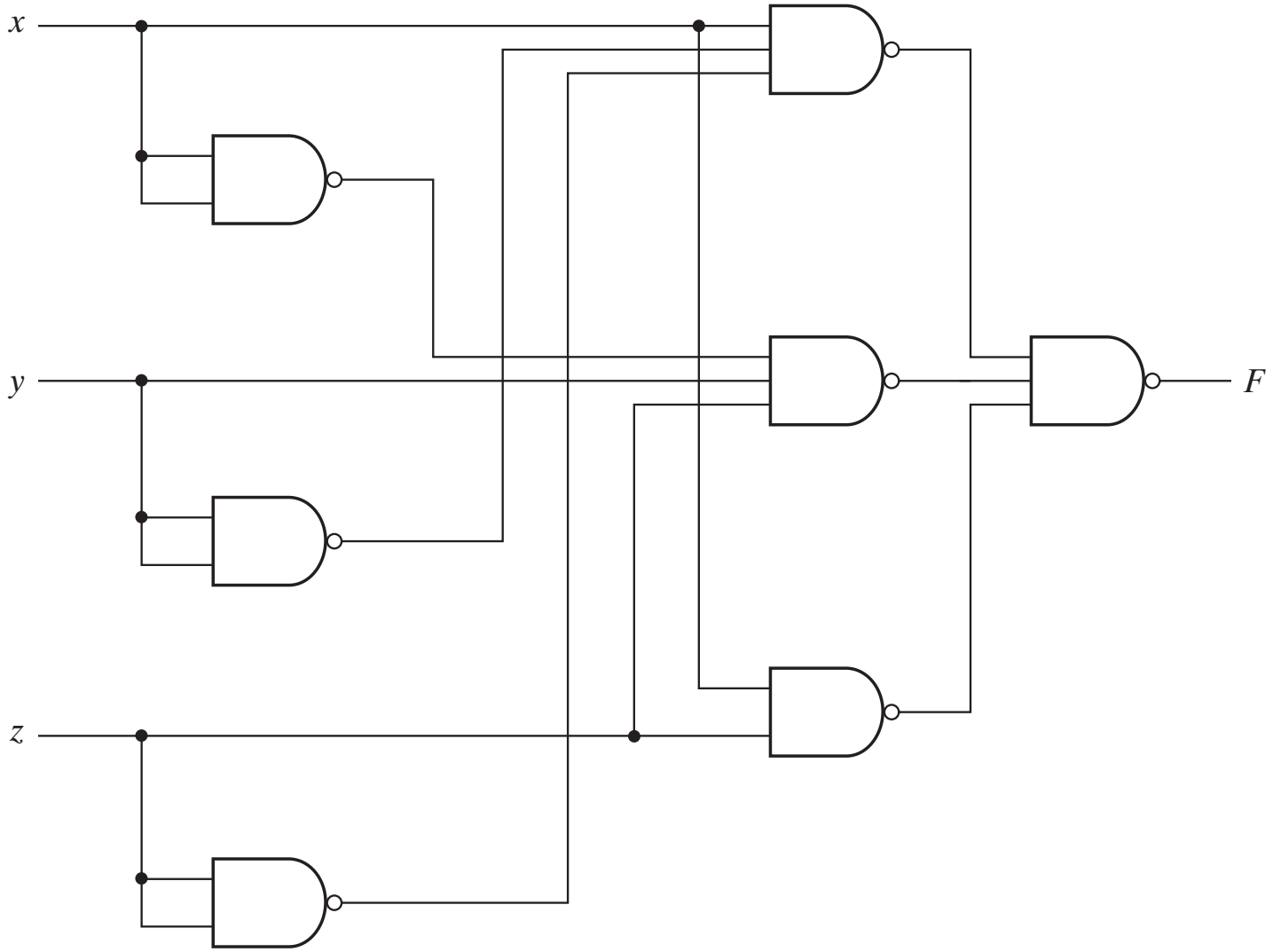
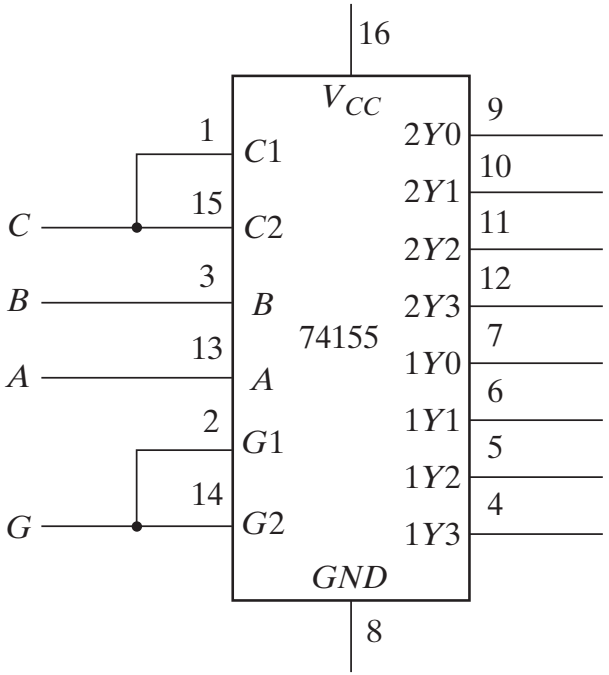


Fig. 11-6 Logic Diagram for Experiment 3



Truth table

Inputs				Outputs							
G	*C*	*B*	*A*	2*Y*0	2*Y*1	2*Y*2	2*Y*3	1*Y*0	1*Y*1	1*Y*2	1*Y*3
1	*X*	*X*	*X*	1	1	1	1	1	1	1	1
0	0	0	0	0	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1
0	1	1	0	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	0

Fig. 11-7 IC Type 74155 Connected as a 3 × 8 Decoder

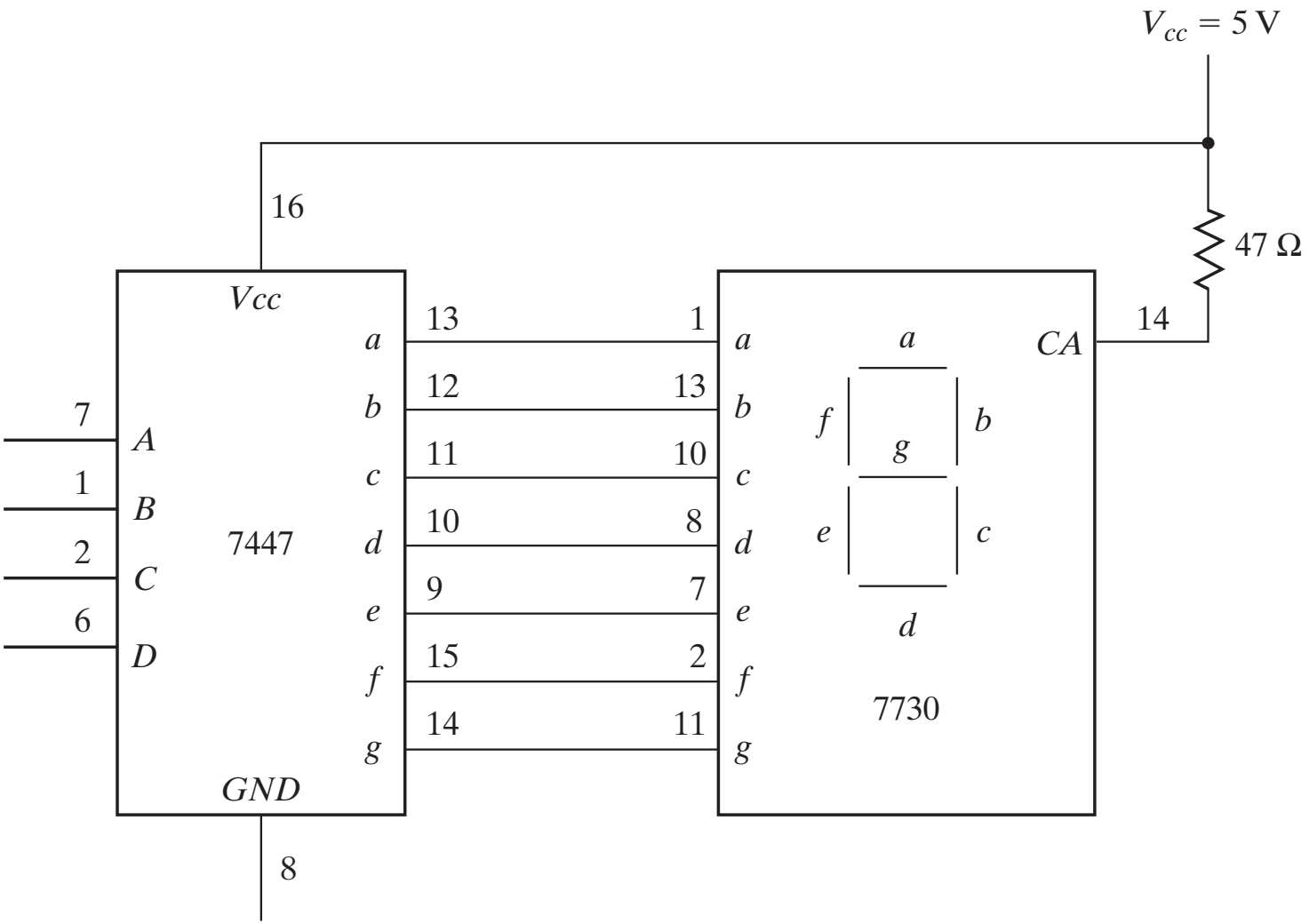
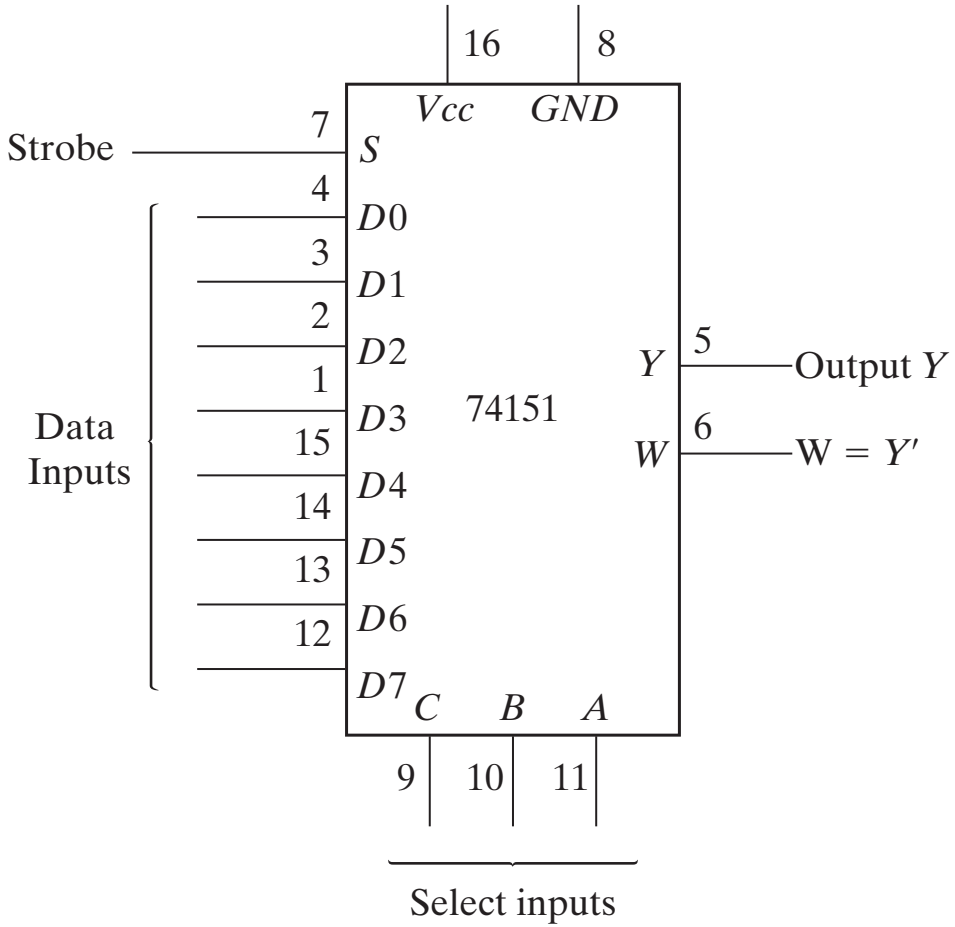


Fig. 11-8 BCD-to-Seven-Segment Decoder (7447) and Seven-Segment Display (7730)



Function table

Strobe S	Select C	B	A	Output Y
1	X	X	X	0
0	0	0	0	$D0$
0	0	0	1	$D1$
0	0	1	0	$D2$
0	0	1	1	$D3$
0	1	0	0	$D4$
0	1	0	1	$D5$
0	1	1	0	$D6$
0	1	1	1	$D7$

Fig. 11-9 IC Type 74151 8 × 1 Multiplexer

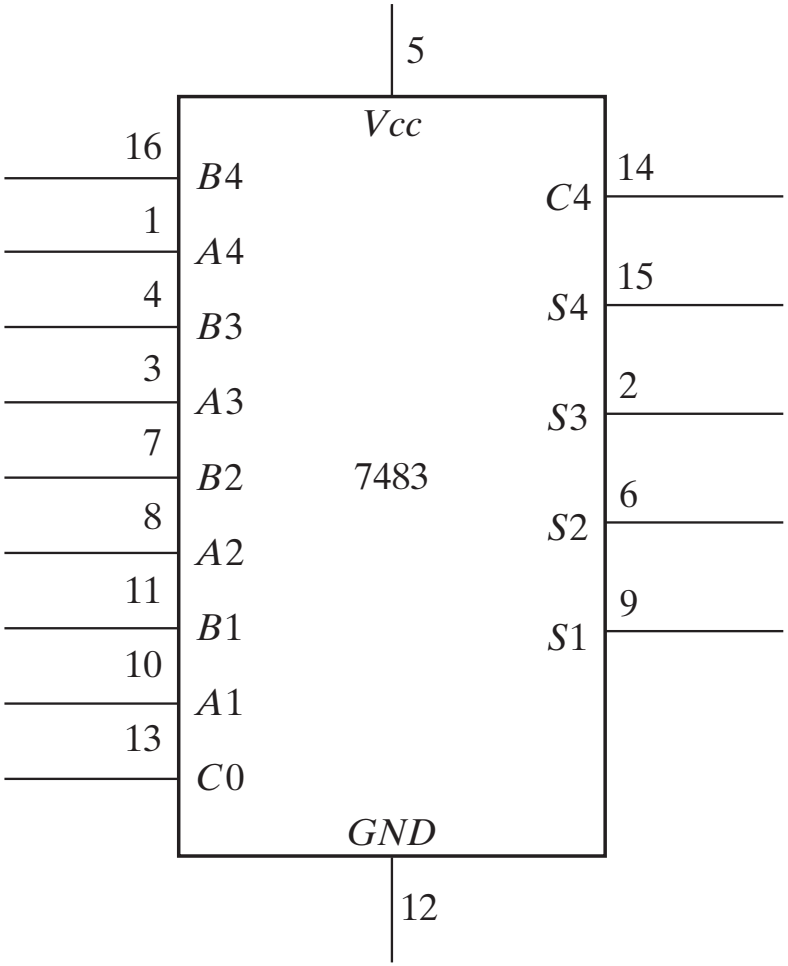


Fig. 11-10 IC Type 7483 4-Bit Binary Adder

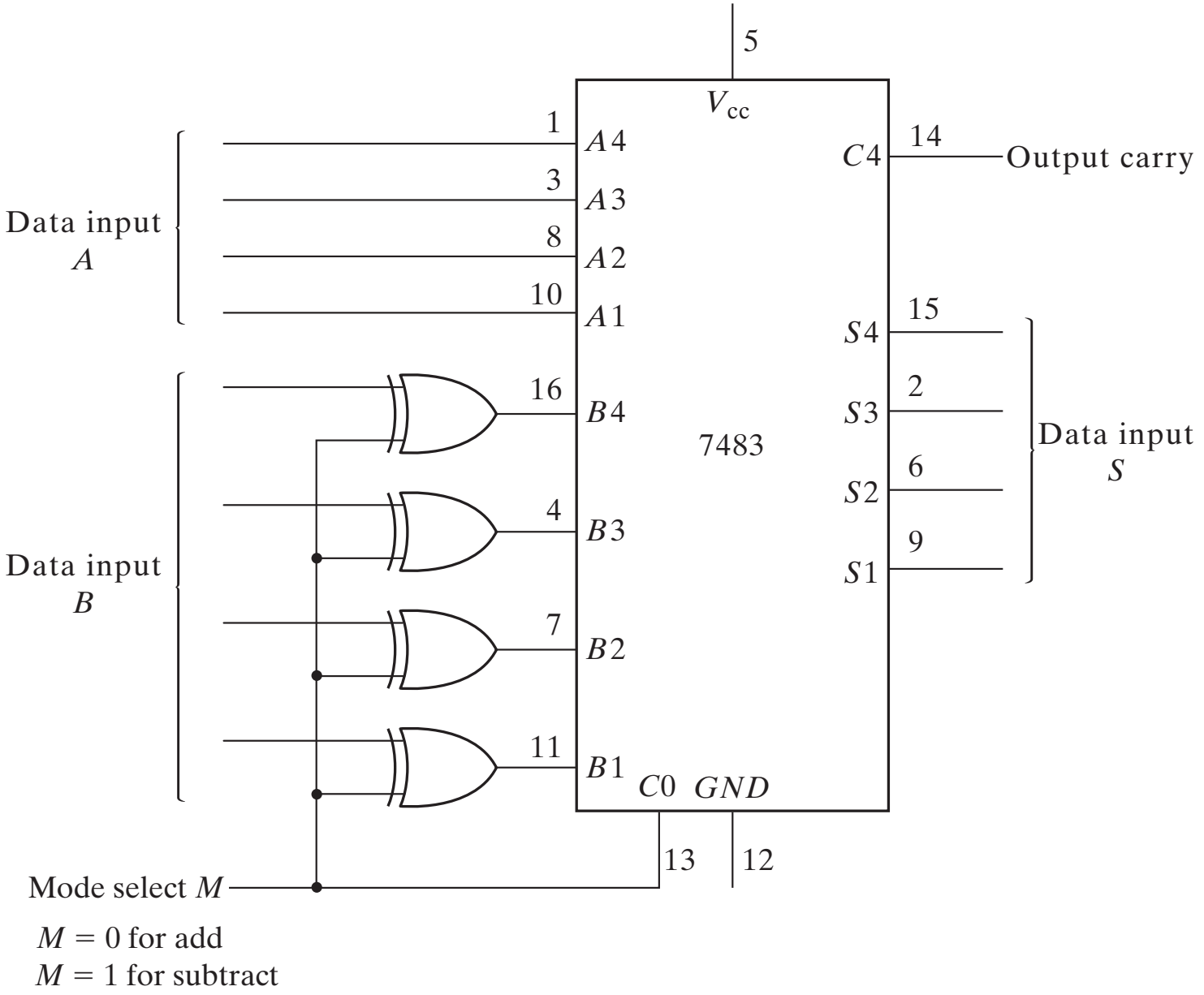
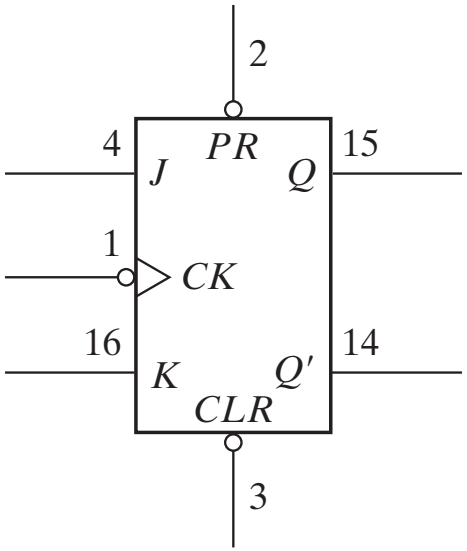
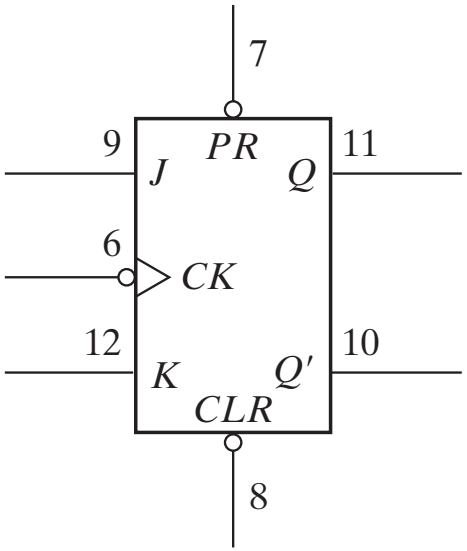


Fig. 11-11 4-Bit Adder–Subtractor



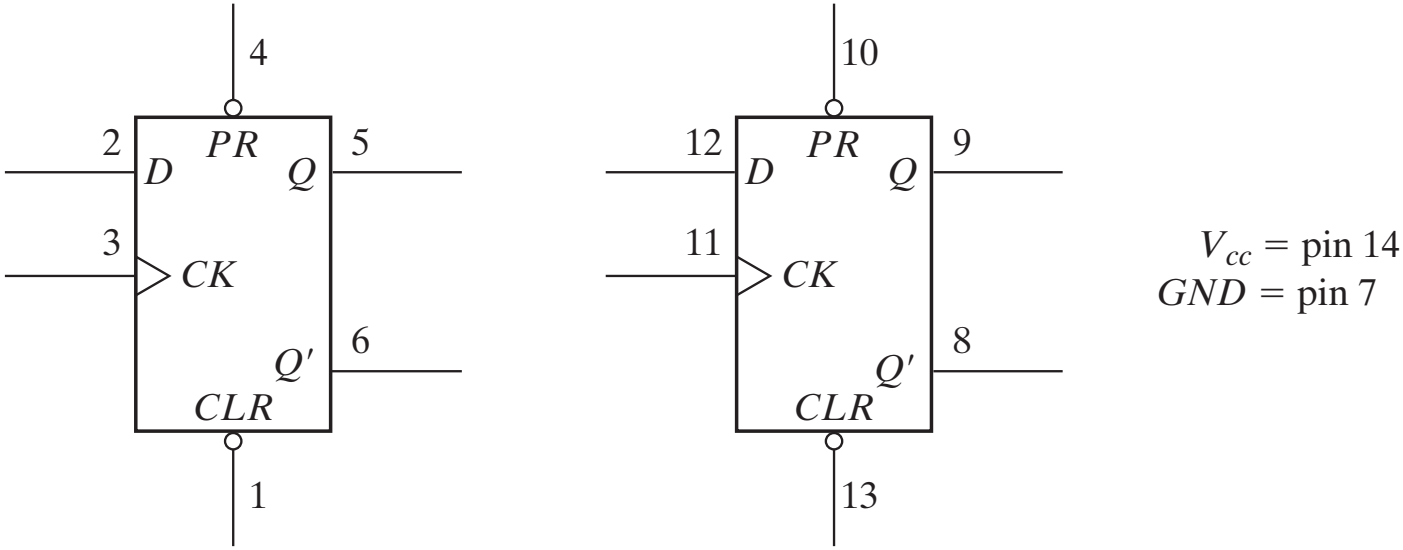


V_{cc} = pin 5
GND = pin 13

Function table

Inputs					Outputs	
Preset	Clear	Clock	J	K	Q	Q'
0	1	X	X	X	1	0
1	0	X	X	X	0	1
0	0	X	X	X	1	1
1	1	⊓	0	0	No change	
1	1	⊓	0	1	0	1
1	1	⊓	1	0	1	0
1	1	⊓	1	1	Toggle	

Fig. 11-12 IC Type 7476 Dual *JK* Master–Slave Flip-Flops



Function table

Inputs				Outputs	
Preset	Clear	Clock	D	Q	Q'
0	1	X	X	1	0
1	0	X	X	0	1
0	0	X	X	1	1
1	1	↑	0	0	1
1	1	↑	1	1	0
1	1	0	X	No change	

Fig. 11-13 IC Type 7474 Dual D Positive–Edge-Triggered Flip-Flops

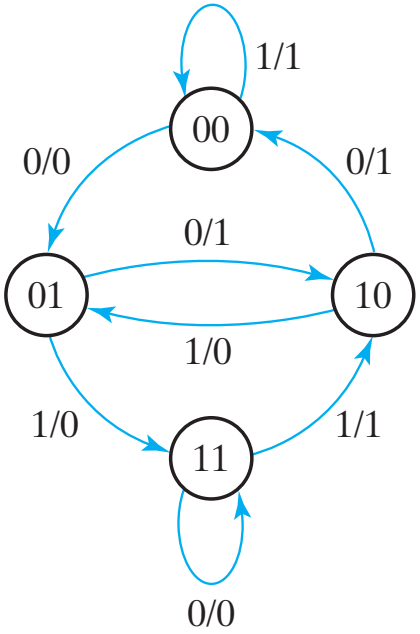
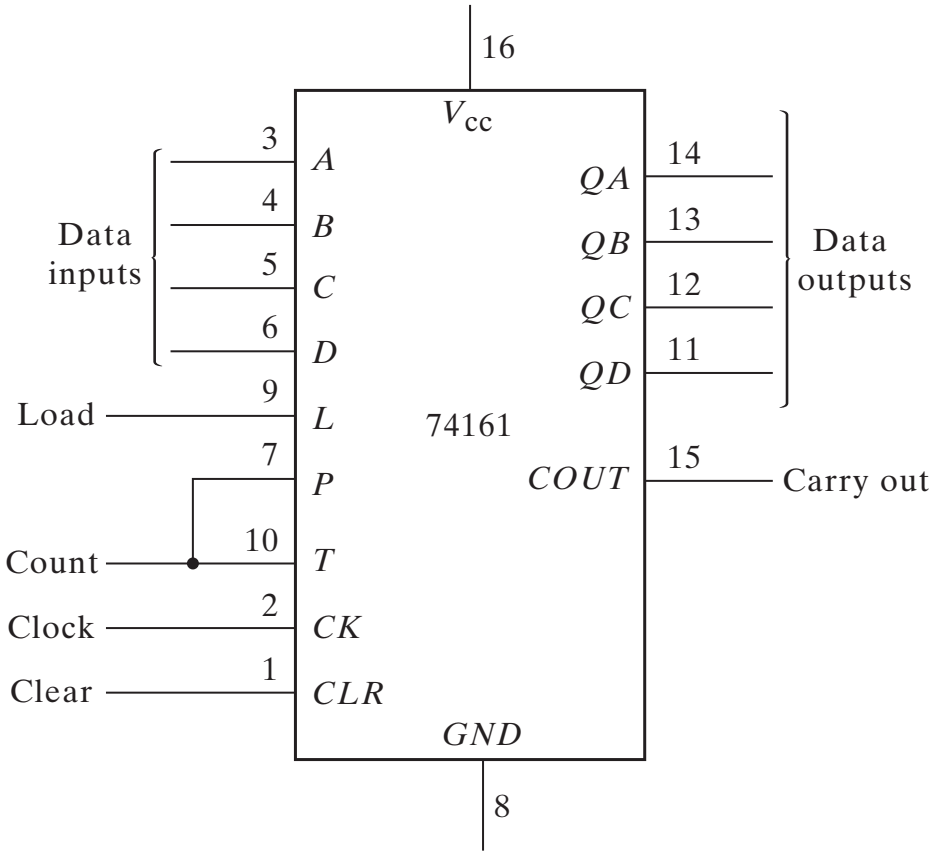


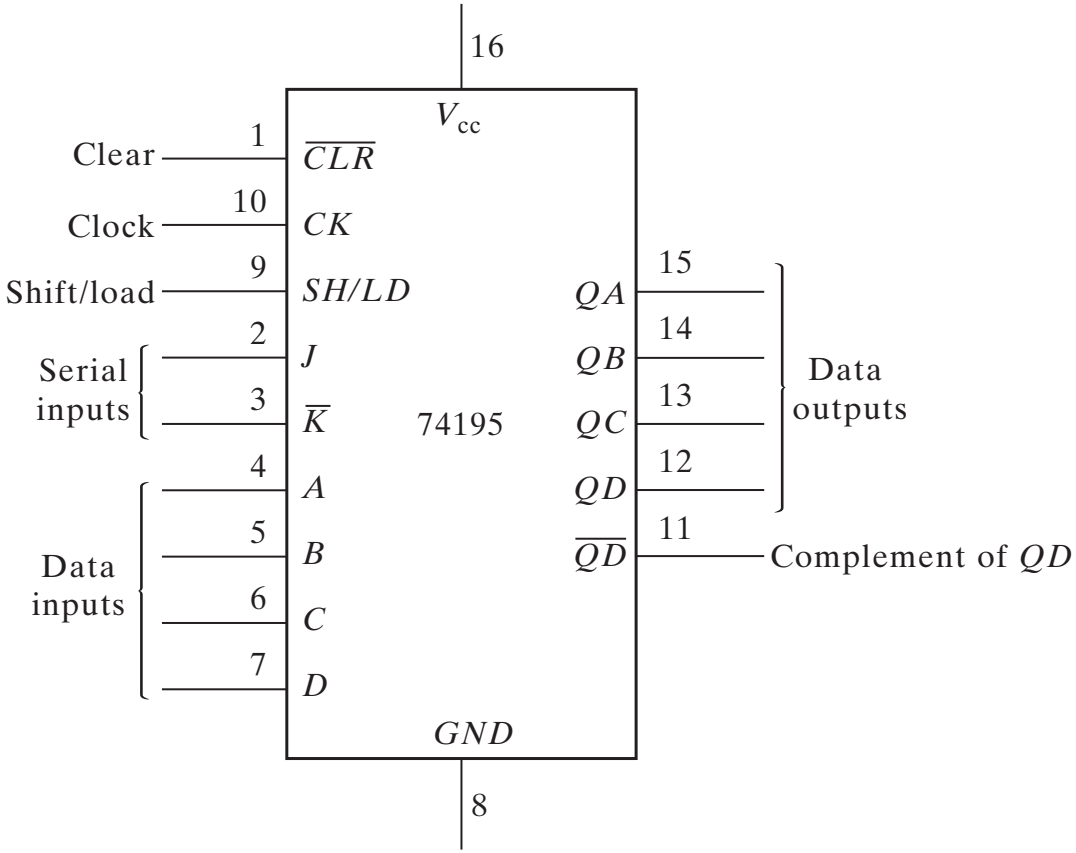
Fig. 11-14 State Diagram for Experiment 9



Function table

Clear	Clock	Load	Count	Function
0	X	X	X	Clear outputs to 0
1	↑	0	X	Load input data
1	↑	1	1	Count to next binary value
1	↑	1	0	No change in output

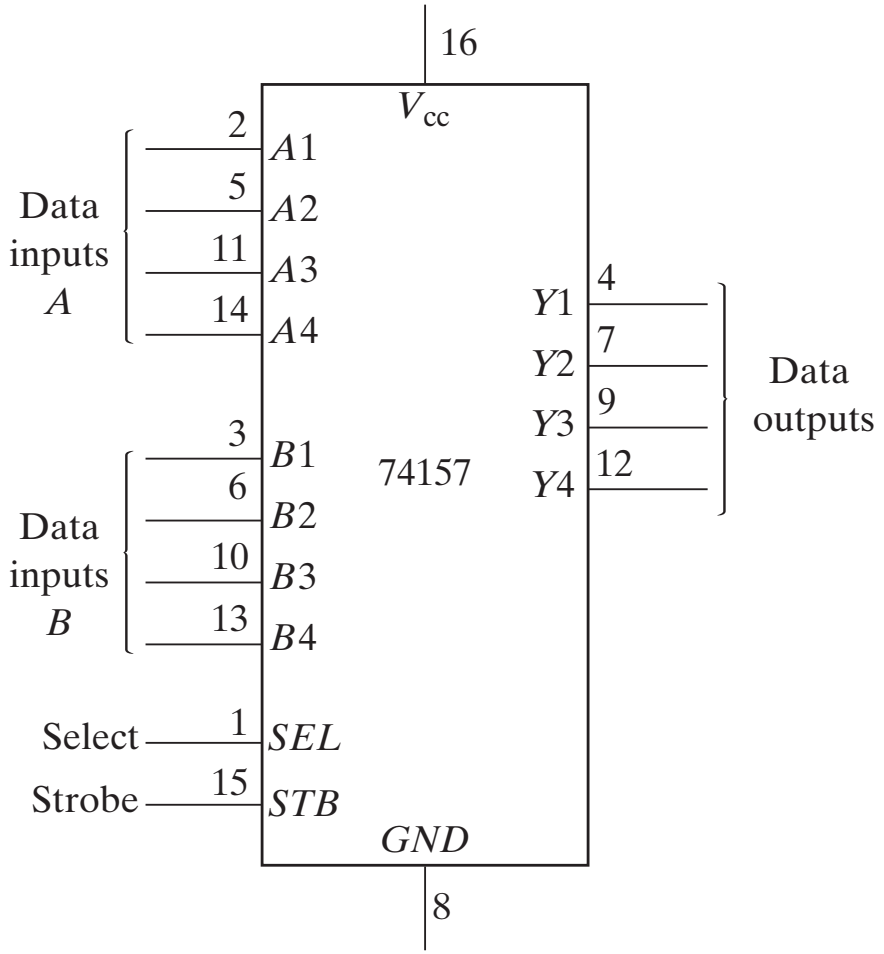
Fig. 11-15 IC Type 74161 Binary Counter with Parallel Load



Function table

Clear	Shift/ load	Clock	J	$\overline{K}$	Serial input	Function
0	X	X	X	X	X	Asynchronous clear
1	X	0	X	X	X	No change in output
1	0	↑	X	X	X	Load input data
1	1	↑	0	0	0	Shift from QA toward QD, $QA = 0$
1	1	↑	1	1	1	Shift from QA toward QD, $QA = 1$

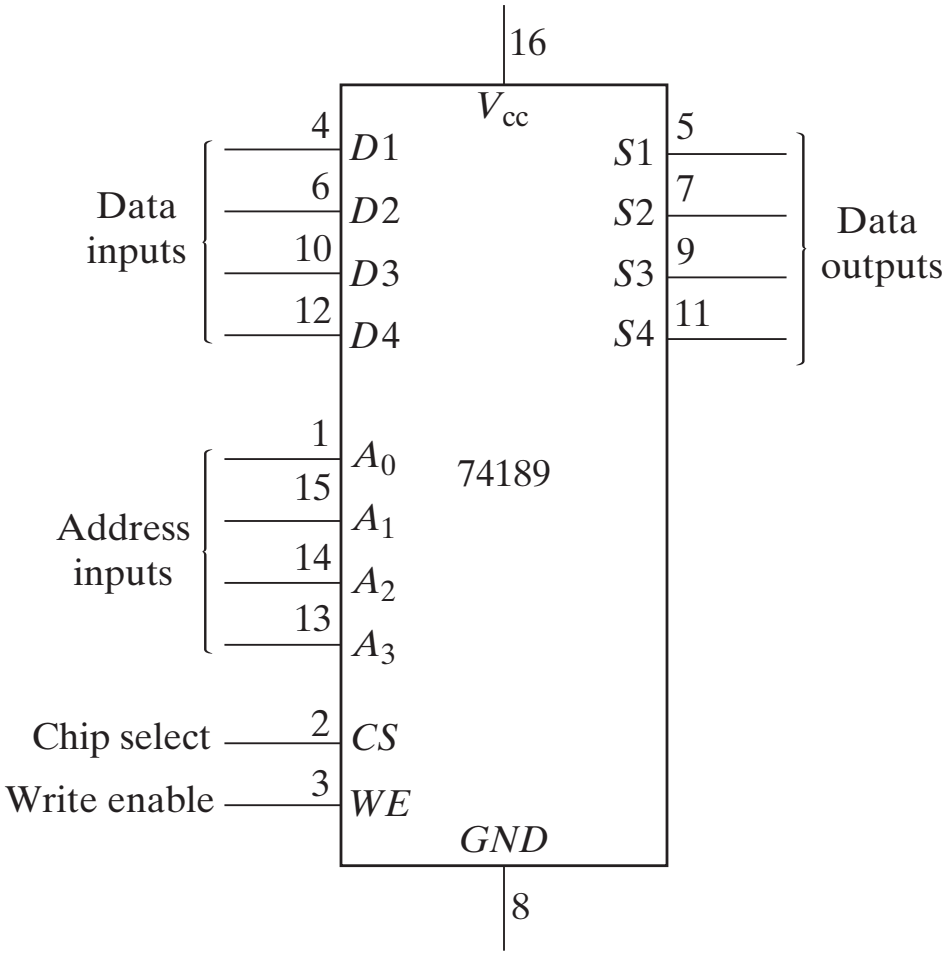
Fig. 11-16 IC Type 74195 Shift Register with Parallel Load



Function table

Strobe	Select	Data outputs Y
1	X	All 0's
0	0	Select data inputs A
0	1	Select data inputs B

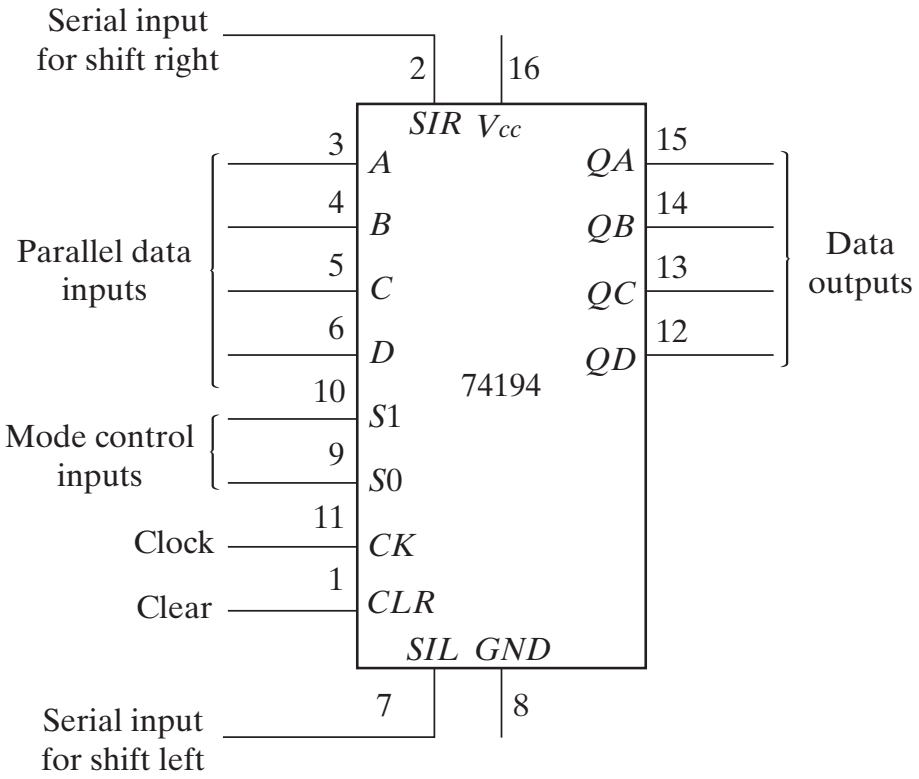
Fig. 11-17 IC Type 74157 Quadruple 2 × 1 Multiplexers



Function table

CS	WE	Operation	Data outputs
0	0	Write	High impedance
0	1	Read	Complement of selected word
1	X	Disable	High impedance

Fig. 11-18 IC Type 74189 16 × 4 RAM



Function table

Clear	Clock	Mode $S1$	Mode $S0$	Function
0	X	X	X	Clear outputs to 0
1	↑	0	0	No change in output
1	↑	0	1	Shift right in the direction from QA to QD. SIR to QA
1	↑	1	0	Shift left in the direction from QD to QA. SIL to QD
1	↑	1	1	Parallel-load input data

Fig. 11-19 IC Type 74194 Bidirectional Shift Register with Parallel Load

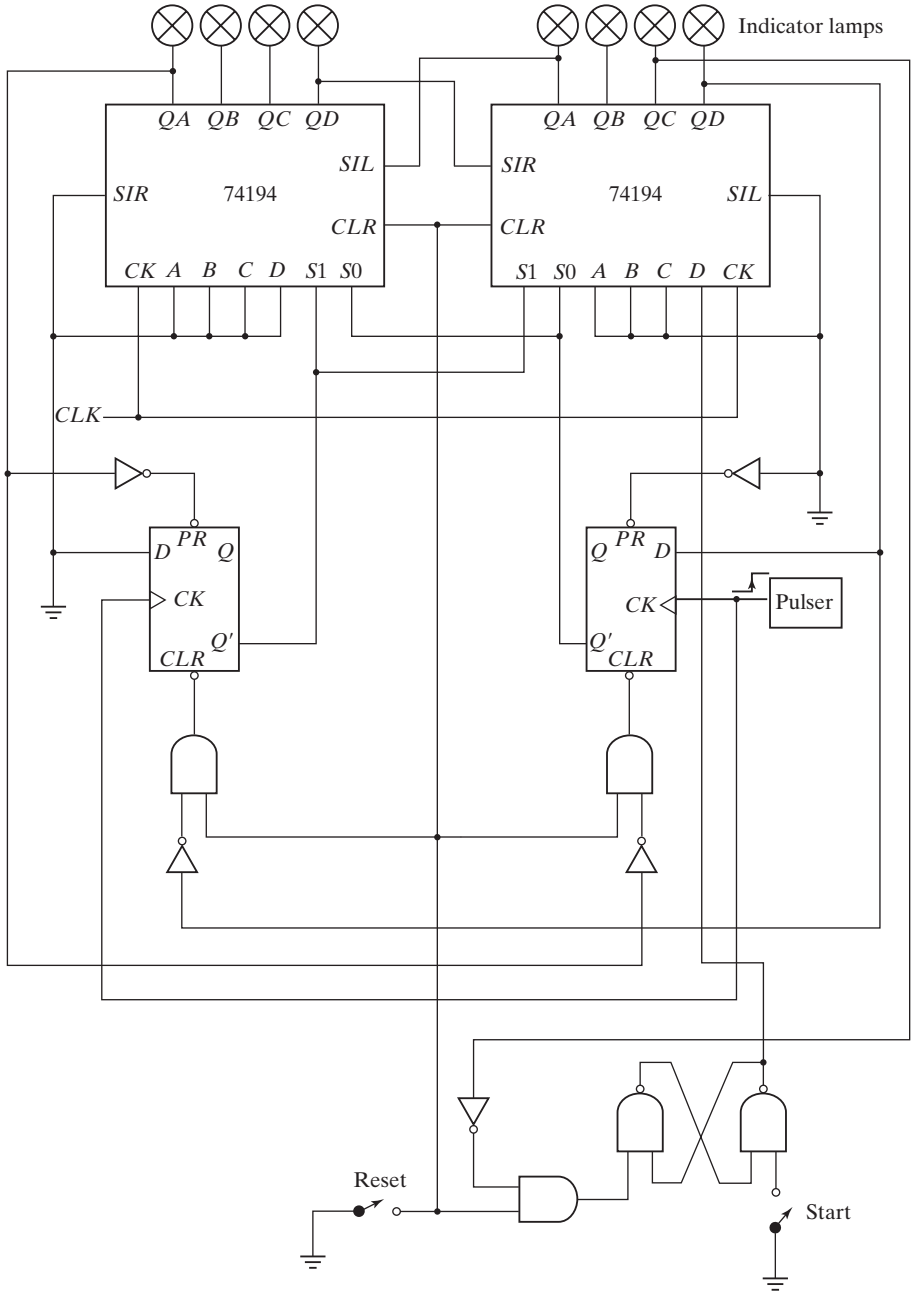


Fig. 11-20 Lamp Handball Logic Diagram

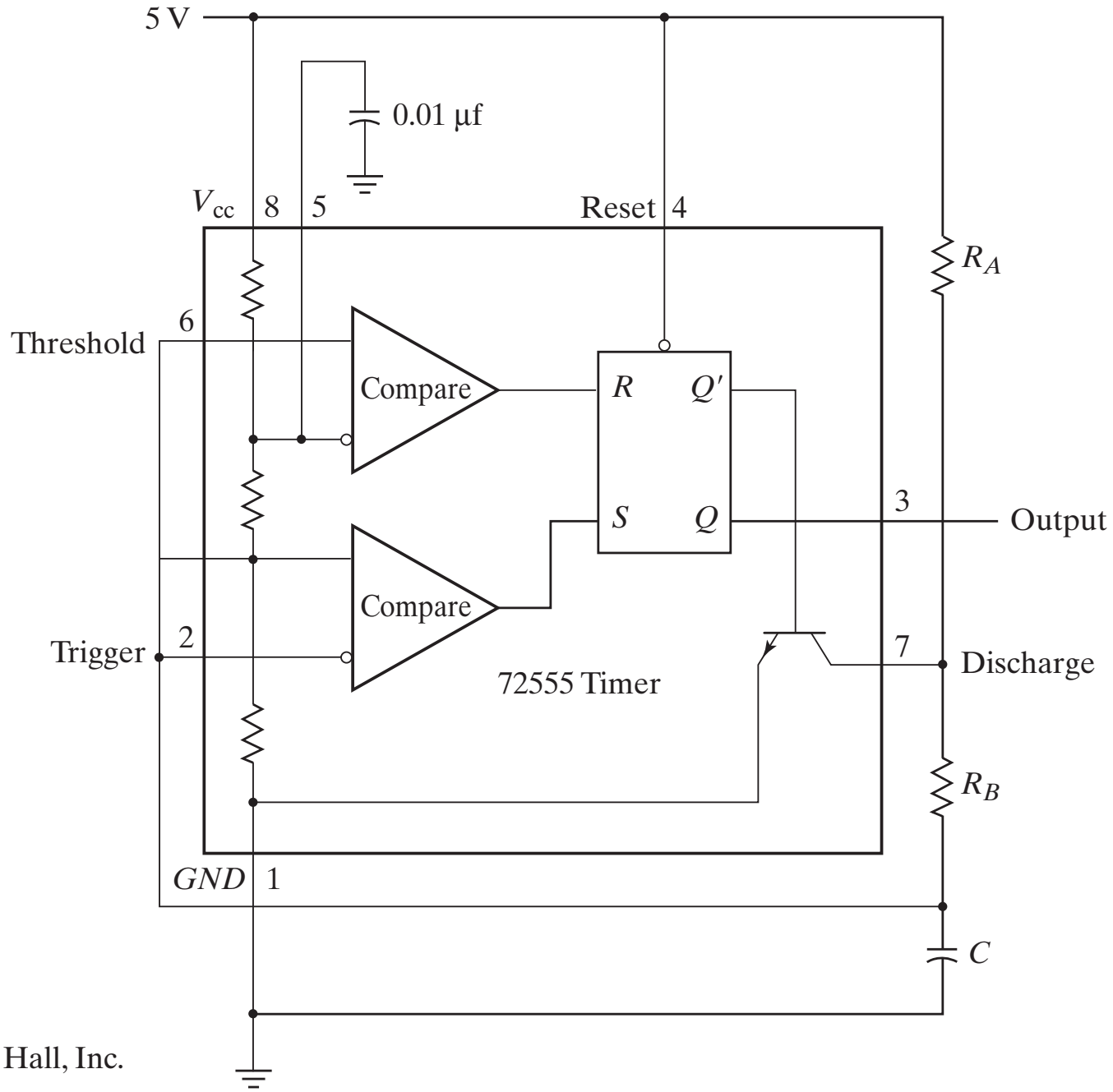


Fig. 11-21 IC Type 72555 Timer Connected as a Clock-Pulse Generator

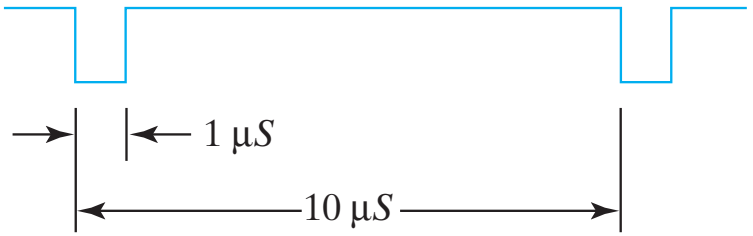


Fig. 11-22 Output Waveform for Clock Generator

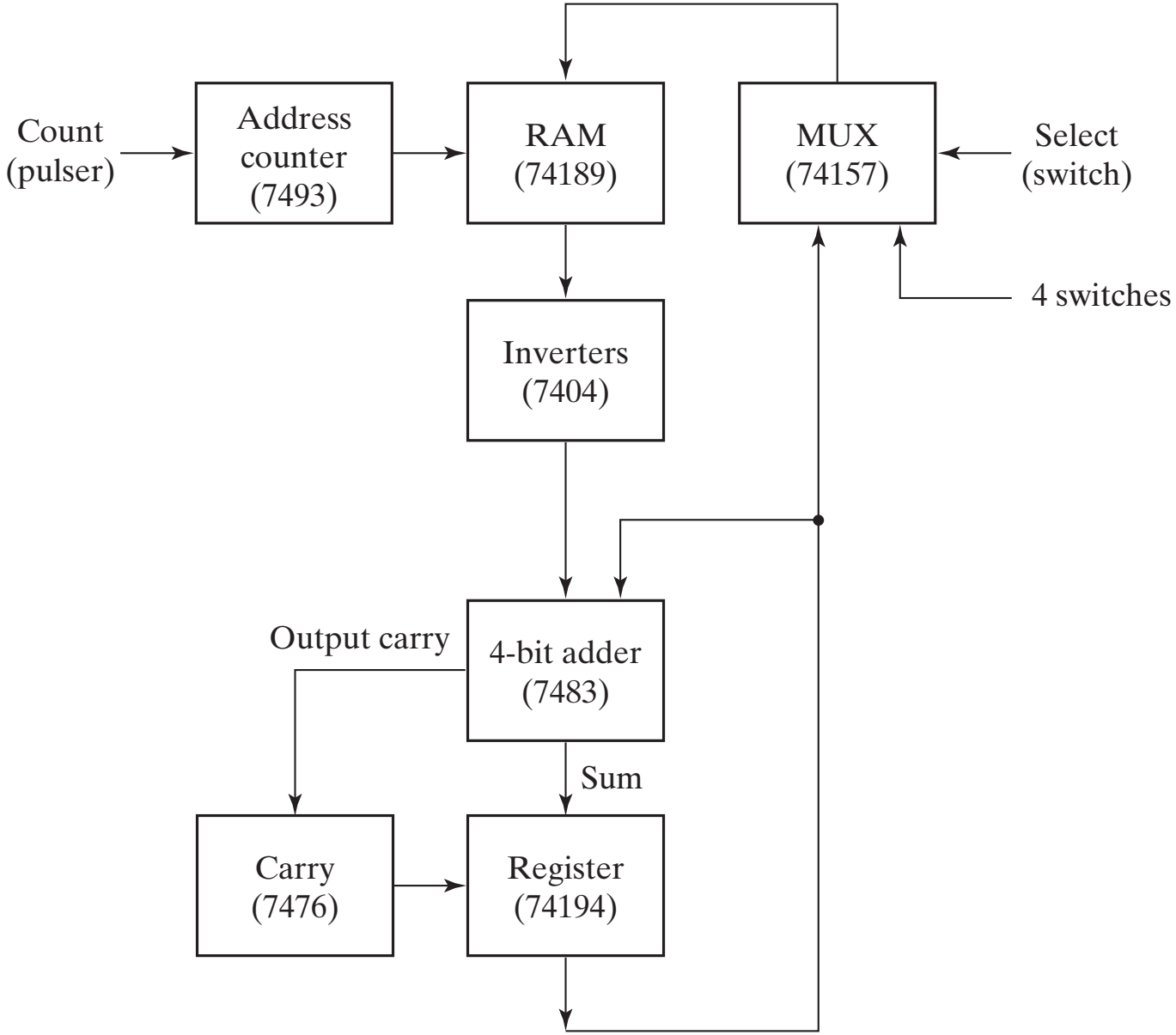
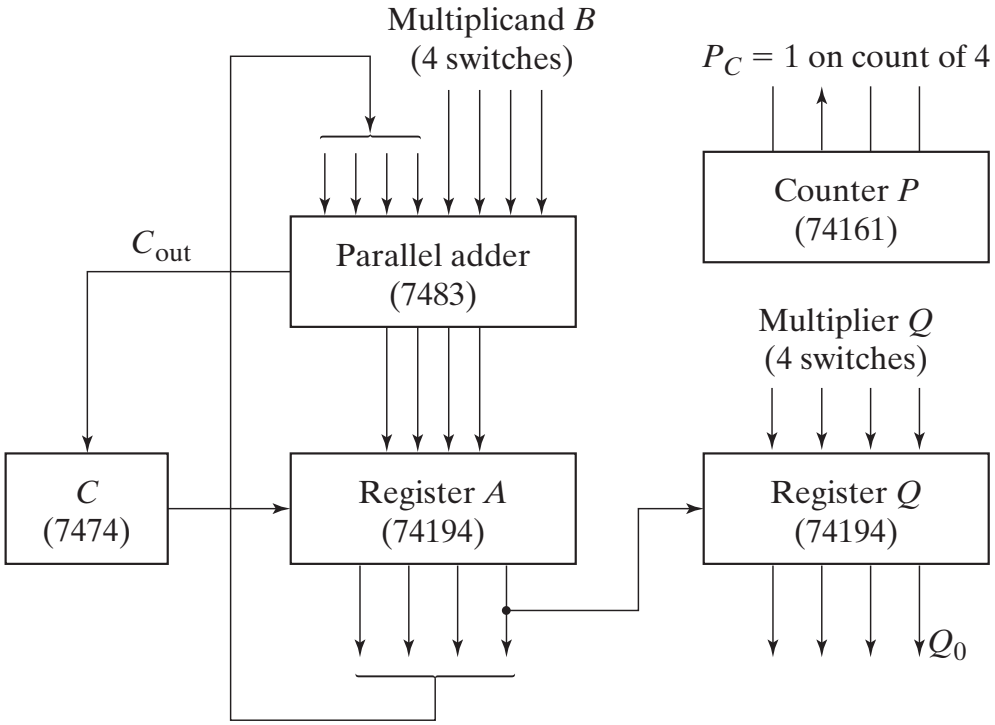
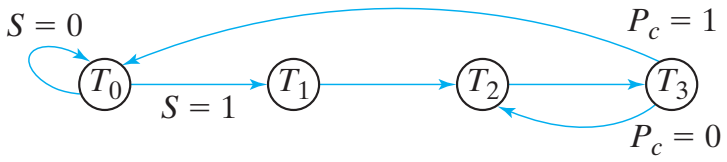


Fig. 11-23 Block Diagram of a Parallel Adder for Experiment 16



(a) Datapath block program



T_1: $A \leftarrow 0, C \leftarrow 0, P \leftarrow 0, Q \leftarrow$ Multiplier
T_2: $P \leftarrow P + 1$
T_2Q_0: $A \leftarrow A + B, C \leftarrow C_{out}$
T_3: Shift right CAQ, C $\leftarrow 0$

(b) Control state diagram

Fig. 11-24 Binary Multiplier Circuit