Digital Design
Lecture 8

Combinatorial Logic
(Continued)

Binary Multiplier: 2-bit by 2-bit

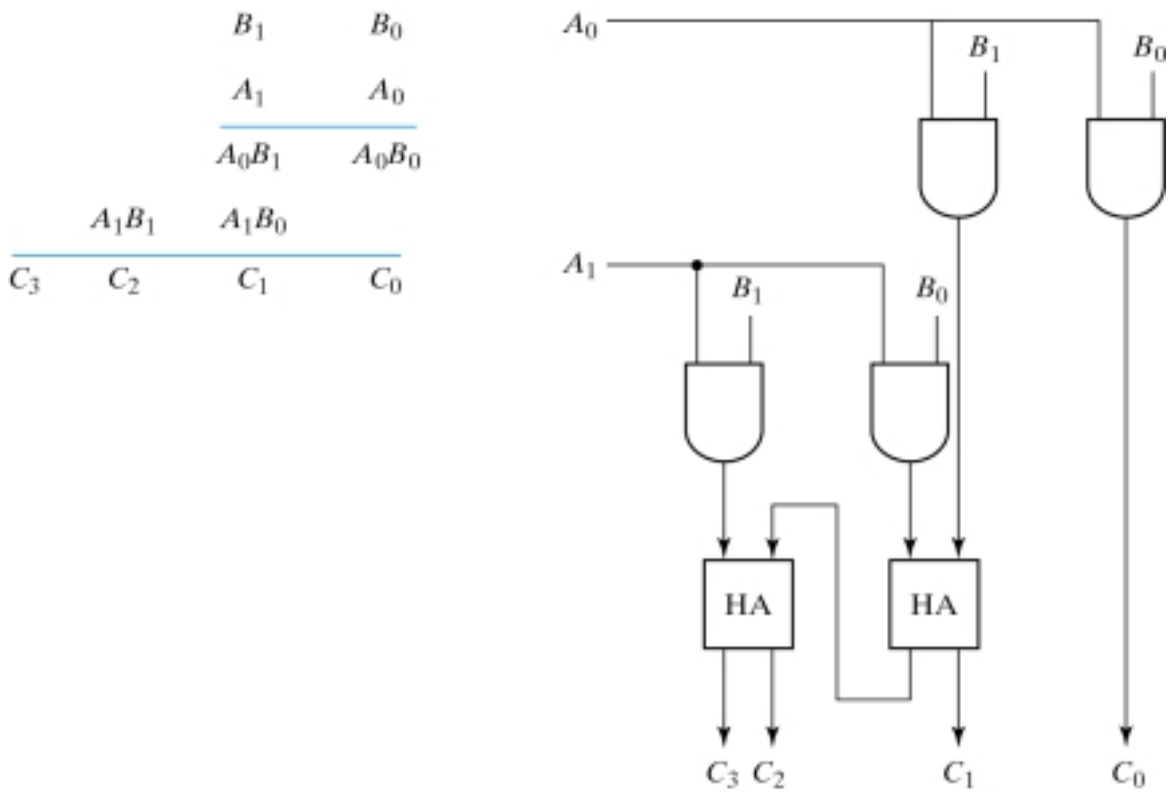


Fig. 4-15 2-Bit by 2-Bit Binary Multiplier

Binary Multiplier: 4-bit by 3-bit

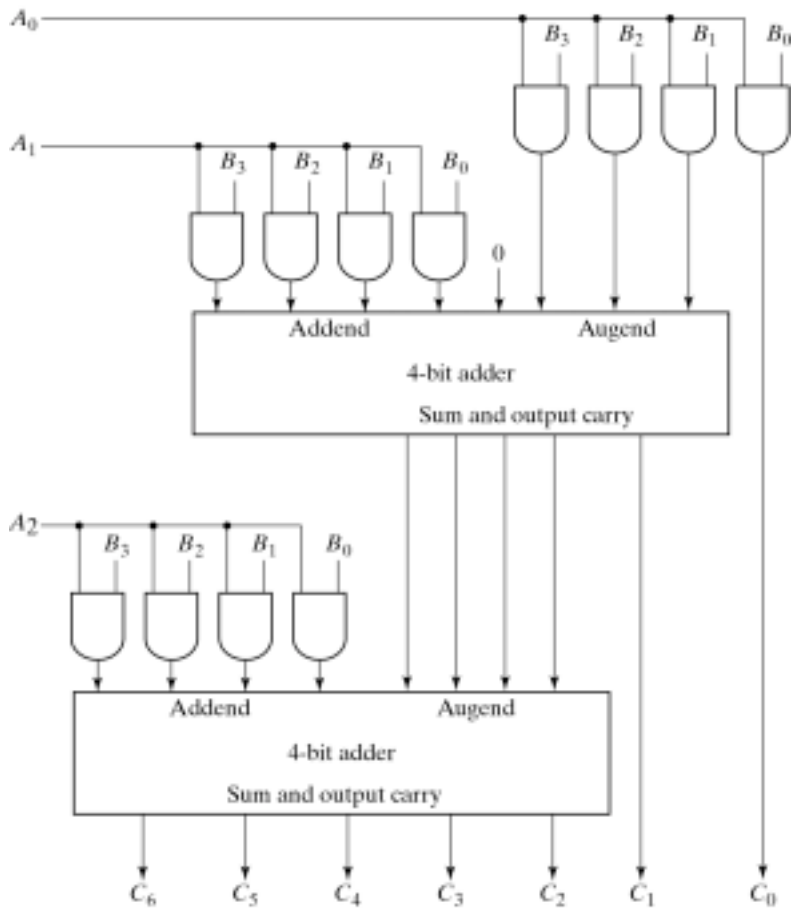


Fig. 4-16 4-Bit by 3-Bit Binary Multiplier

4-Bit Magnitude Comparator

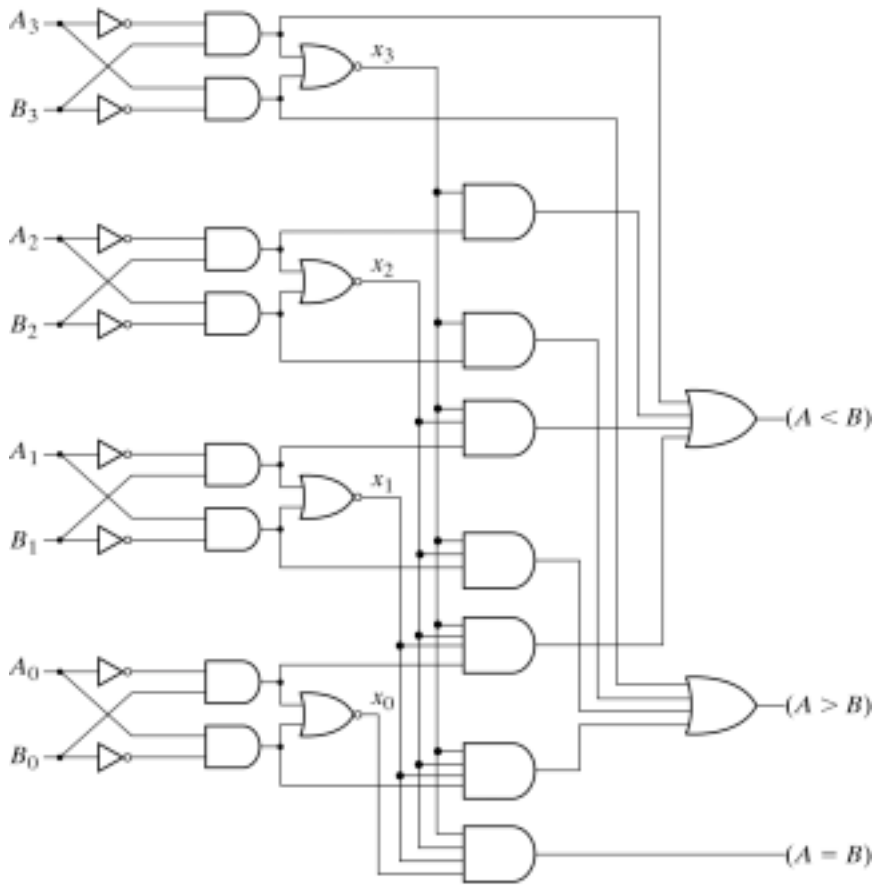


Fig. 4-17 4-Bit Magnitude Comparator

3-to-8 Line Decoder

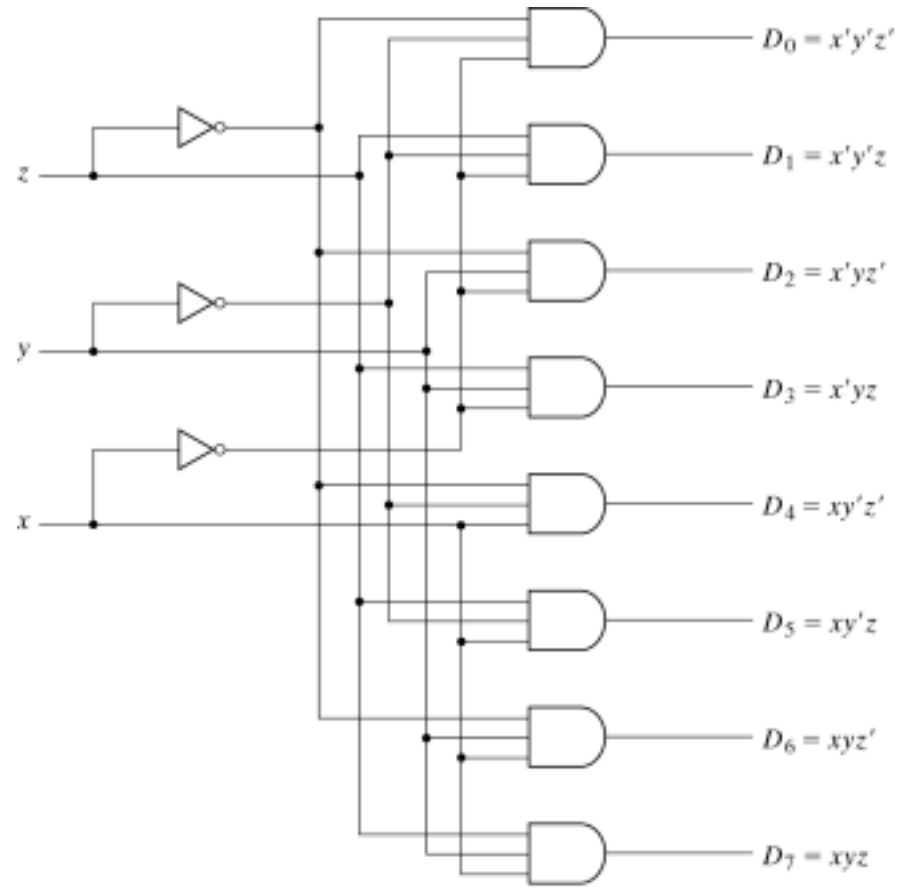
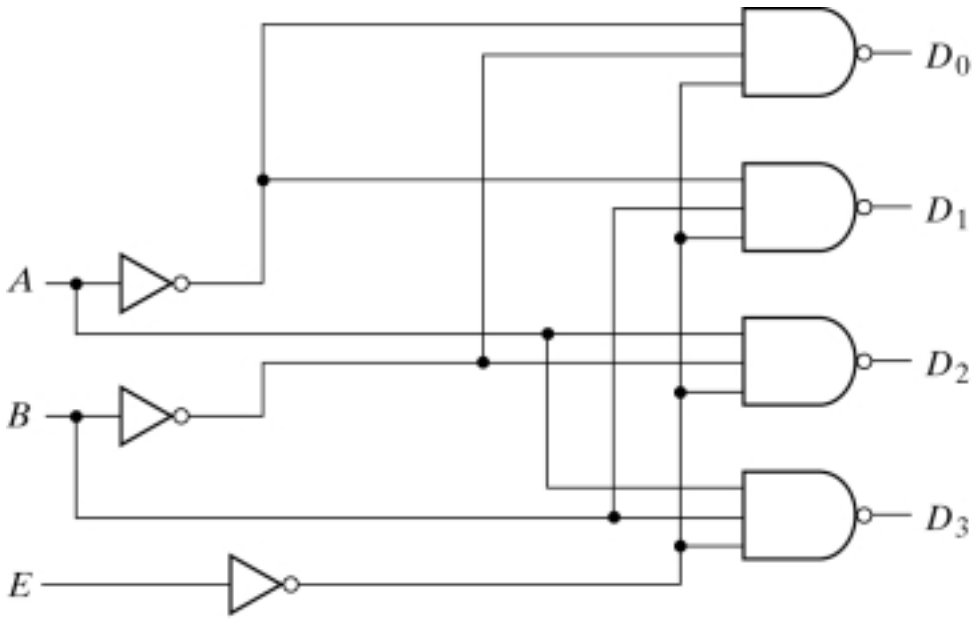


Fig. 4-18 3-to-8-Line Decoder

2-to-4 Line Decoder with Enable



(a) Logic diagram

E	A	B	D_0	D_1	D_2	D_3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

(b) Truth table

Fig. 4-19 2-to-4-Line Decoder with Enable Input

Building Large Decoders

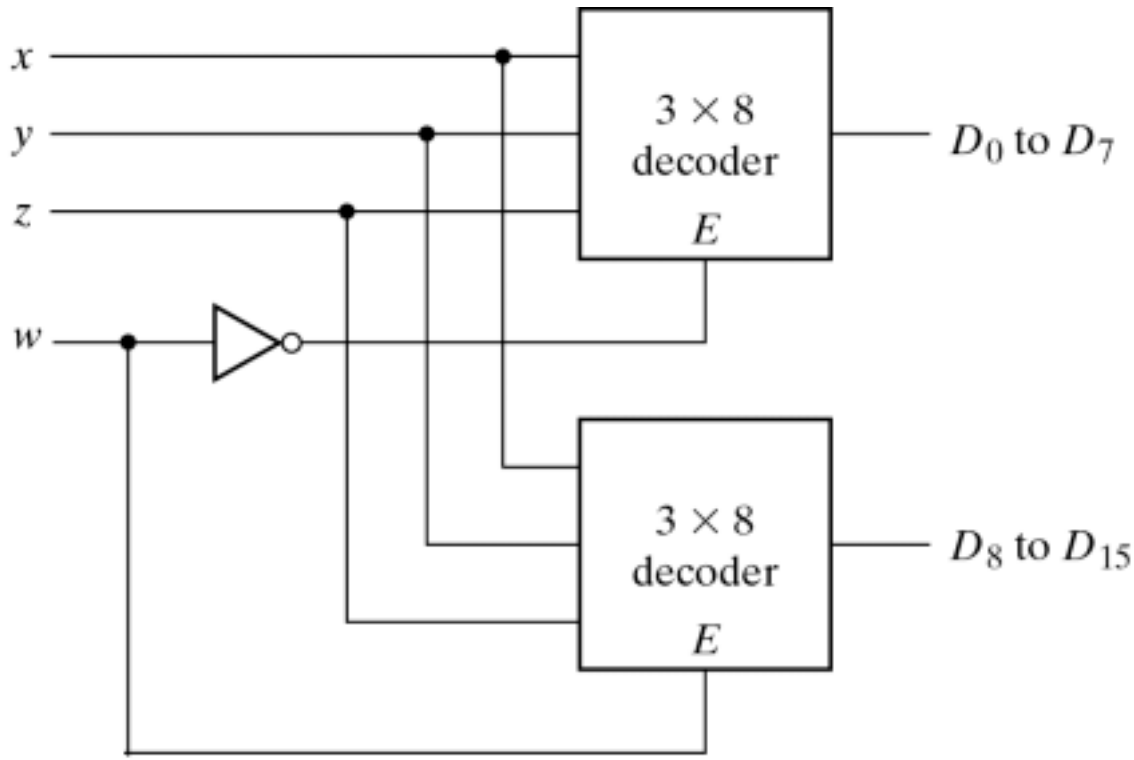


Fig. 4-20 4 × 16 Decoder Constructed with Two 3 × 8 Decoders

Full Adder Via a Decoder

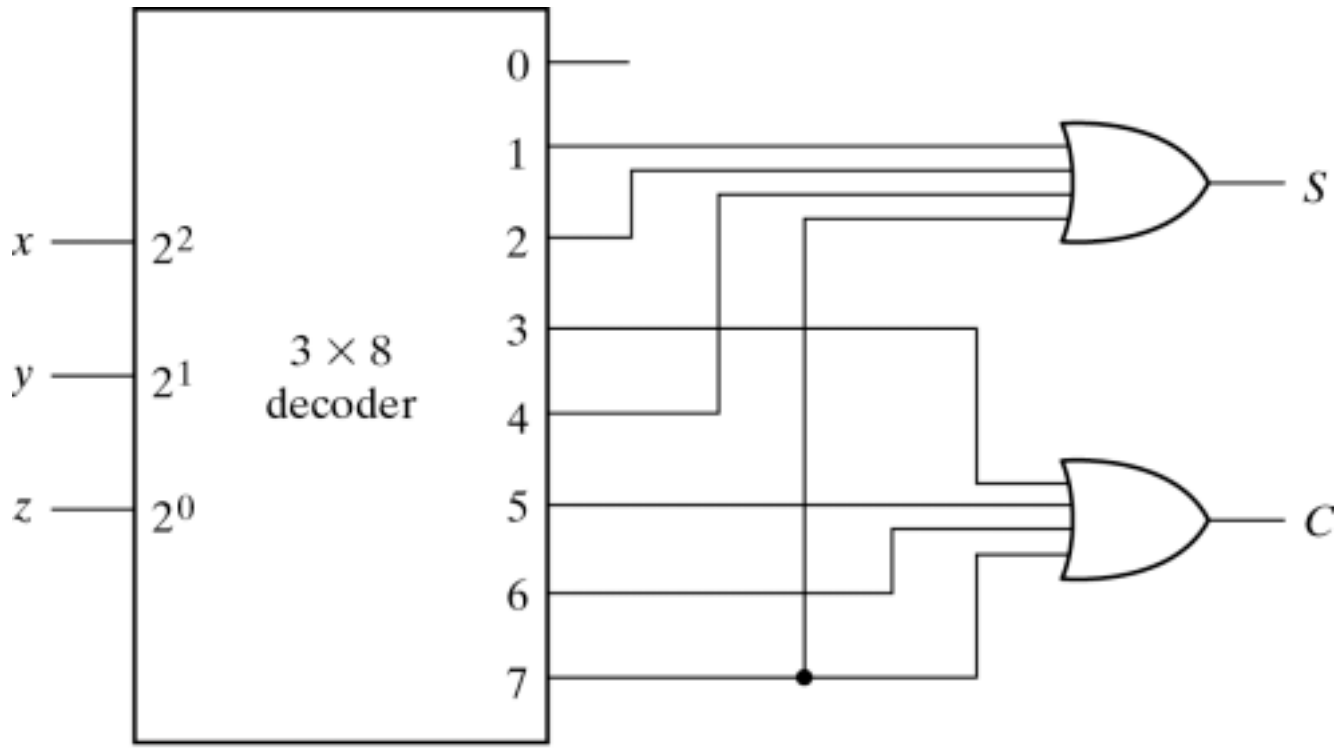


Fig. 4-21 Implementation of a Full Adder with a Decoder

Priority Encoder

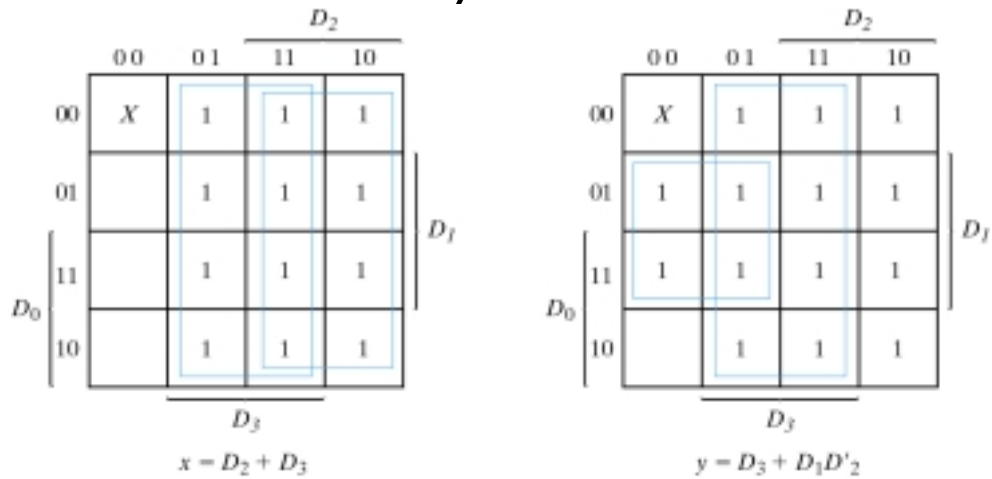


Fig. 4-22 Maps for a Priority Encoder

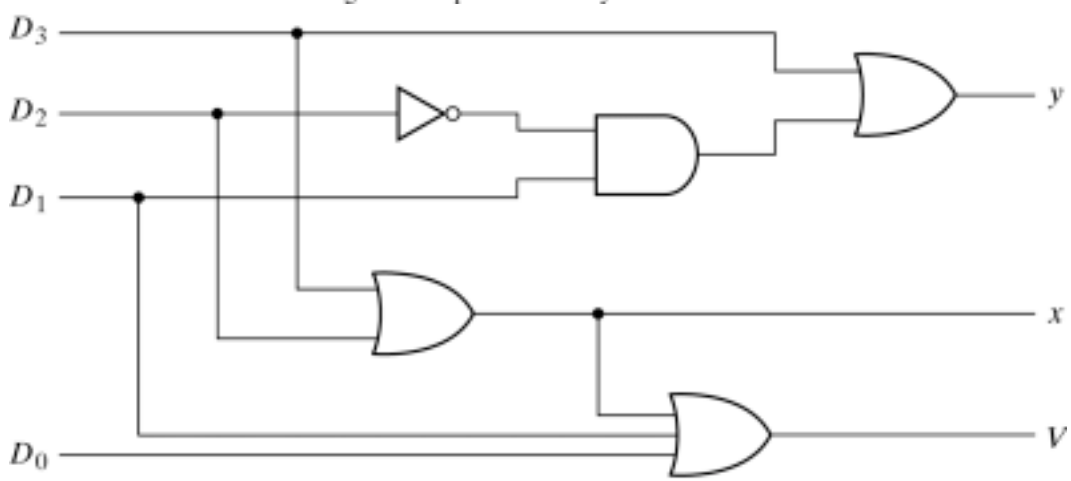
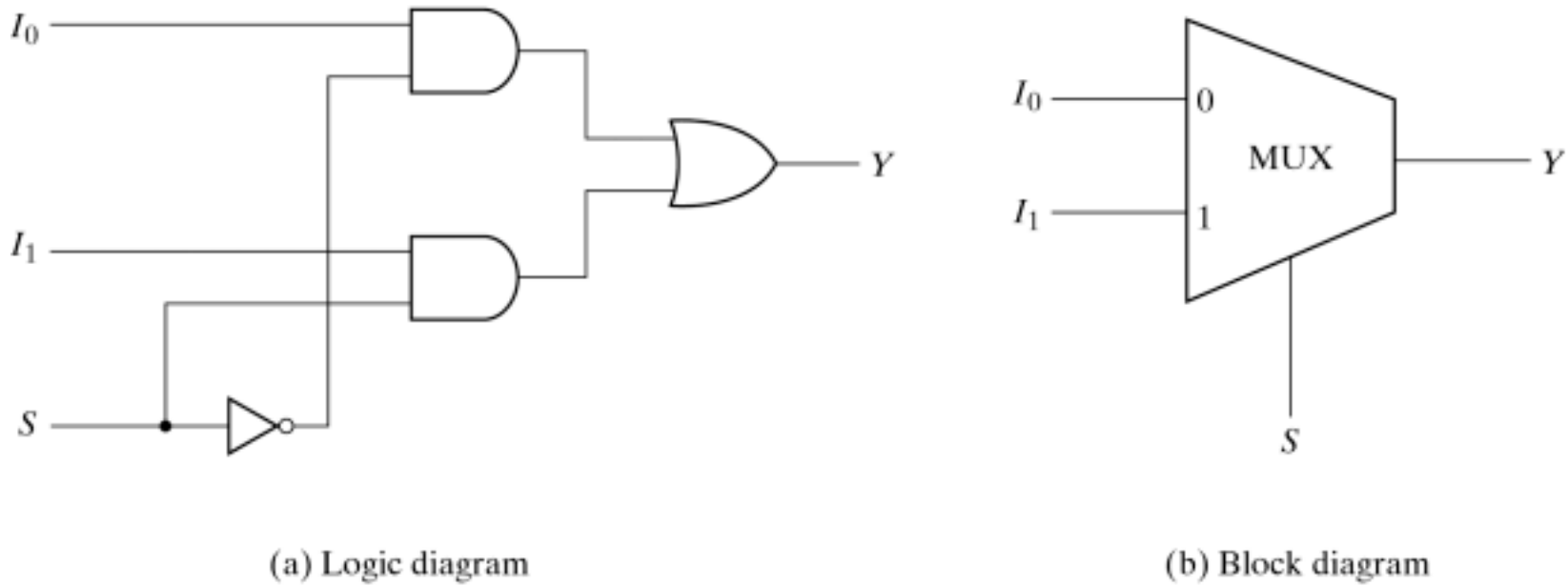


Fig. 4-23 4-Input Priority Encoder

2-to-1 Line Multiplexer

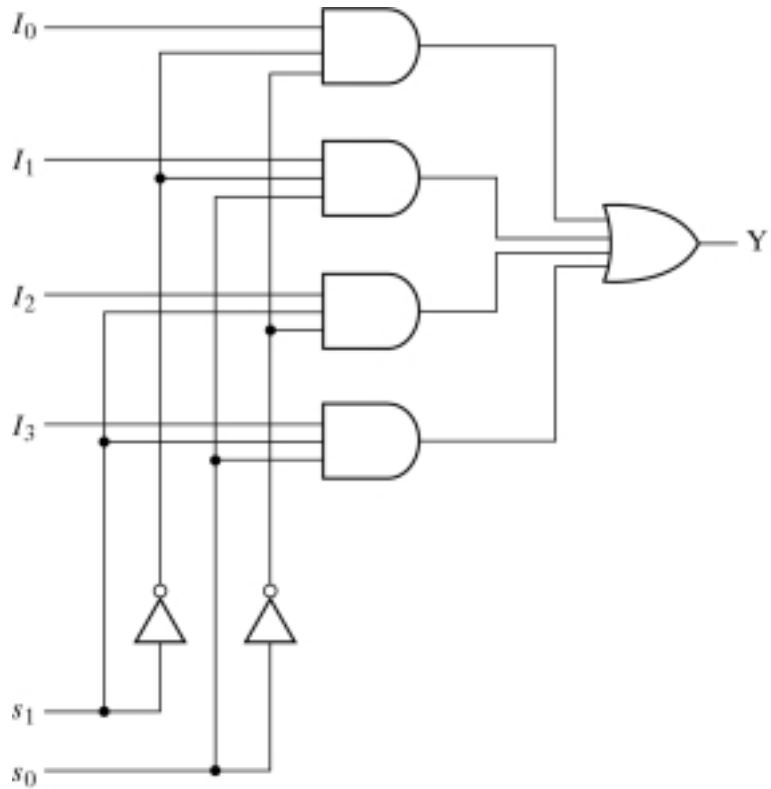


(a) Logic diagram

(b) Block diagram

Fig. 4-24 2-to-1-Line Multiplexer

4-to-1 Line Multiplexer



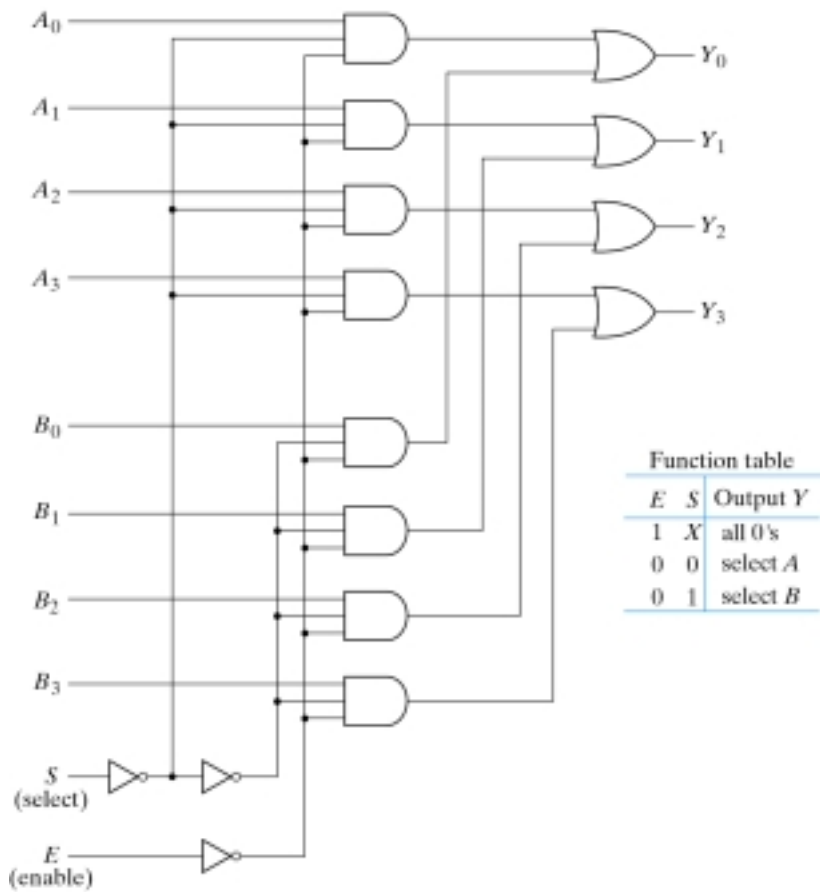
(a) Logic diagram

s_1	s_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

(b) Function table

Fig. 4-25 4-to-1-Line Multiplexer

2-to-1 Line Multiplexer * 4



Function table

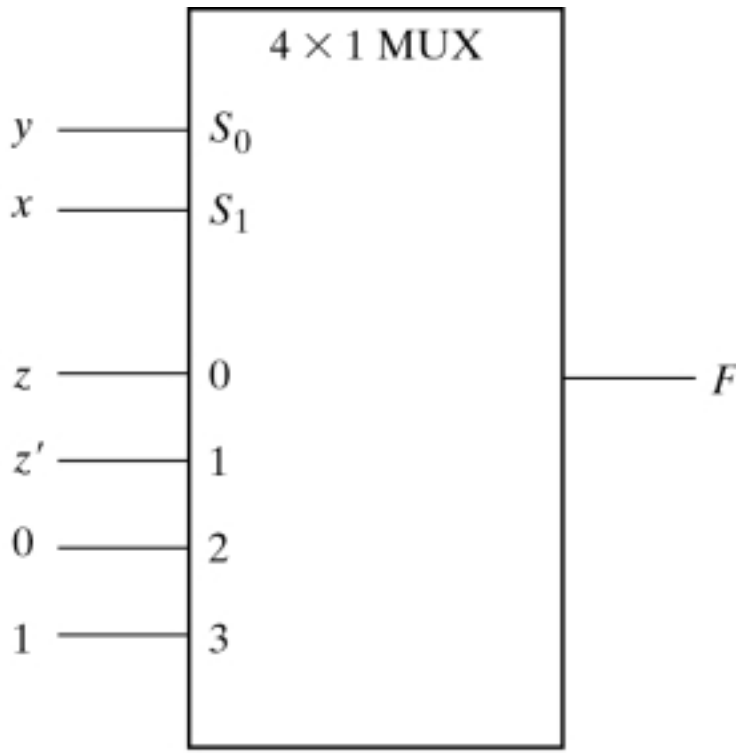
E	S	Output Y
1	X	all 0's
0	0	select A
0	1	select B

Fig. 4-26 Quadruple 2-to-1-Line Multiplexer

Boolean Functions Via a Multiplexer

x	y	z	F	
0	0	0	0	$F = z$
0	0	1	1	
0	1	0	1	$F = z'$
0	1	1	0	
1	0	0	0	$F = 0$
1	0	1	0	
1	1	0	1	$F = 1$
1	1	1	1	

(a) Truth table



(b) Multiplexer implementation

Fig. 4-27 Implementing a Boolean Function with a Multiplexer

A 4-Input Function Via a Multiplexer

A	B	C	D	F	
0	0	0	0	0	$F = D$
0	0	0	1	1	
0	0	1	0	0	$F = D$
0	0	1	1	1	
0	1	0	0	1	$F = D'$
0	1	0	1	0	
0	1	1	0	0	$F = 0$
0	1	1	1	0	
1	0	0	0	0	$F = 0$
1	0	0	1	0	
1	0	1	0	0	$F = D$
1	0	1	1	1	
1	1	0	0	1	$F = 1$
1	1	0	1	1	
1	1	1	0	1	$F = 1$
1	1	1	1	1	

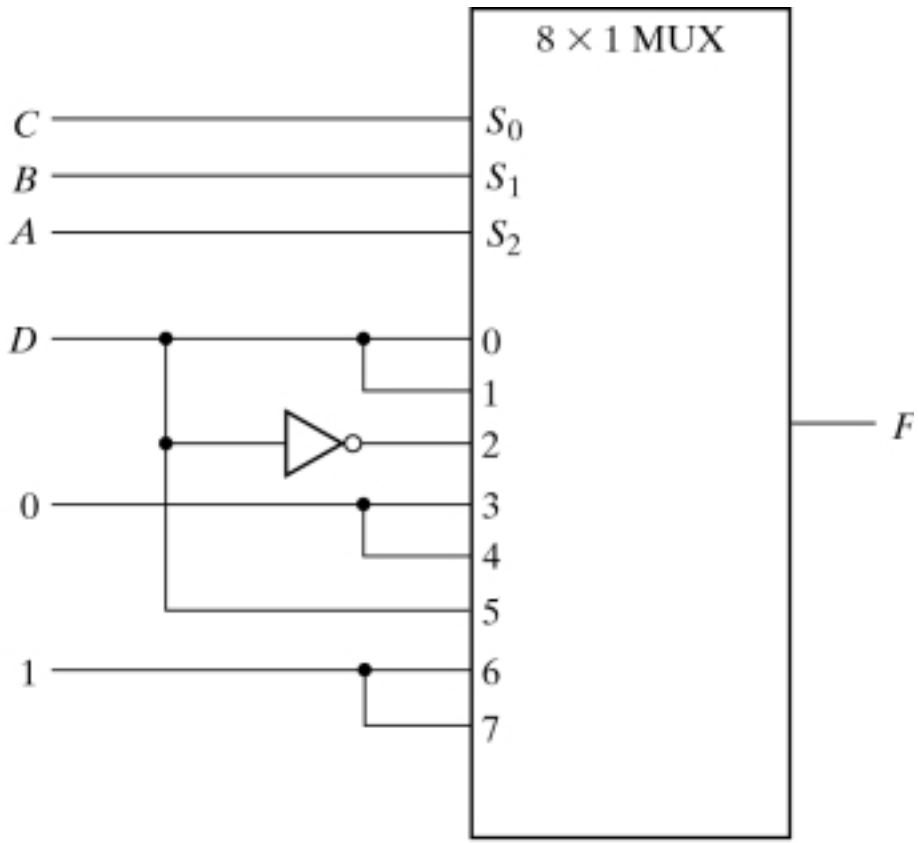


Fig. 4-28 Implementing a 4-Input Function with a Multiplexer

Three State Buffers

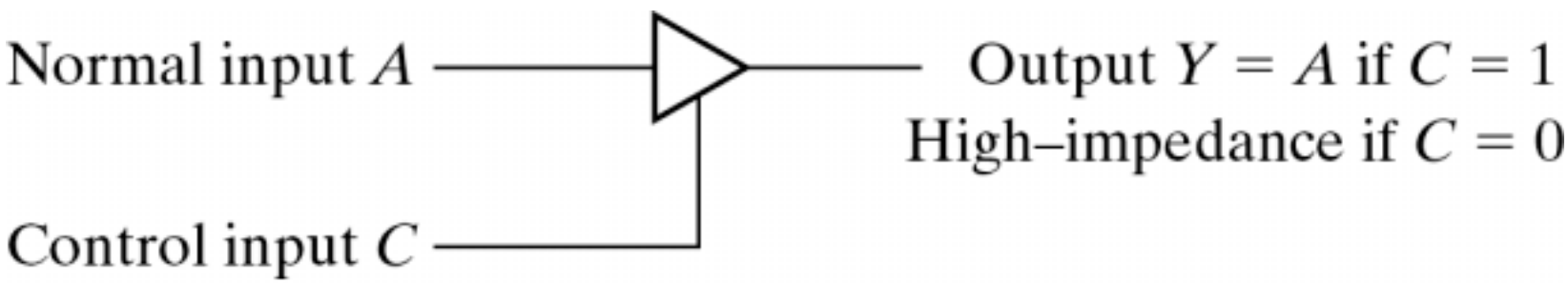
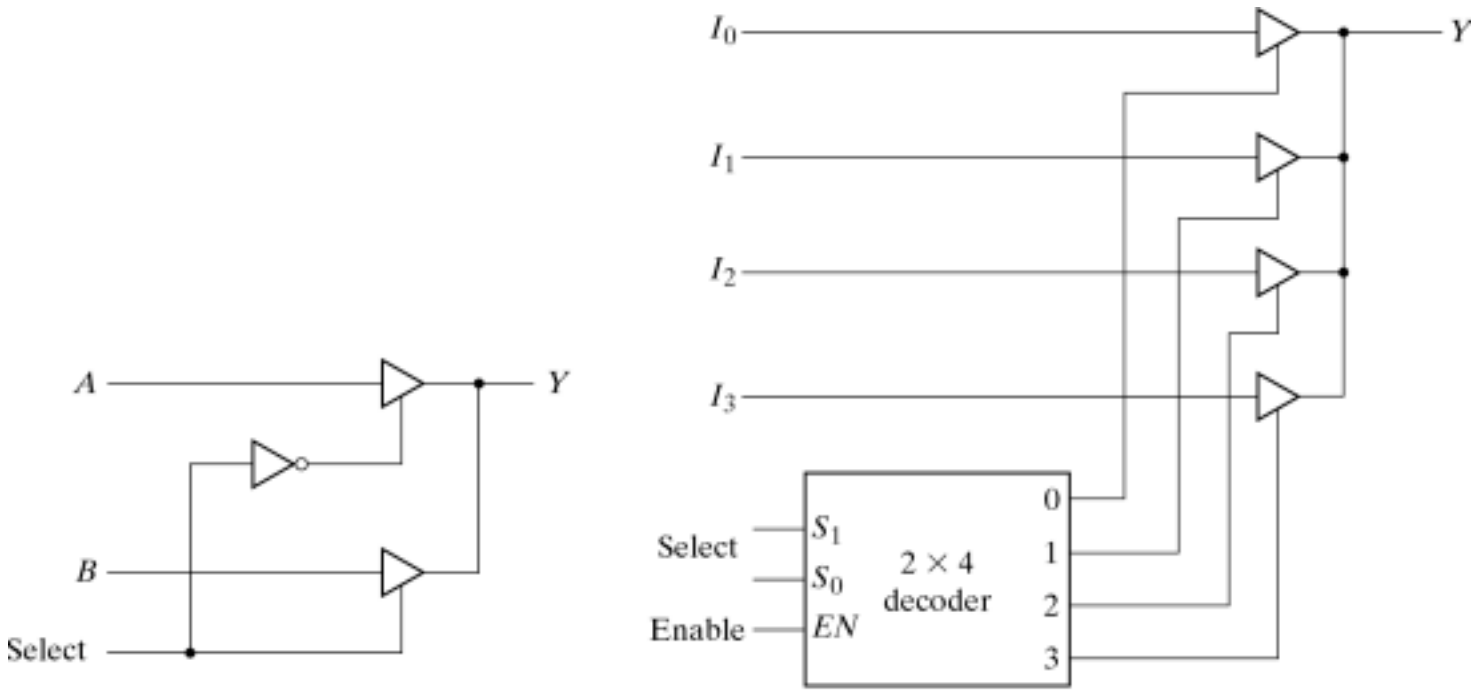


Fig. 4-29 Graphic Symbol for a Three-State Buffer

Multiplexer Via Three-State Gates



(a) 2-to-1- line mux

(b) 4 - to - 1 line mux

Fig. 4-30 Multiplexers with Three-State Gates

Three-State Gates

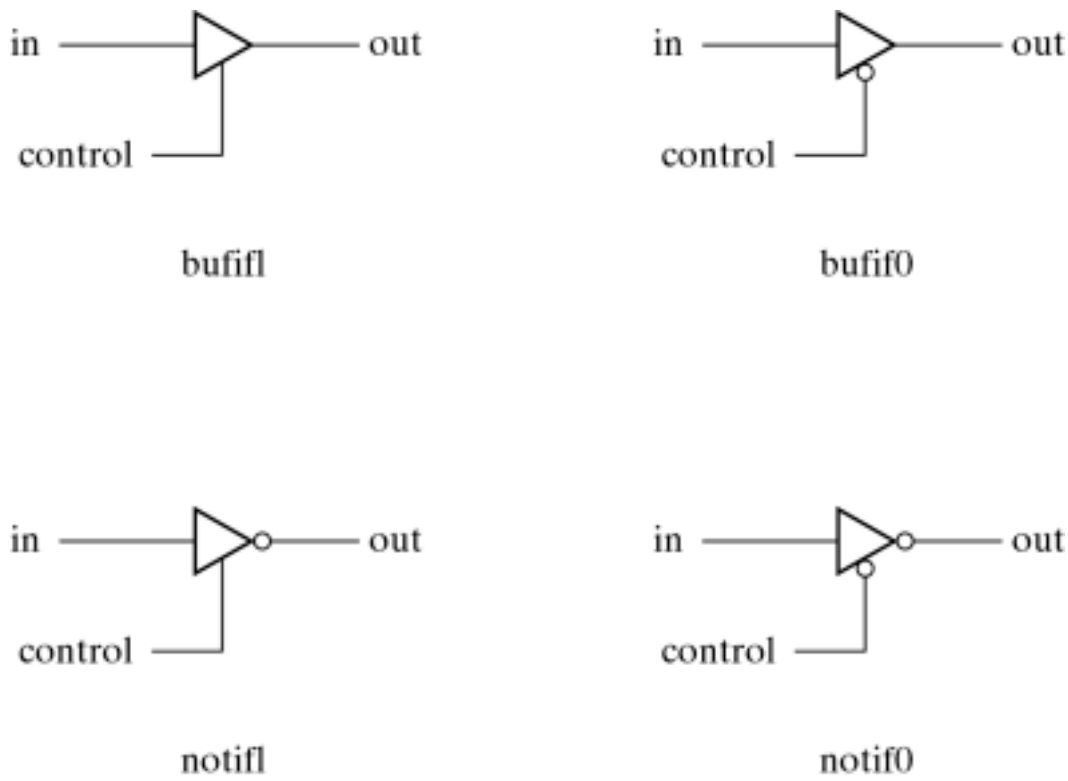


Fig. 4-31 Three-State Gates

A 2-to-1 Line Multiplexer Via Three-State Buffers

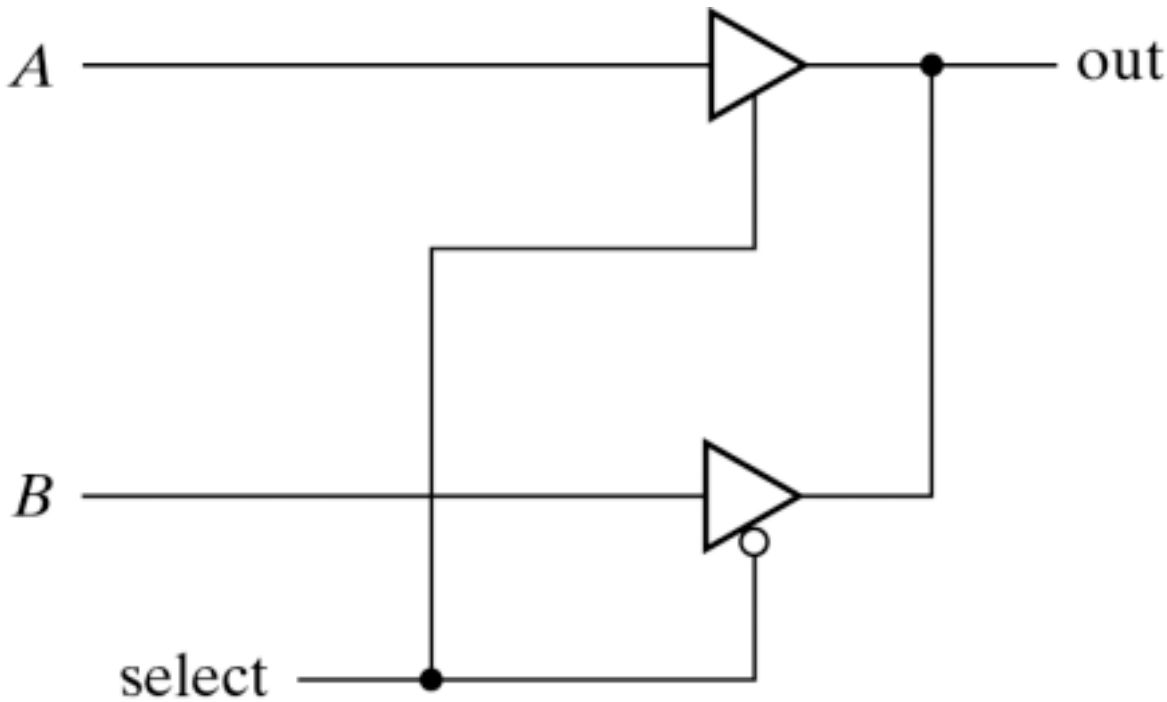


Fig. 4-32 2-to-1-Line Multiplexer with Three-State Buffers

Stimulus and Design Modules Interaction

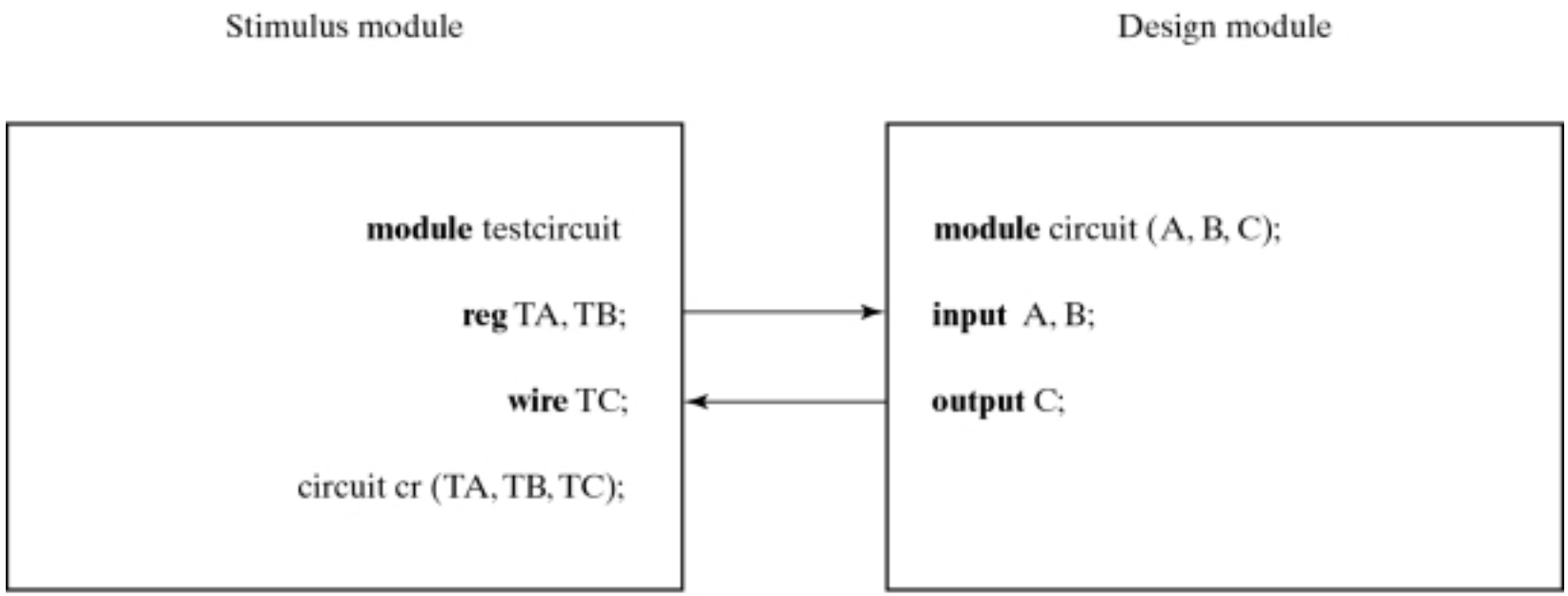


Fig. 4-33 Stimulus and Design Modules Interaction