Digital Design
Lecture 10

Sequential Design

State Reduction

- Equivalent Circuits
  - Identical input sequence
  - Identical output sequence
- Equivalent States
  - Same input ⇒ same output
  - Same input ⇒ same or equivalent next state

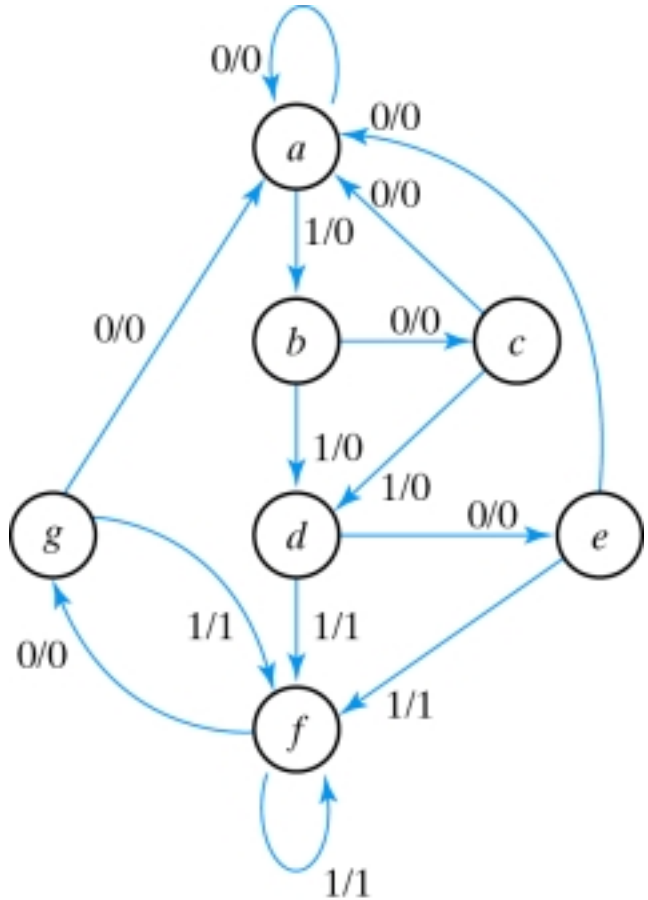


Fig. 5-22 State Diagram

State	Next State x=0	Next State x=1	Output x=0	Output x=1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

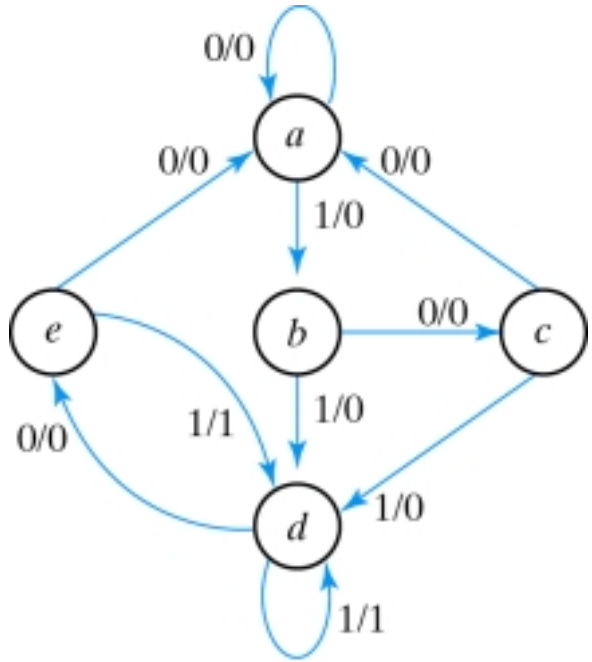


Fig. 5-23 Reduced State Diagram

- g & e equivalent, f & d equivalent

State Assignment

State	Binary	Gray Code	One-Hot
a	000	000	00001
b	001	001	00010
c	010	011	00100
d	011	010	01000
e	100	110	10000

Reduced State Table:
Binary State Assignment

	Next State		Output	
State	x=0	x=1	x=0	x=1
001	000	001	0	0
010	010	011	0	0
011	000	011	0	0
100	100	011	0	1
101	000	011	0	1

Table 5-10

Design Procedure

- Develop State Diagram From Specs
- Reduce States
- Assign Binary values to States
- Write Binary-coded State Table
- Choose Flip-Flops
- Derive Input and Output Equations
- Draw the Logic Diagram

Develop State Diagram: Sequence Detector

- Detect 3 or more 1s in sequence (a Moore Model)

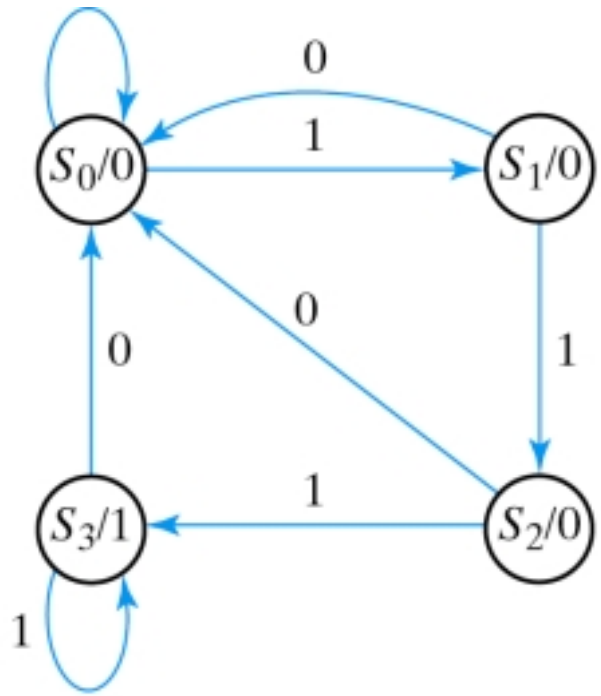


Fig. 5-24 State Diagram for Sequence Detector

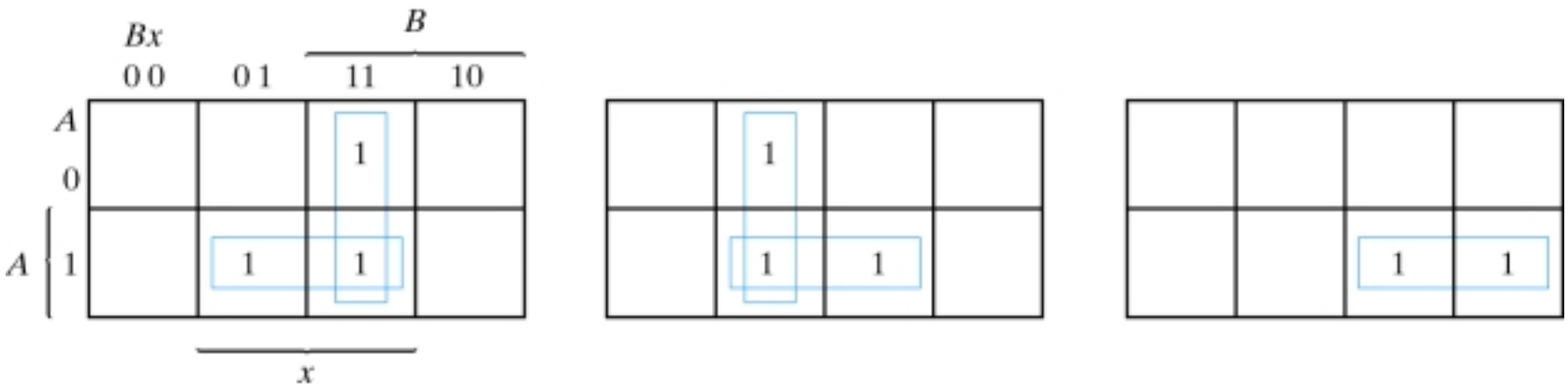
D Flip-Flop Input Equations

State		Input	Next State		Output
A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	1	1	1	1

Input equations come directly from the next state in D Flip-Flop design

$$A(t+1) = D_A(A,B,x) = \Sigma(3,5,7)$$
$$B(t+1) = D_B(A,B,x) = \Sigma(1,5,7)$$
$$y(A,B,x) = \Sigma(6,7)$$

Simplified Boolean Equations



$D_A = Ax + Bx$ $D_B = Ax + B'x$ $y = AB$

Fig. 5-25 Maps for Sequence Detector

Sequence Detector: D Flip-Flops

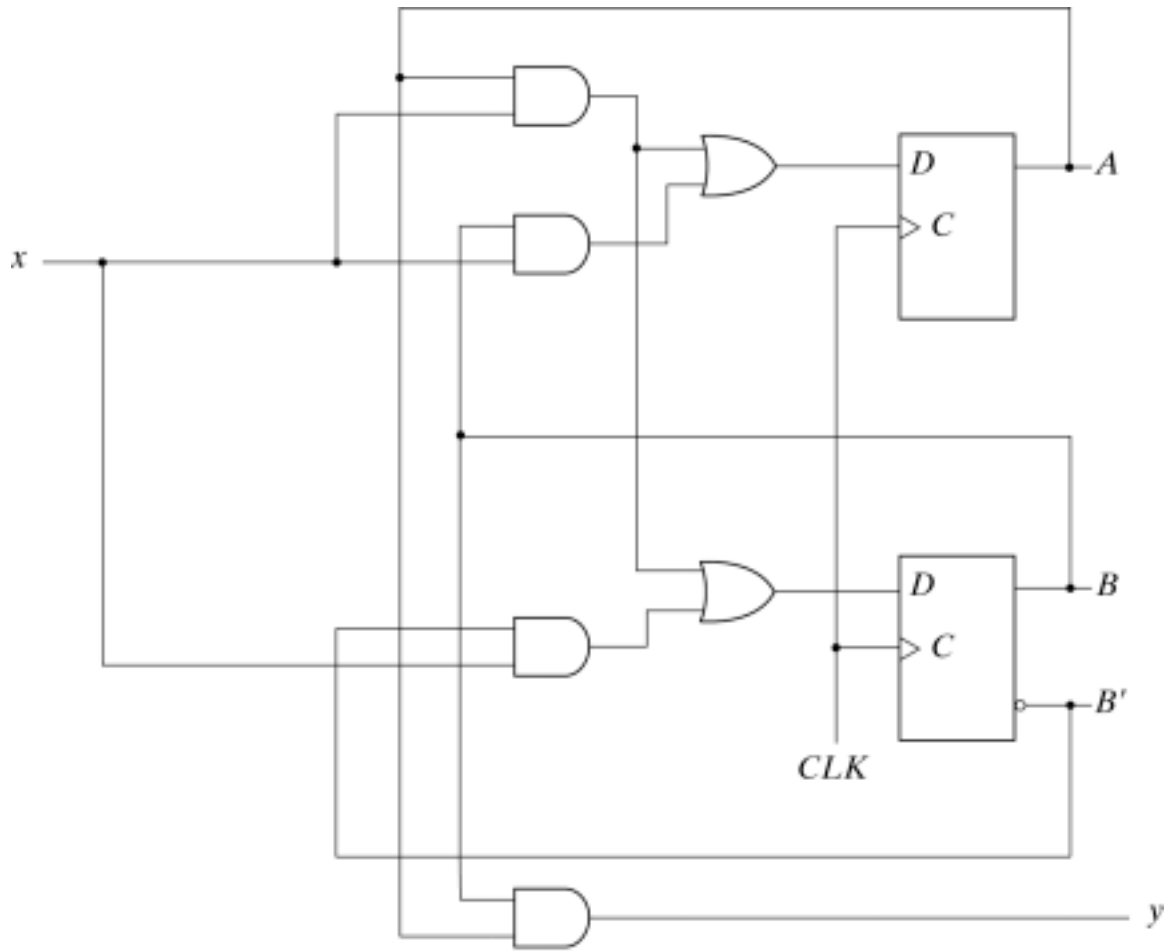


Fig. 5-26 Logic Diagram of Sequence Detector

Using JK or T Flip-Flops

1. Develop Excitation Table Using Excitation Tables

JK Flip-Flop

Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

T Flip-Flop

Q(t)	Q(t+1)	T
0	0	0
0	1	1
1	0	1
1	1	0

Table 5-12

State Table: JK Flip-Flop Inputs

Present State		Input	Next State		Flip-Flop Inputs			
A	B	x	A	B	J_A	K_A	J_B	K_B
0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	1	0	1
0	1	0	1	0	1	0	1	0
0	1	0	0	1	0	1	0	1
1	0	1	1	0	1	0	1	0
1	0	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1
1	1	1	0	0	0	0	0	0

Table 5-13

Maps for J and K Input Equations

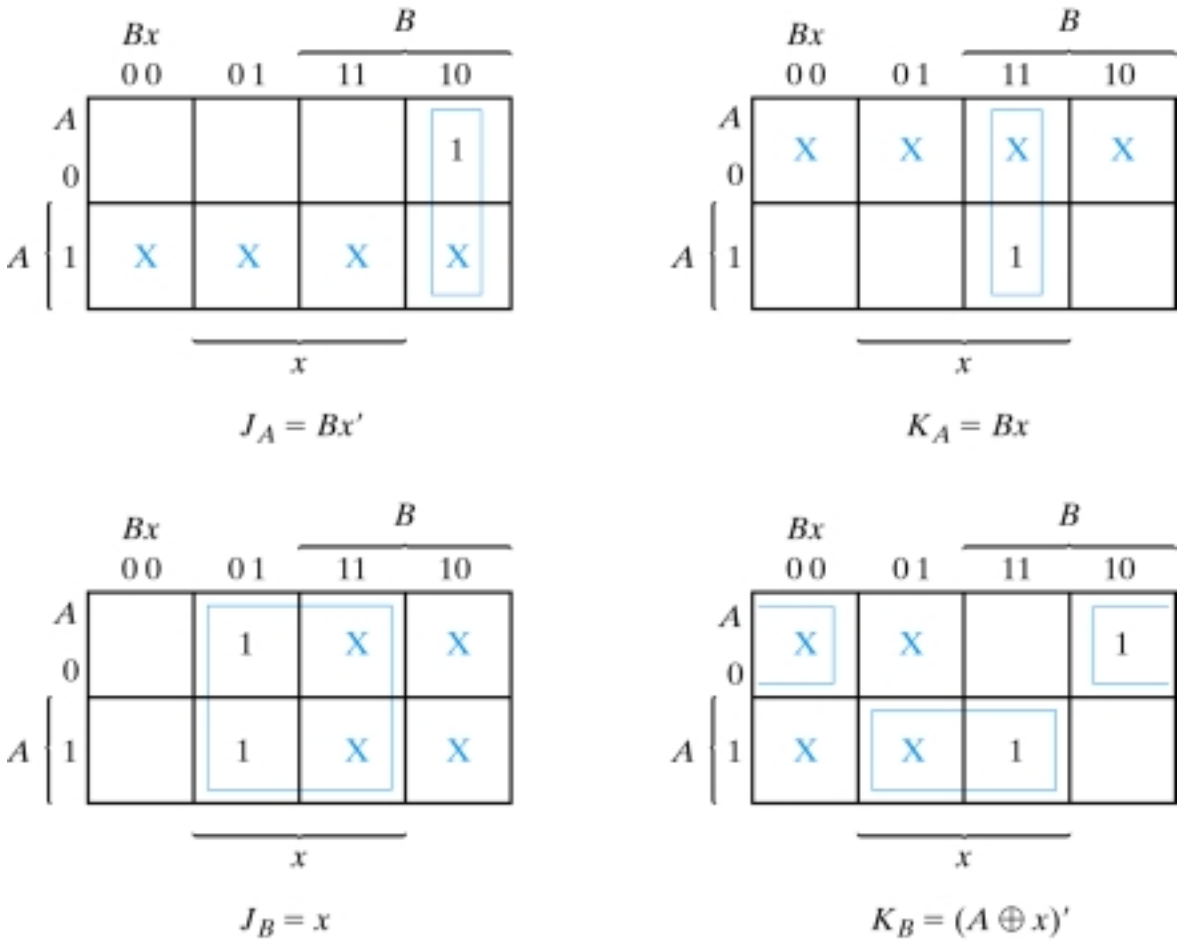


Fig. 5-27 Maps for J and K Input Equations

JK Flip-Flop Sequence Detector

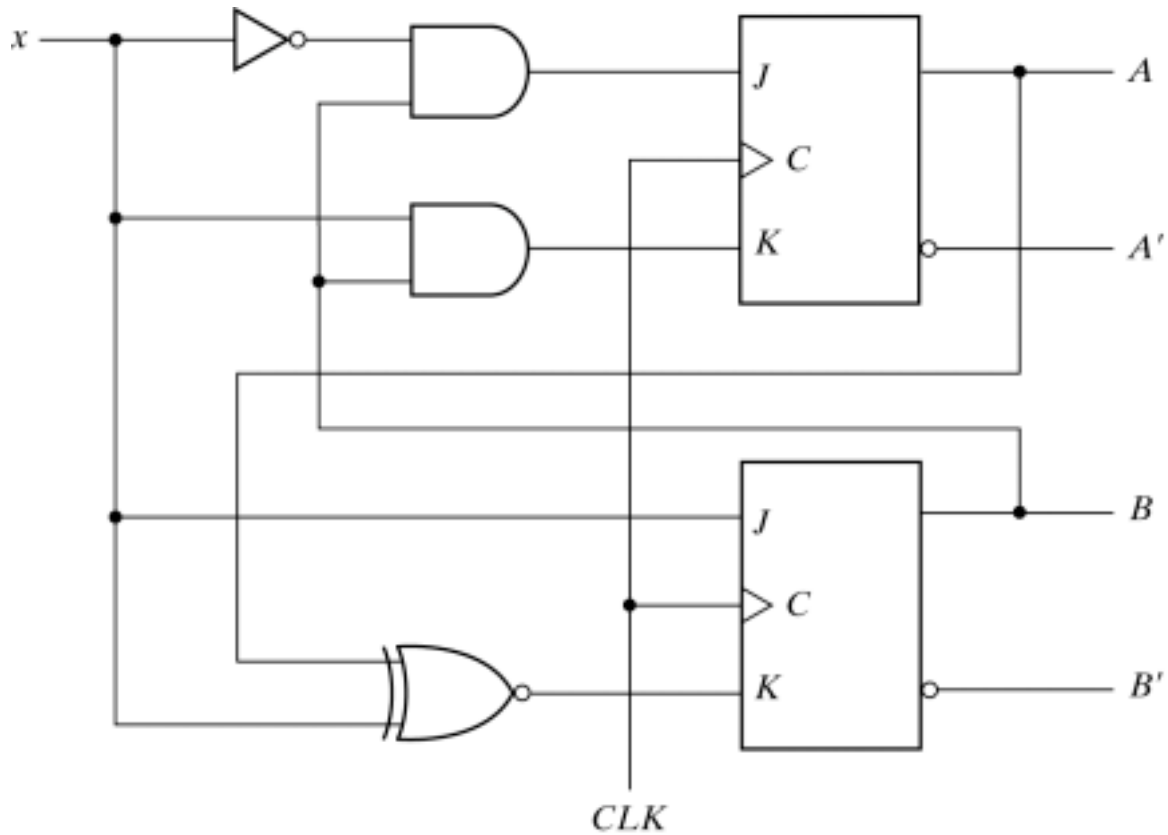


Fig. 5-28 Logic Diagram for Sequential Circuit with *JK* Flip-Flops

Synthesis Using T Flip-Flops:
Designing a Counter

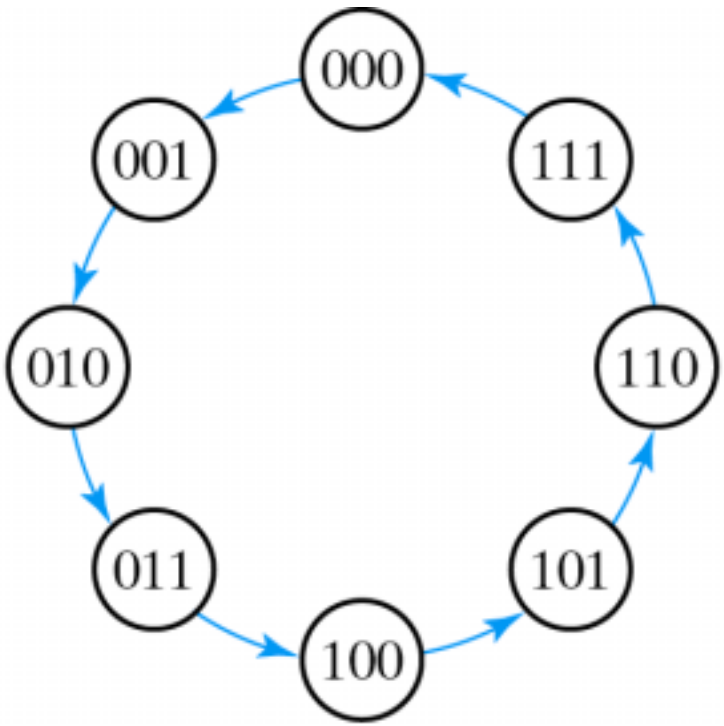


Fig. 5-29 State Diagram of 3-Bit Binary Counter

3-Bit Counter State Table

Present State			Next State			Flip-Flop Inputs		
A_2	A_1	A_0	A_2	A_1	A_0	T_{A2}	T_{A1}	T_{A0}
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	1	1
1	1	1	0	0	0	1	1	1

3-Bit Counter Karnaugh Maps

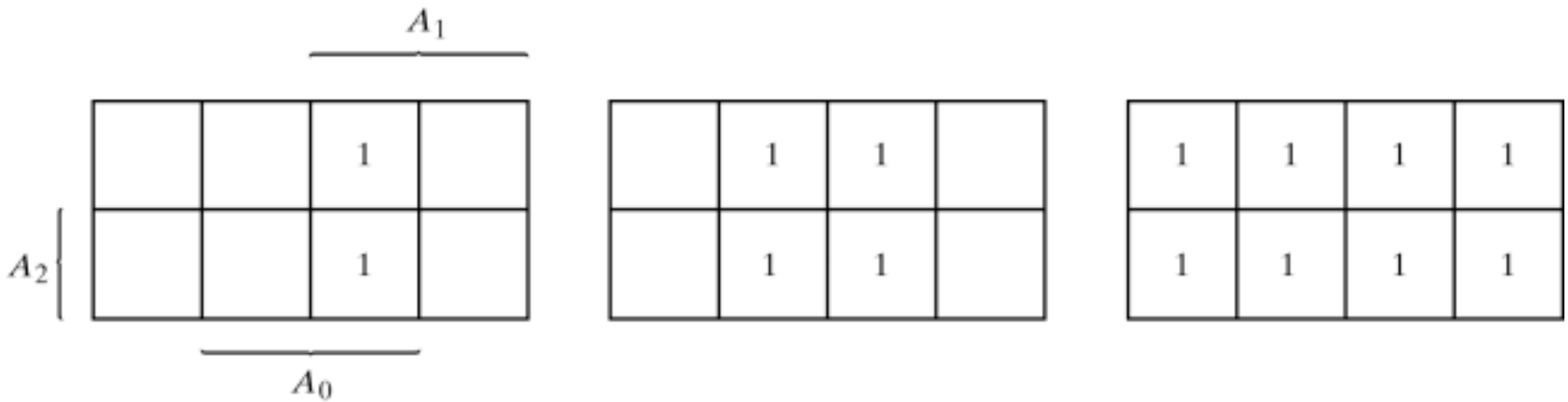


Fig. 5-30 Maps for 3-Bit Binary Counter

The 3-Bit Counter

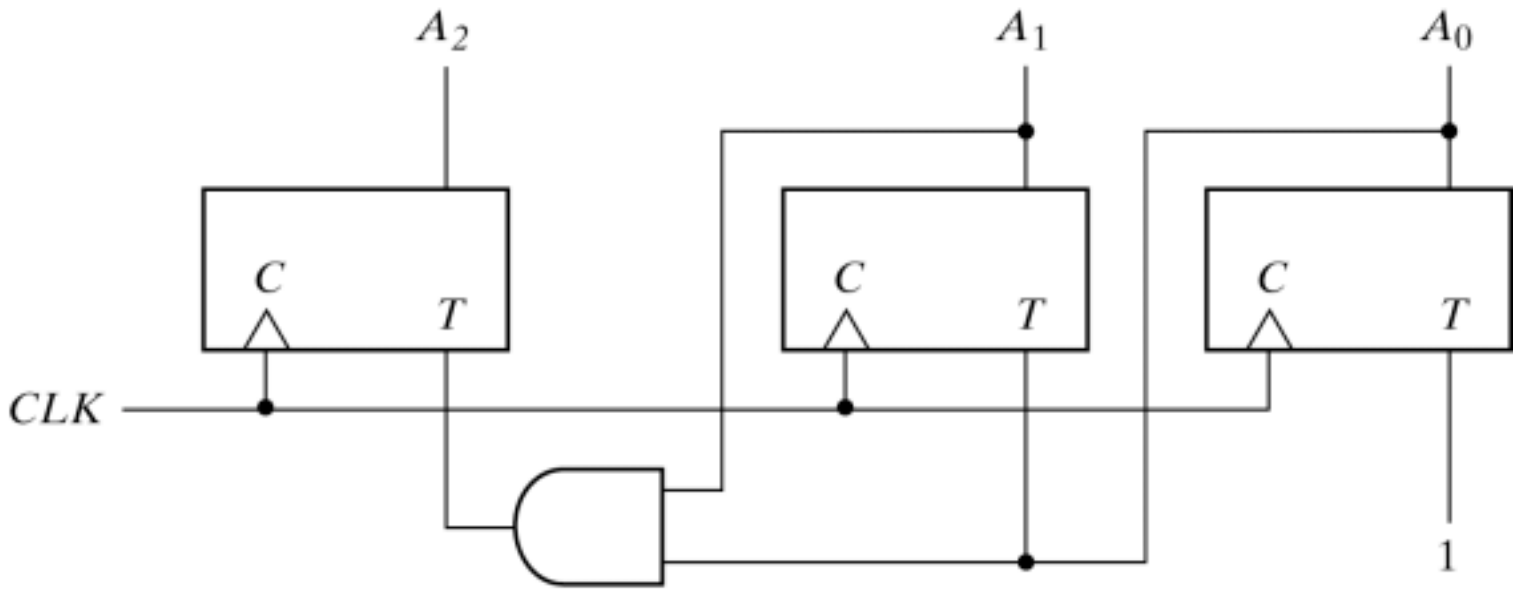


Fig. 5-31 Logic Diagram of 3-Bit Binary Counter