Digital Design
Lecture 13

ROMs and RAMs
Mano, 7.1-7.5

Conventional and Array Logic (PLA) Symbols

- PLA symbol has provisions for denoting "Cross Connects"
  (whether or not an input is connected)
- The horizontal line is actually a bus

(a) Conventional symbol (b) Array logic symbol

Fig. 7-1 Conventional and Array Logic Diagrams for OR Gate

Memory Unit

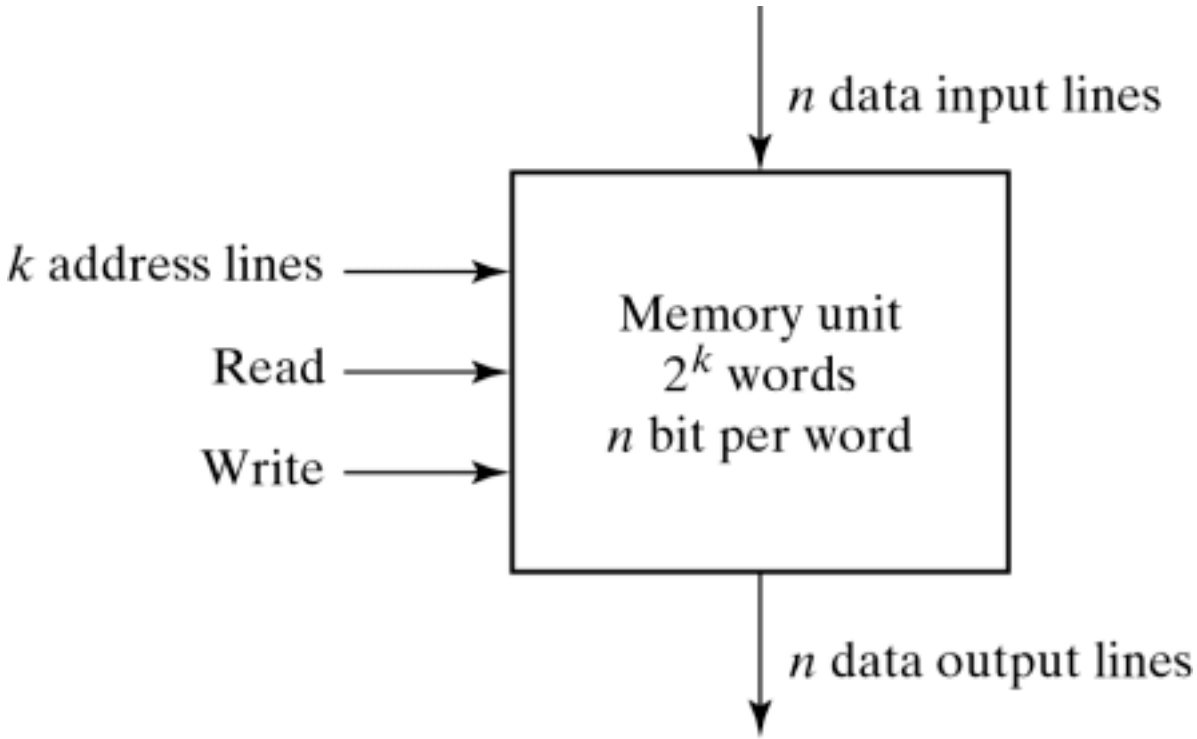


Fig. 7-2 Block Diagram of a Memory Unit

A 1024 x 16 Memory

Memory address		
Binary	decimal	Memory contest
0000000000	0	1011010101011101
0000000001	1	1010101110001001
0000000010	2	0000110101000110
	⋮	⋮
1111111101	1021	1001110100010100
1111111110	1022	0000110100011110
1111111111	1023	1101111000100101

Fig. 7-3 Content of a 1024 × 16 Memory

RAM Timing Diagram

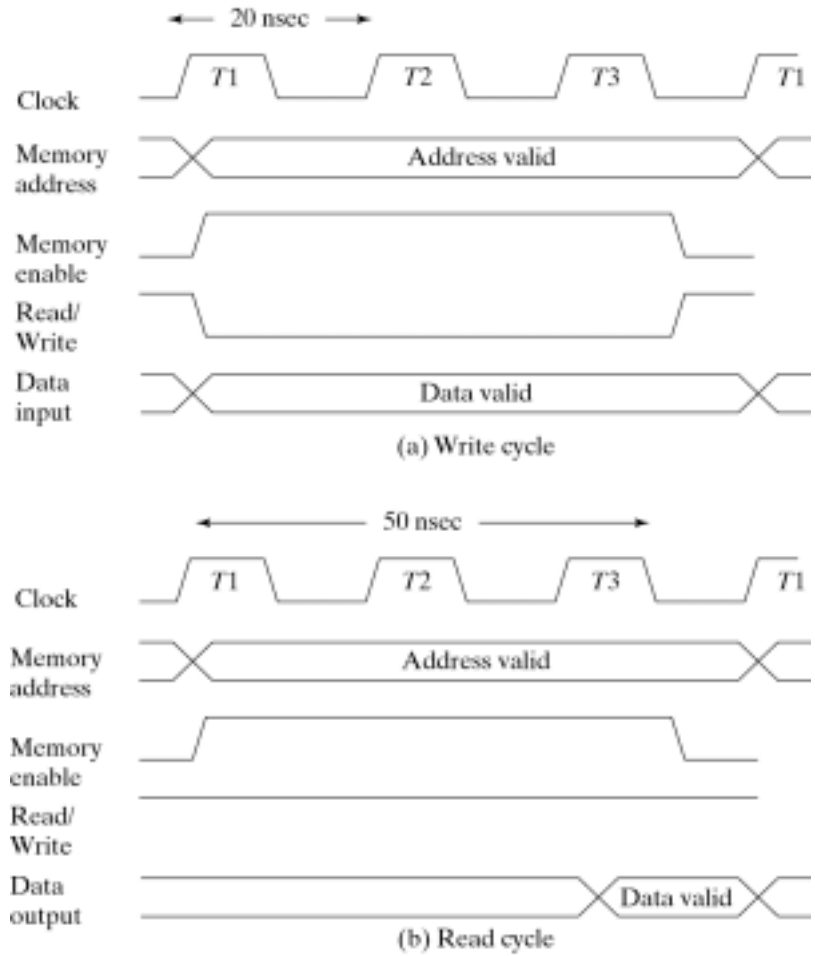


Fig. 7-4 Memory Cycle Timing Waveforms

A Memory Cell

- This is a “logical” structure
- The actual implementation is highly optimized

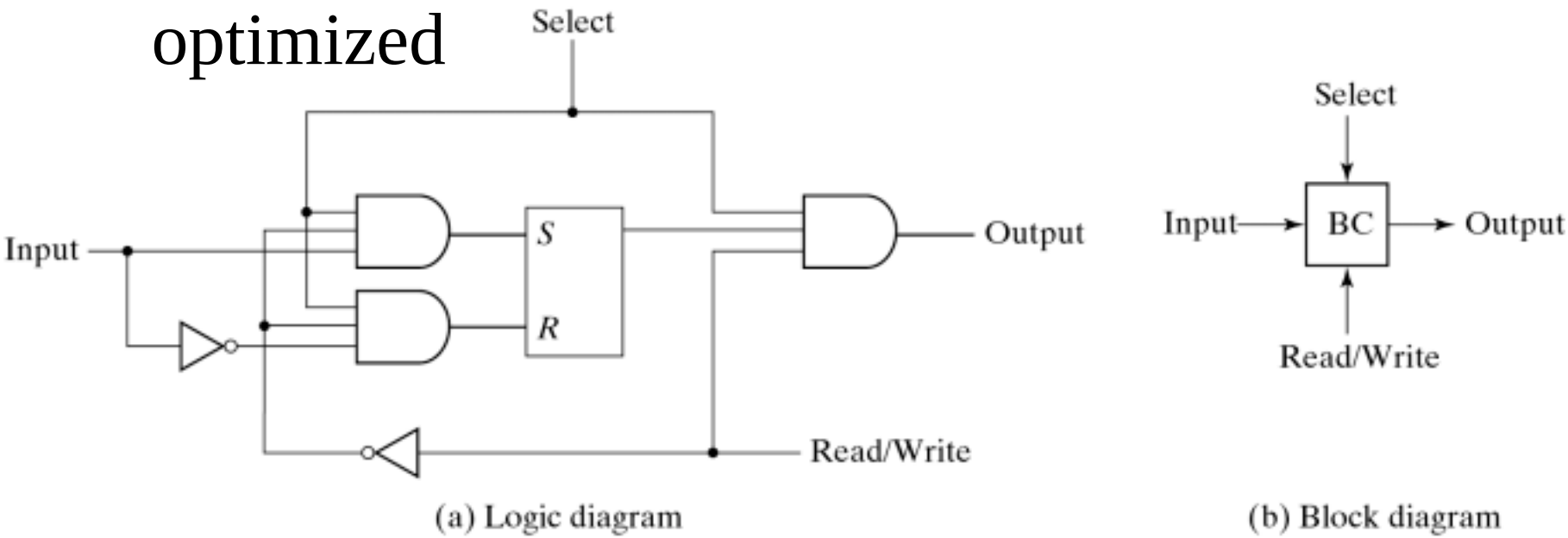


Fig. 7-5 Memory Cell

A 4 x 4 RAM

- One Dimensiona Decoding
- Suitable for small memories only

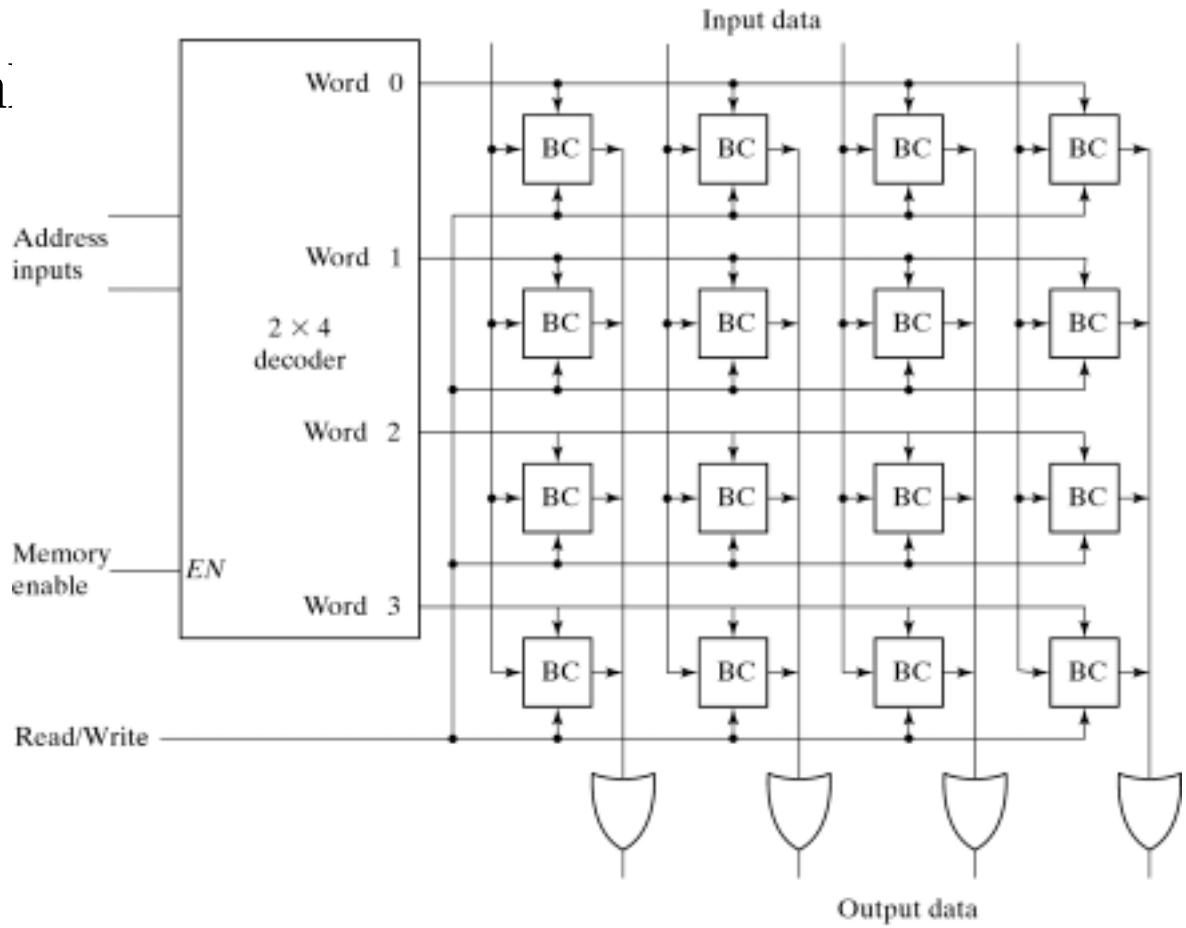


Fig. 7-6 Diagram of a 4 × 4 RAM

Two Dimensional Decoding

- Significant reduction in decoding hardware

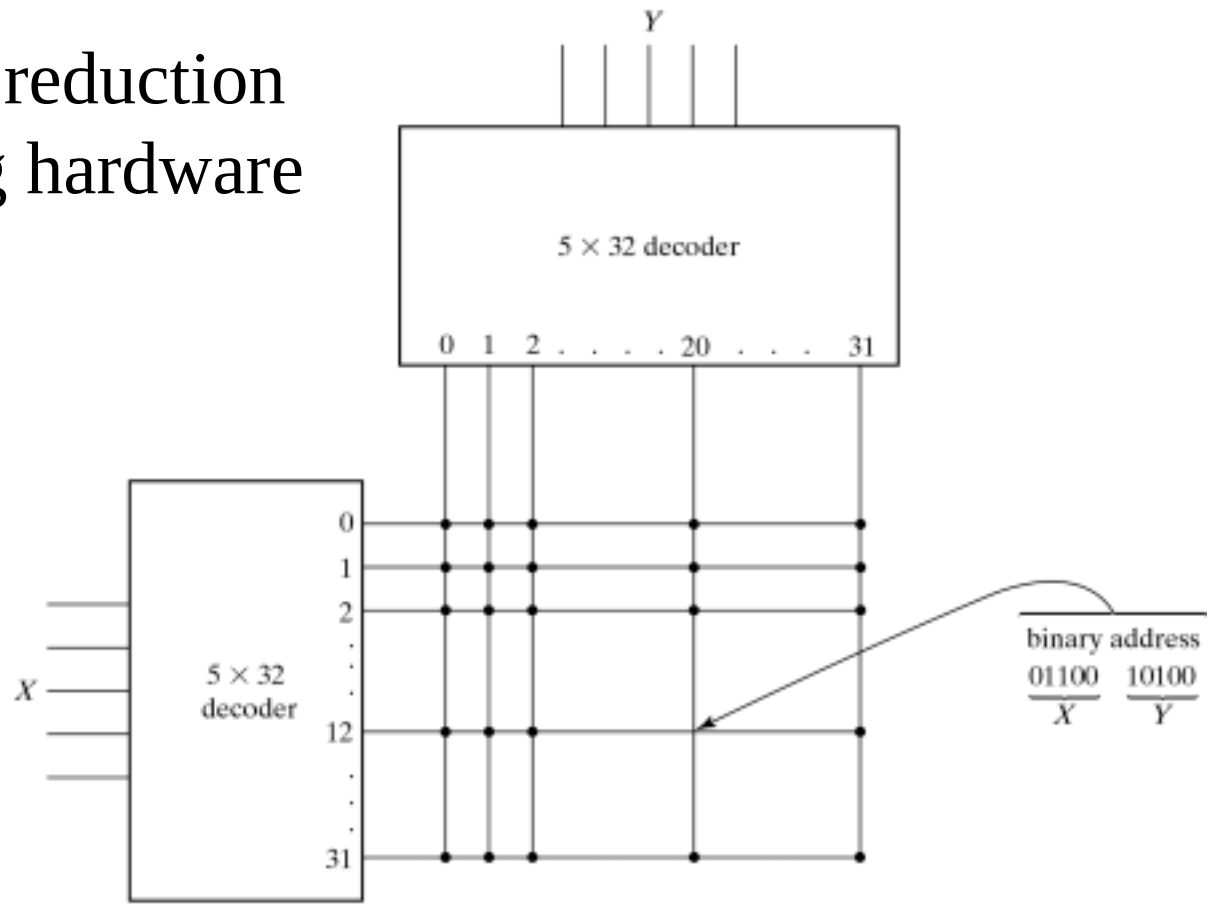


Fig. 7-7 Two-Dimensional Decoding Structure for a 1K-Word Memory

A 64Kword RAM

- Address selects (CAS and RAS) are “enables” that allow multiple “pages”

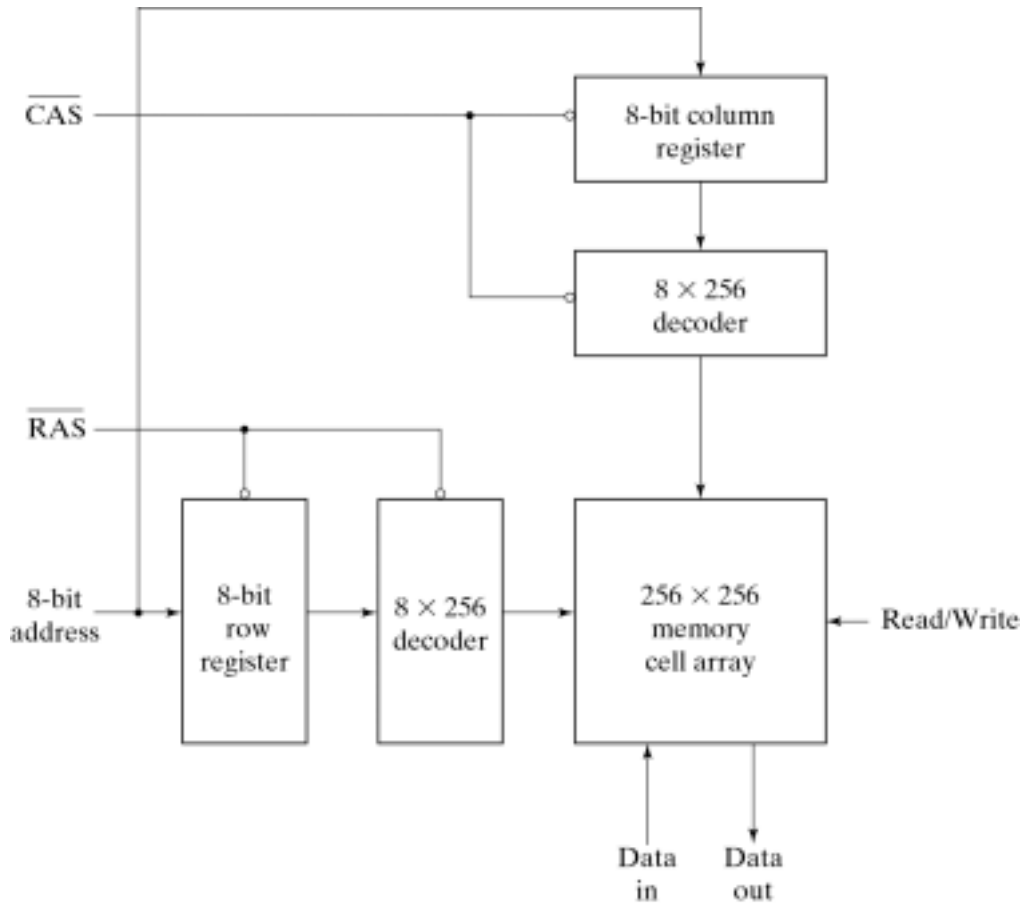


Fig. 7-8 Address Multiplexing for a 64K DRAM

Error Detection and Correction

- “Parity” bits added to data words for redundancy
- Stated when Claude Shannon introduced Information Theory in 1940
  (Two part BSTJ article)
  - The bit is the smallest measure of information
  - Channel Capacity Theorem:
    “If you send data slower than the Channel Capacity,
    You can receive it with no errors”
  - He proved this theorem, and gave how to calculate the Channel Capacity. He didn’t say how to achieve zero errors.

Simple Parity

- Add one bit to each word
  - Make the total number of ones even for "even parity"
  - Make the total number of ones odd for "odd parity"
- Detects "single bit" errors
- Used in most PCs (not Macs) at the byte level

Hamming Distance

- A measure of how different are the allowed data codes from each other
- Just add up the bit differences between two allowed codes to determine the “Hamming Distance”
  (a simplification of the Euclidean distance)
- The minimum Hamming Distance across the set of allowed codes is a measure of the strength of the code
- Parity yields ad minimum Hamming Distance of two

The Hamming Codes

- A clever code that adds multiple parity bits to a word at specific bit positions that cover different bits.
- Yields a Hamming Distance of 3 so that a single error is still closer to the original data word than any other and you can then correct the error.
- Adding one more overall parity bit increases the Hamming distance to 4 so you can also detect a Double error.
- PCs with ECC RAM use 22 bit words (5 plus 1 parity for 16 Data bits) to achieve single error correction and double error detection.

Read-Only Memory (ROM)

- Same as RAM, but simpler
- Data is established when manufactured and cannot be altered

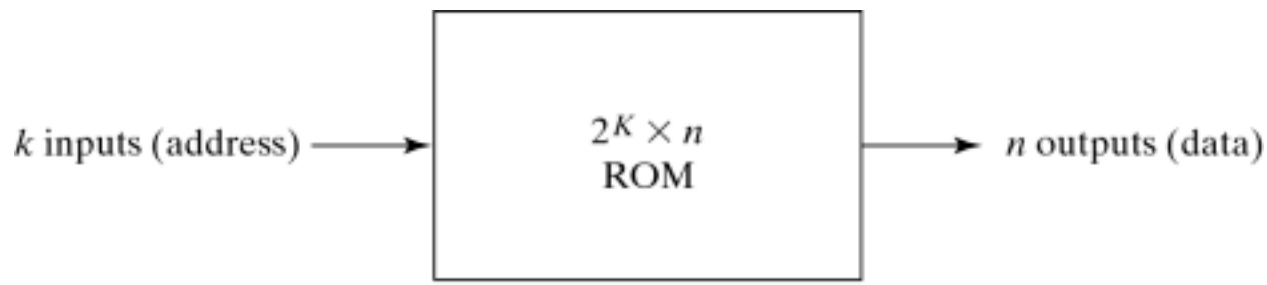


Fig. 7-9 ROM Block Diagram

ROM Internal Logic

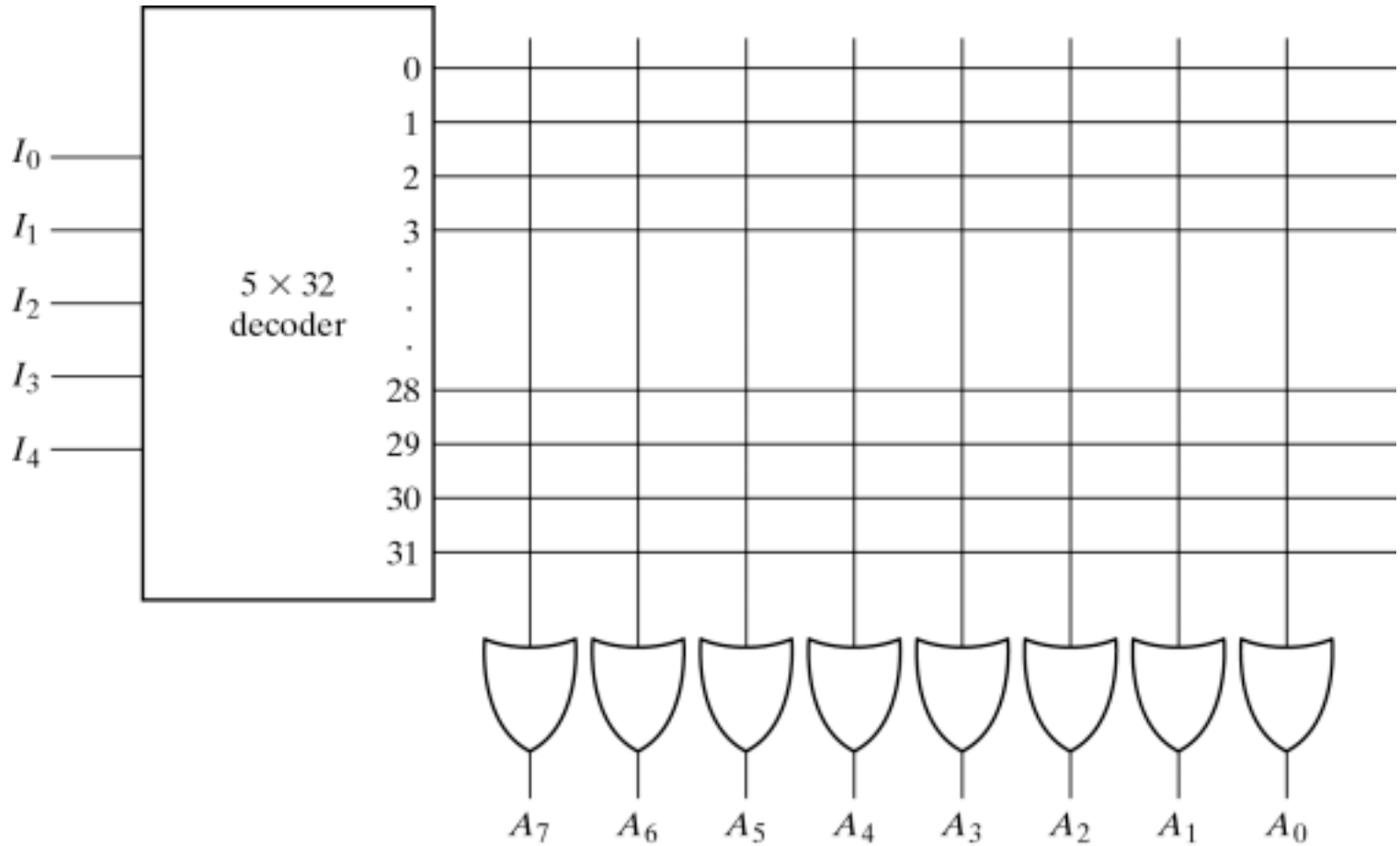


Fig. 7-10 Internal Logic of a 32 × 8 ROM

A “Programmable” ROM (PROM)

- Data “Burned” in later
- Cannot be altered a second time

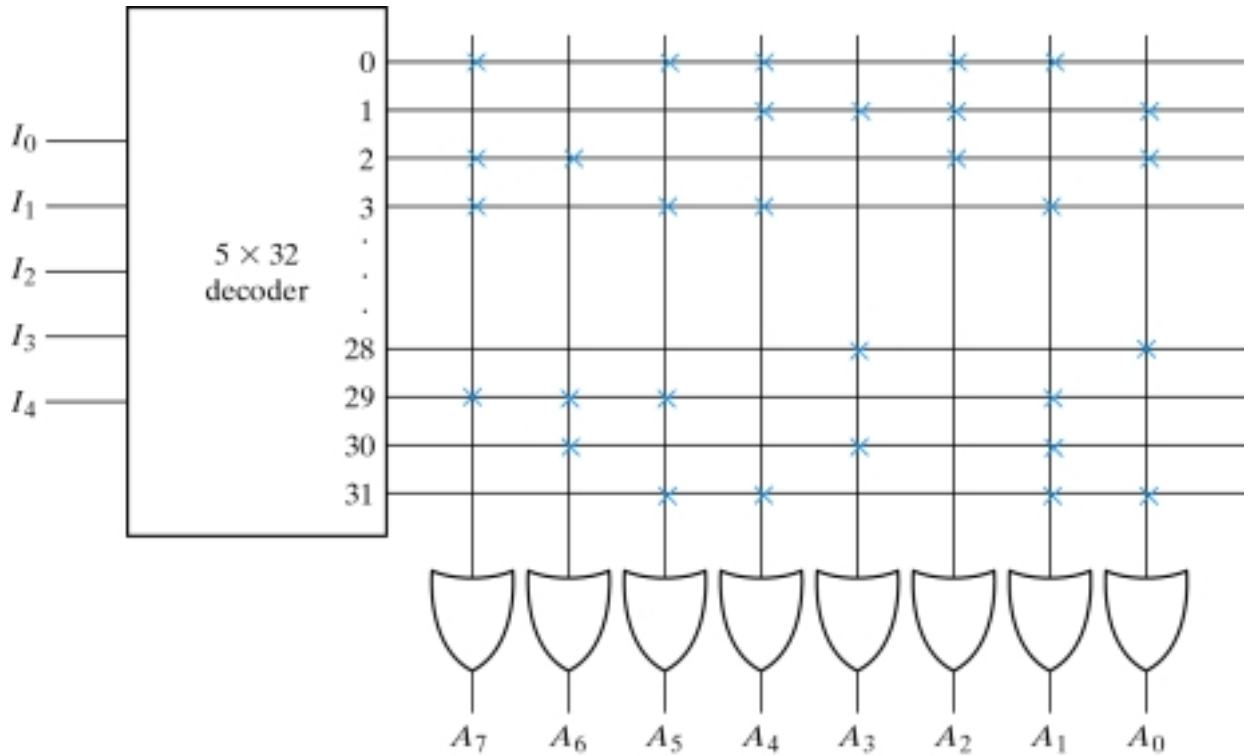
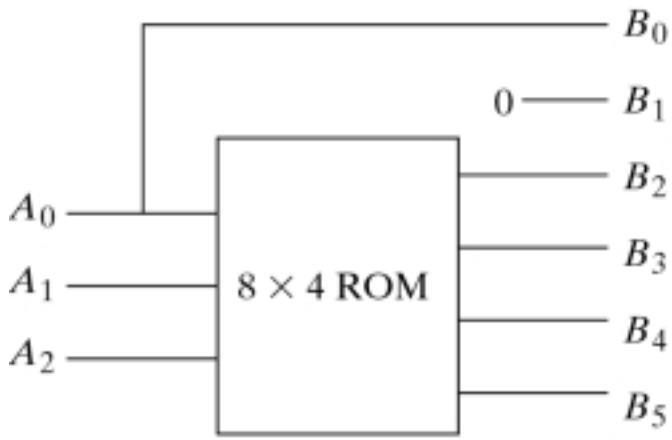


Fig. 7-11 Programming the ROM According to Table 7-3

A Example ROM



(a) Block diagram

A_2	A_1	A_0	B_5	B_4	B_3	B_2
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	1
0	1	1	0	0	1	0
1	0	0	0	1	0	0
1	0	1	0	1	1	0
1	1	0	1	0	0	1
1	1	1	1	1	0	0

(b) ROM truth table

Fig. 7-12 ROM Implementation of Example 7-1

Other Semiconductor Memories

- EPROM: PROMS that are “erasable” (usually by exposure to UV light, note that x-ray can also change them as in airport security)
- Flash or EEROM: Electrically erasable. Can be fully erased and rewritten in place using higher voltages than used to read data.