Week 10: MOS Logic Circuits

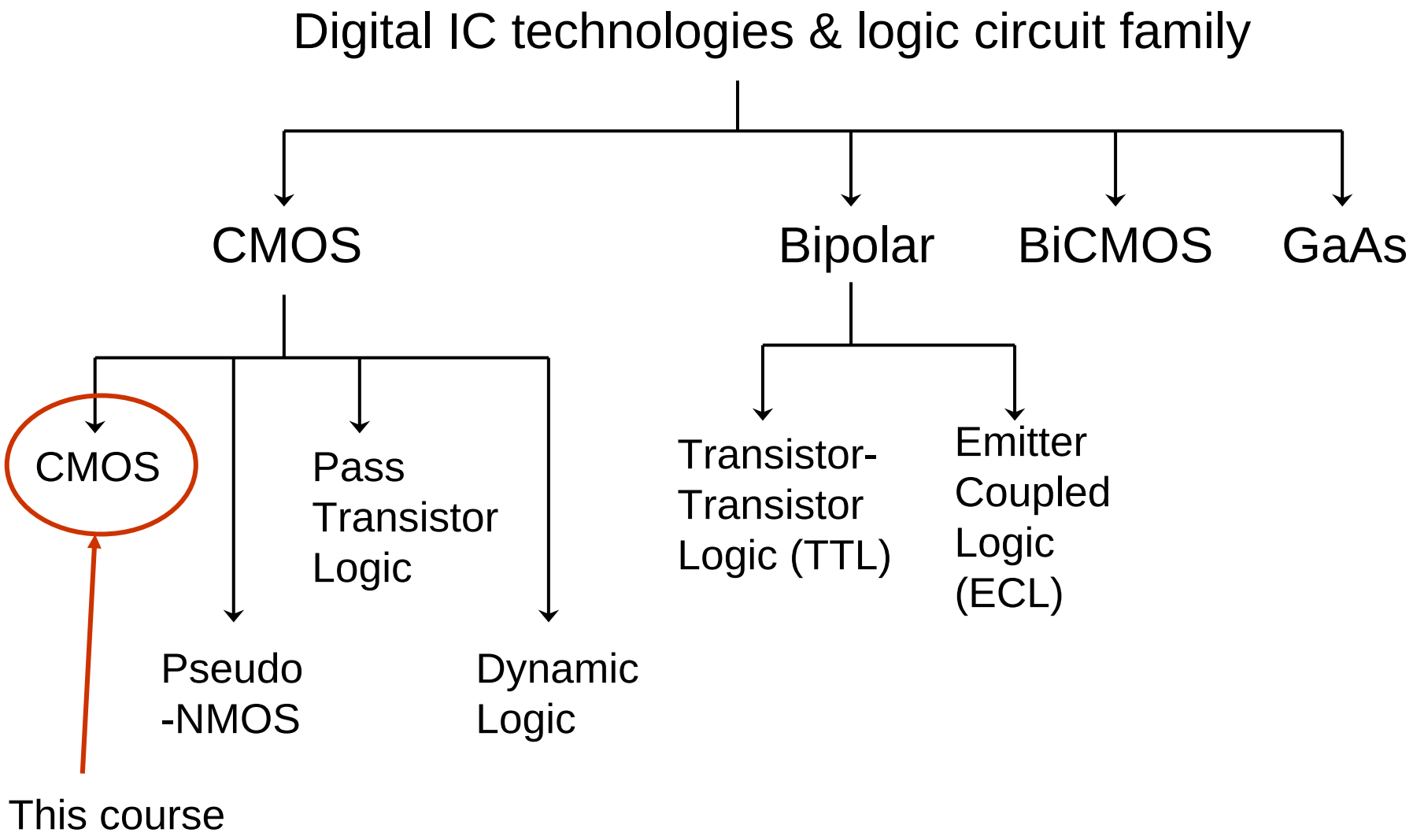
(45 minutes only)

Topics to cover …

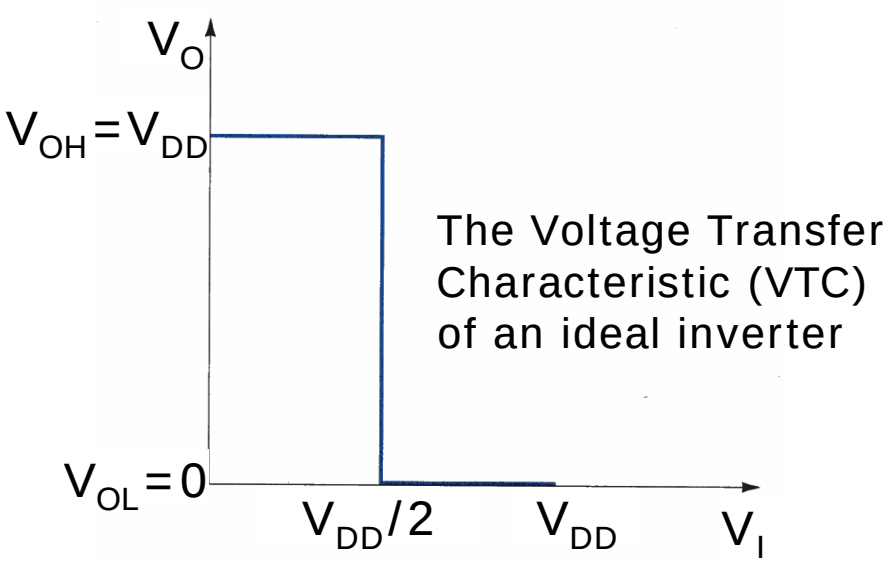
- CMOS Inverter
  - Static characteristics
  - Dynamic characteristics
  - Power dissipation
- Other CMOS logic gates

Reading Assignment:
Chap 6.1-6.3, 7.1-7.4 of Jaeger and Blalock or
Chap 7.1 - 7.3, 7.7 of Sedra and Smith

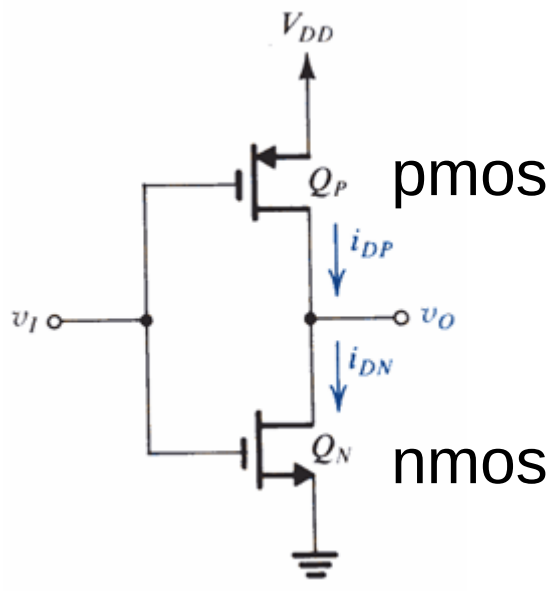
Digital IC Technologies and Logic-Circuit Family

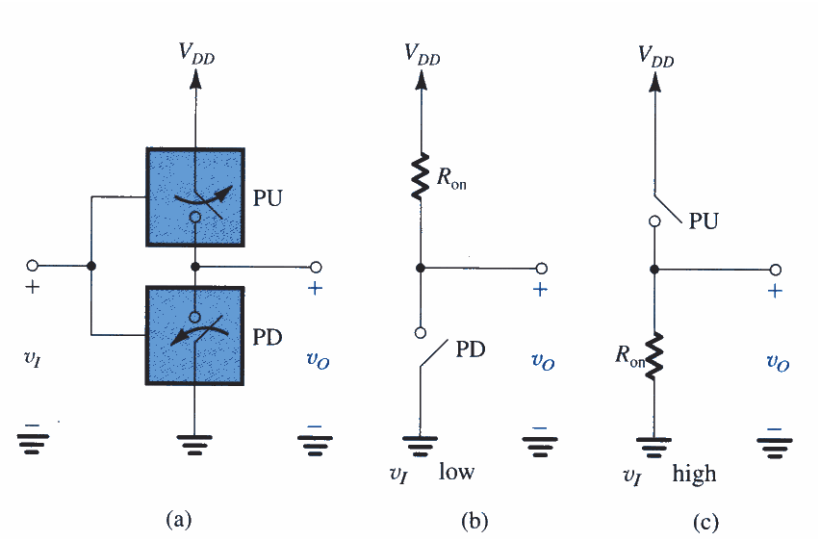


Ideal Inverter



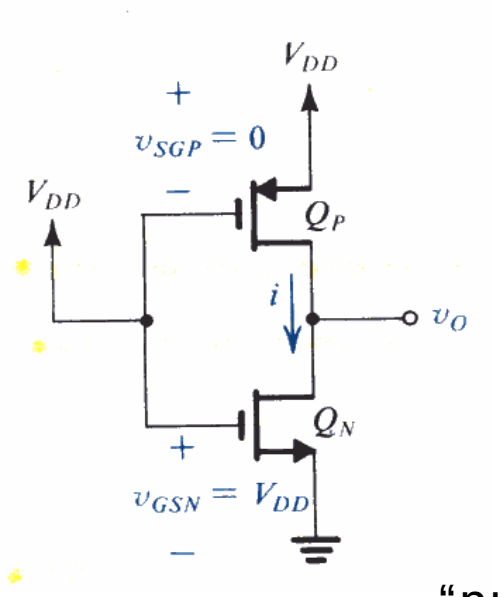
CMOS Inverter

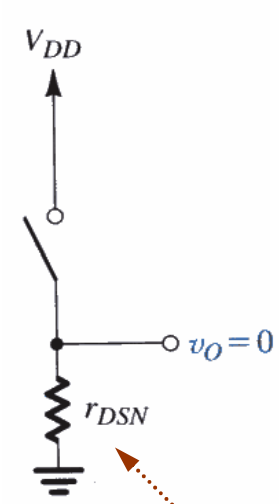


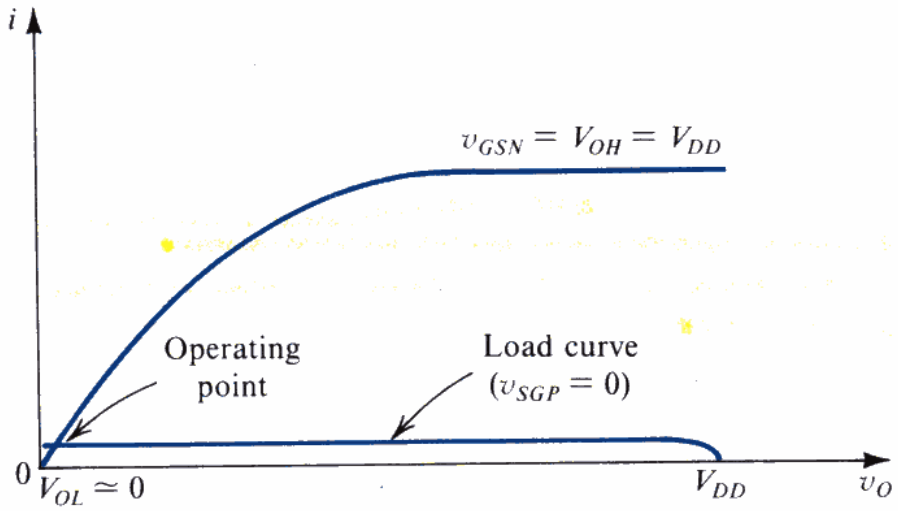


PU: pull up network, responsible for producing HIGH output
PD: pull down network, responsible for producing LOW output

Case 1: $V_I = V_{DD}$







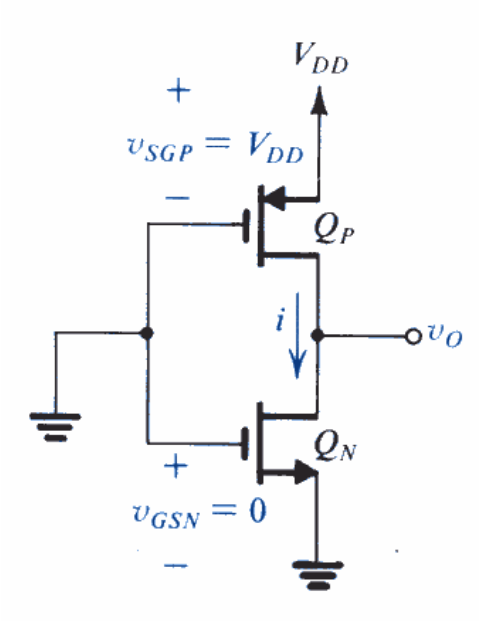
"pull-down"

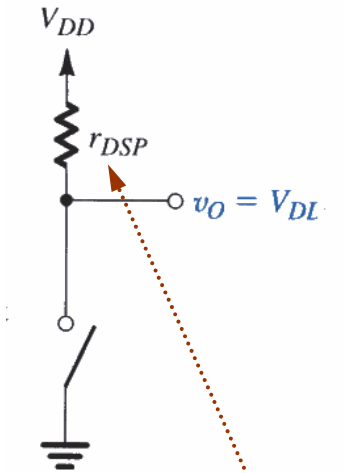
Q_P OFF
Q_N ON: output pulled down
→ V_O=0V

The output resistance of Q_N (linear mode):

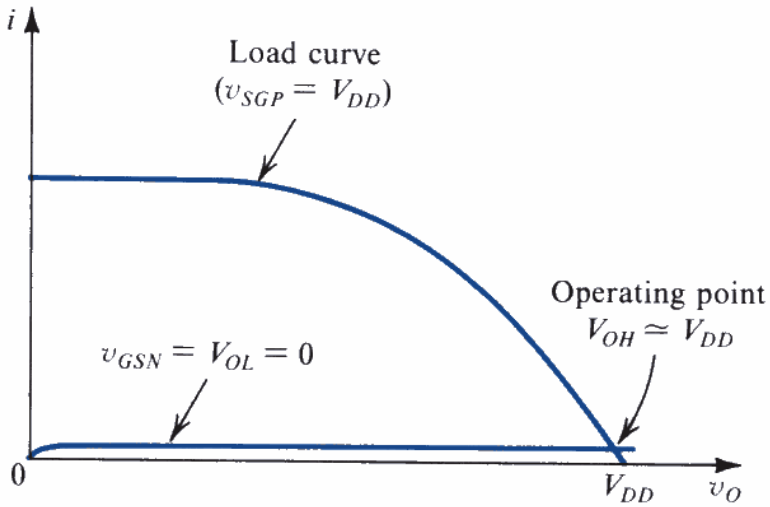
$$r_{DSN} = \frac{1}{k_n'\left(\frac{W}{L}\right)(V_{DD} - V_{tn})}$$

Case 2: $V_I = 0V$





"pull-up"



Q_N OFF
Q_P ON: output pulled up.
$\rightarrow V_O = V_{DD}$

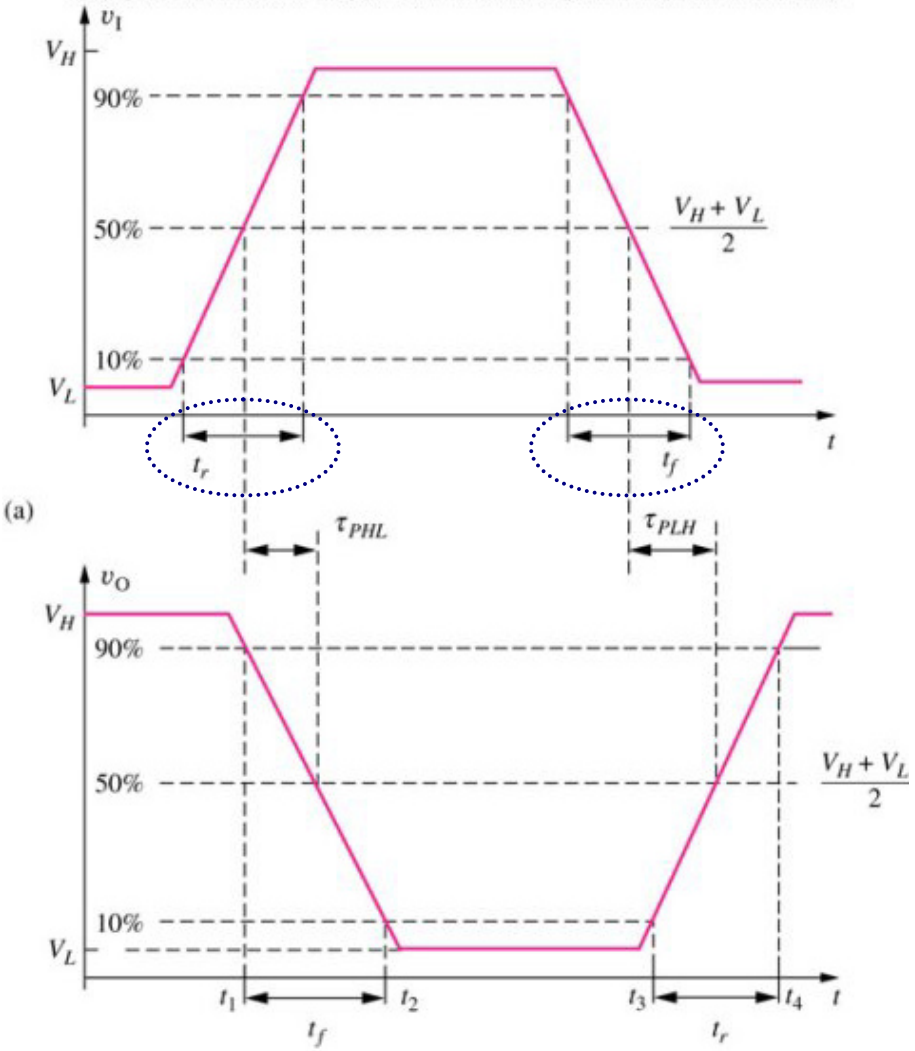
The output resistance of Q_P (linear mode):

$$r_{DSN} = \frac{1}{k'_p \left(\frac{W}{L}\right)(V_{DD} - V_{tp})}$$

Topics to cover …

- CMOS Inverter
  - Static characteristics
  - Dynamic characteristics
  - Power dissipation
- Other CMOS logic gates

Dynamic Characteristic: Rise and Fall times



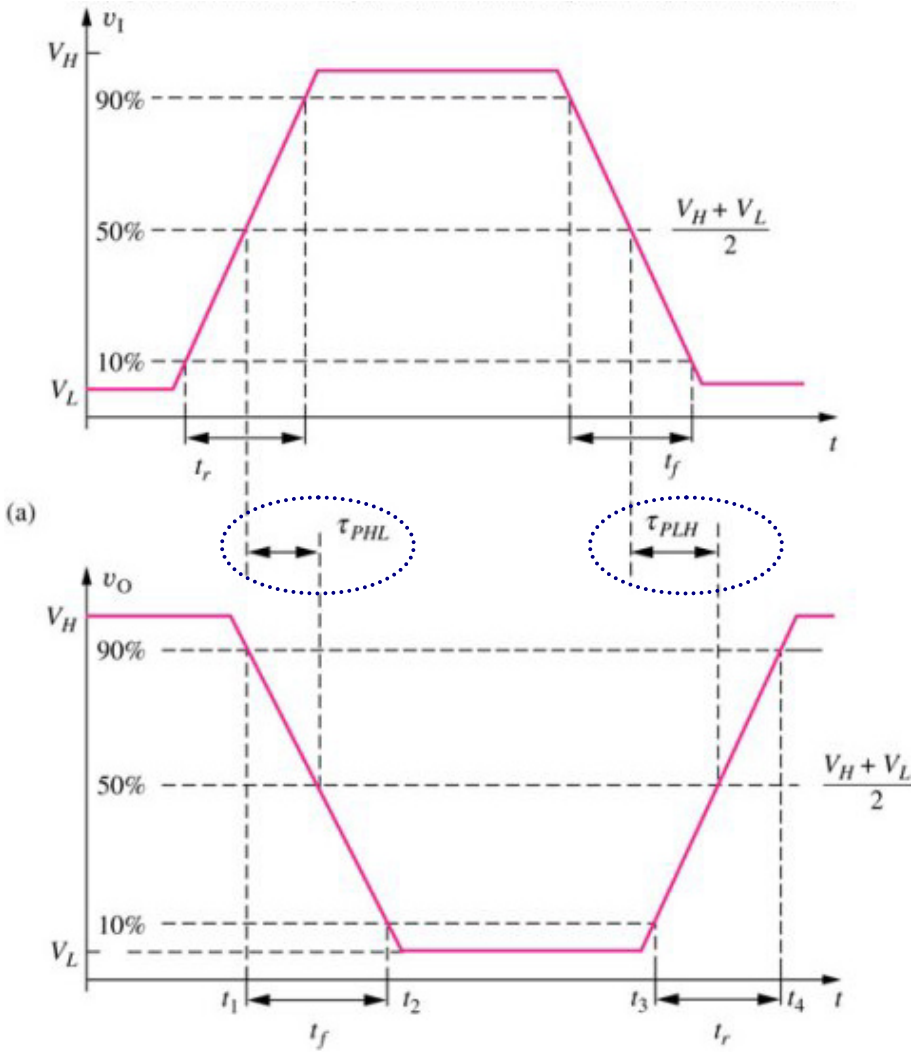
- The rise and fall times, t_f and t_r, are measured at the 10% and 90% points on the transitions between the two states.

$$V_{10\%} = V_L + 0.1\Delta V$$

$$V_{90\%} = V_L + 0.9\Delta V$$

$$= V_H - 0.1\Delta V$$

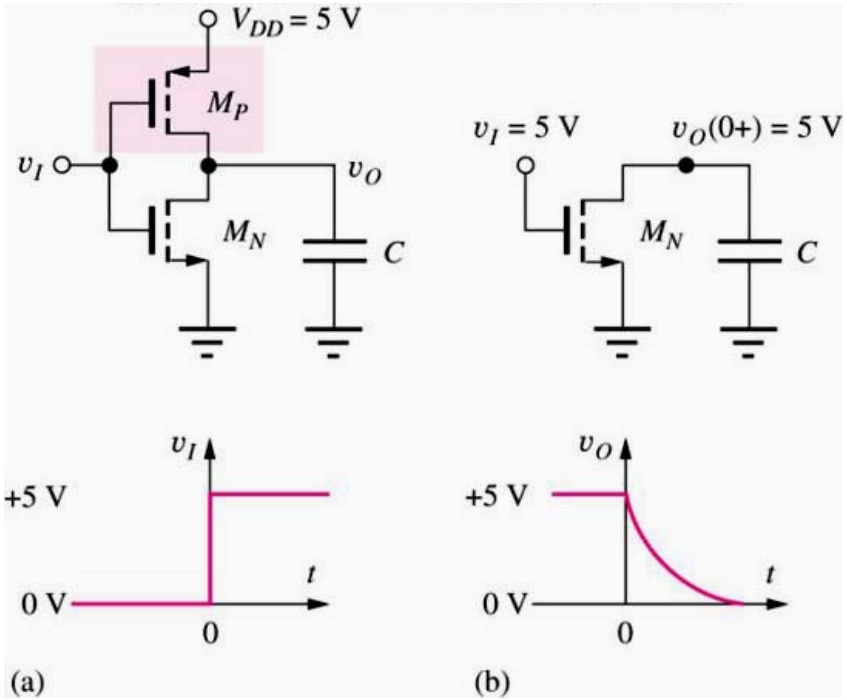
Dynamic Characteristic: Propagation Delay

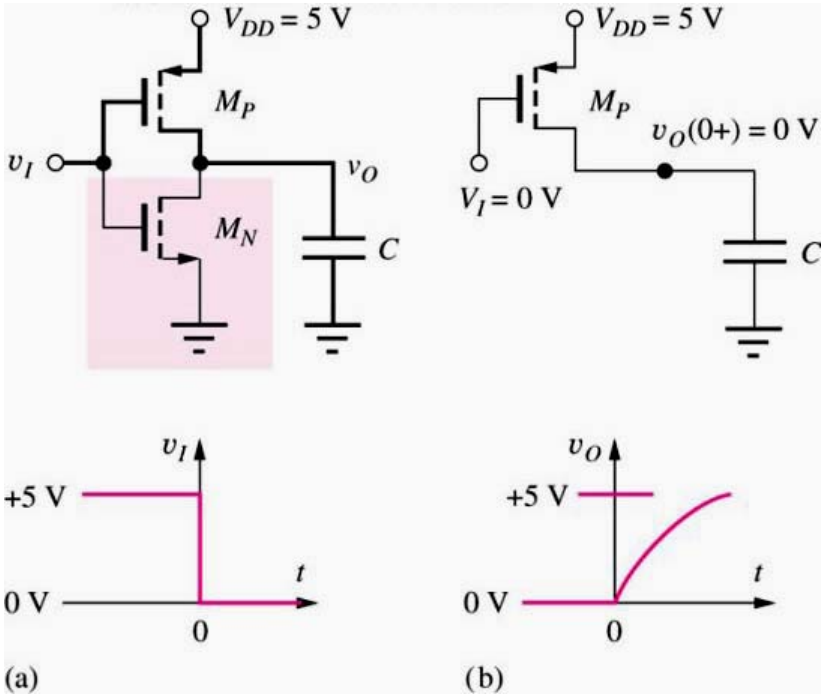


- Propagation delay: the time between a change at the 50% point input to cause a change at the 50% point of the output
- The high-to-low prop delay, τ_{PHL}, and the low-to-high prop delay, τ_{PLH}, are usually not equal, but can be described as an average value:

$$\tau_P = \frac{\tau_{PHL} + \tau_{PLH}}{2}$$

Propagation Delay





- C represents parasitic capacitances:
  - MOS gate capacitance of next logic gate
  - Wire capacitance to ground
- Output parasitic capacitor voltage cannot change instantaneously
- Capacitive charging/discharging contributes to propagation delay

Propagation Delay Estimate

- It can be shown (see section 7.3.1 and 6.14.12)

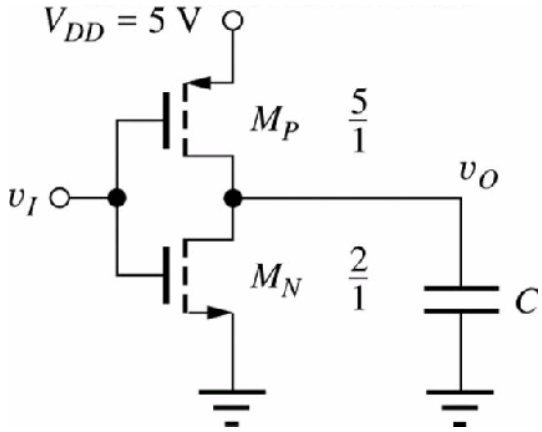
$$\tau_{PHL} \propto R_{onN} C$$

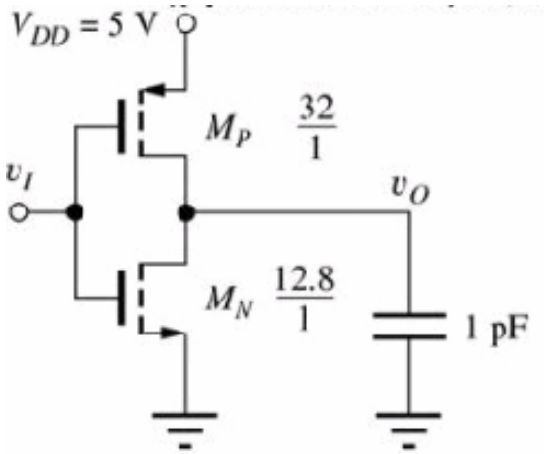
$$\text{where } R_{onN} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_H - V_{TN})}$$

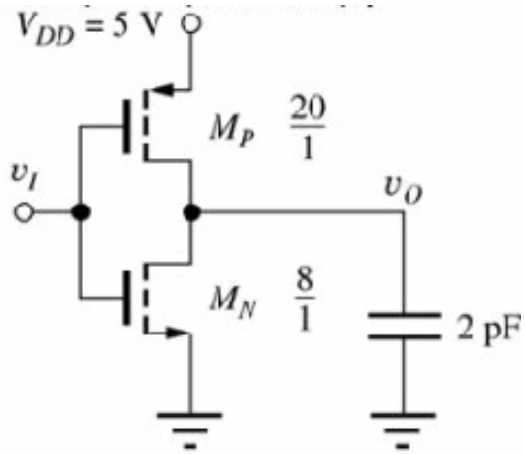
- For matched nmos and pmos ($\mu_n C_{ox} \left(\frac{W}{L}\right)_n = \mu_p C_{ox} \left(\frac{W}{L}\right)_p$), $\tau_{PLH} = \tau_{PHL}$

- The delay depends on C
  - In smaller feature size CMOS process, wires and transistors are smaller
  - Parasitic C is smaller
  - Delay is smaller → Circuits run faster
- The delay also depends on R_{ON}

Example







Given that:

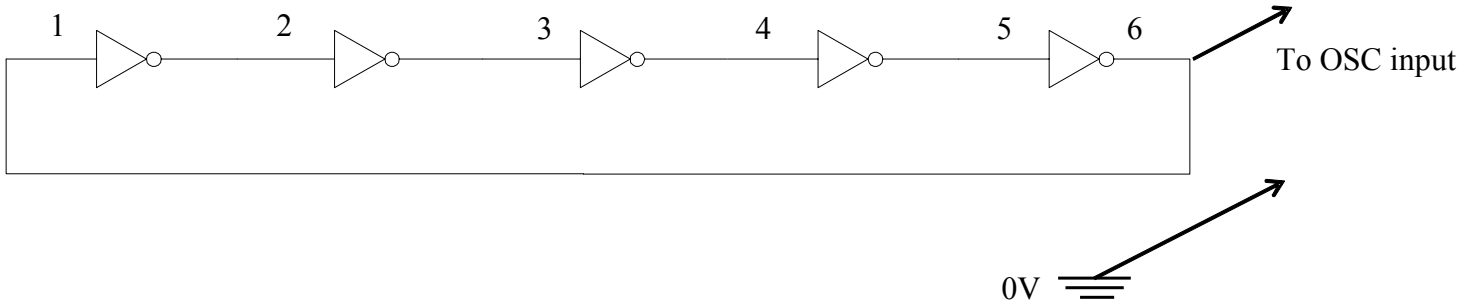
For C=1pF,

$\tau_p = 6.4ns$

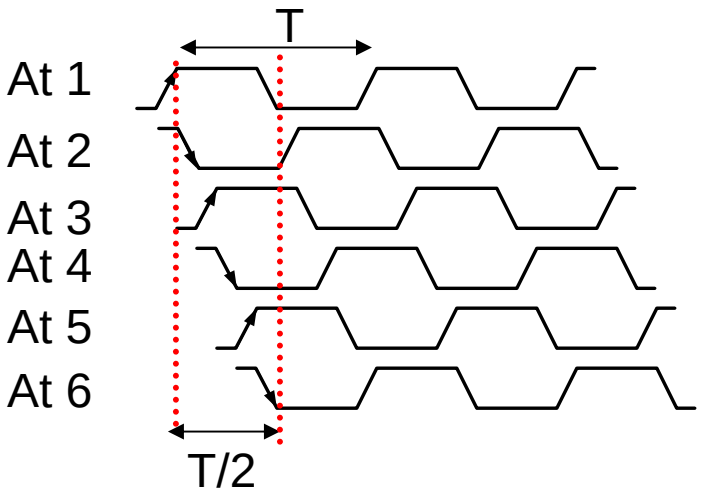
$\tau_p = ?$

$\tau_p = ?$

Ring Oscillator



- If odd number of inverters (at least 3) are connected as a ring, it oscillates.
- Oscillation frequency relates to the propagation delay of the inverters
- Waveform at 6 = waveform at 1 → 5 Delays = T/2 → Delay = T/10



Topics to cover …

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  - Dynamic characteristics
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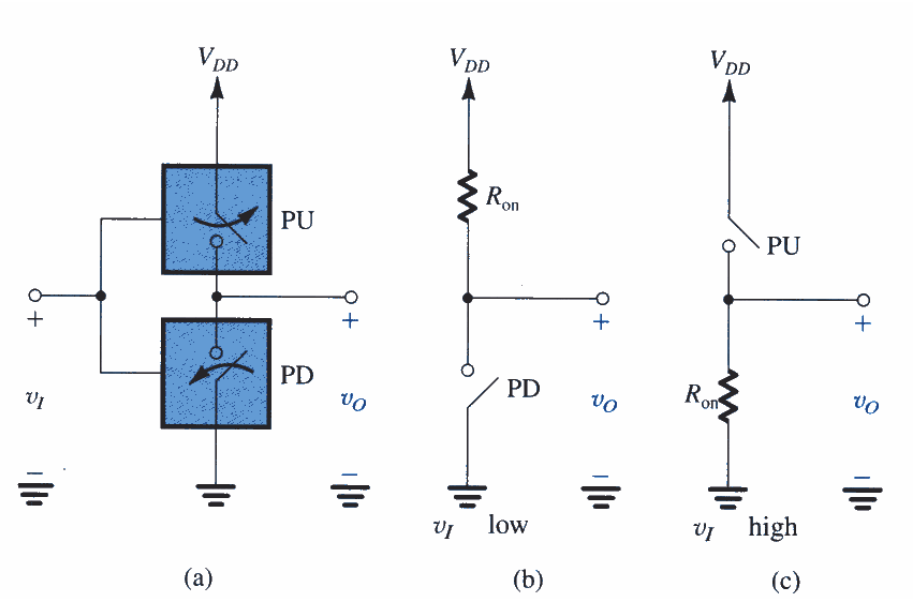
Power Dissipation

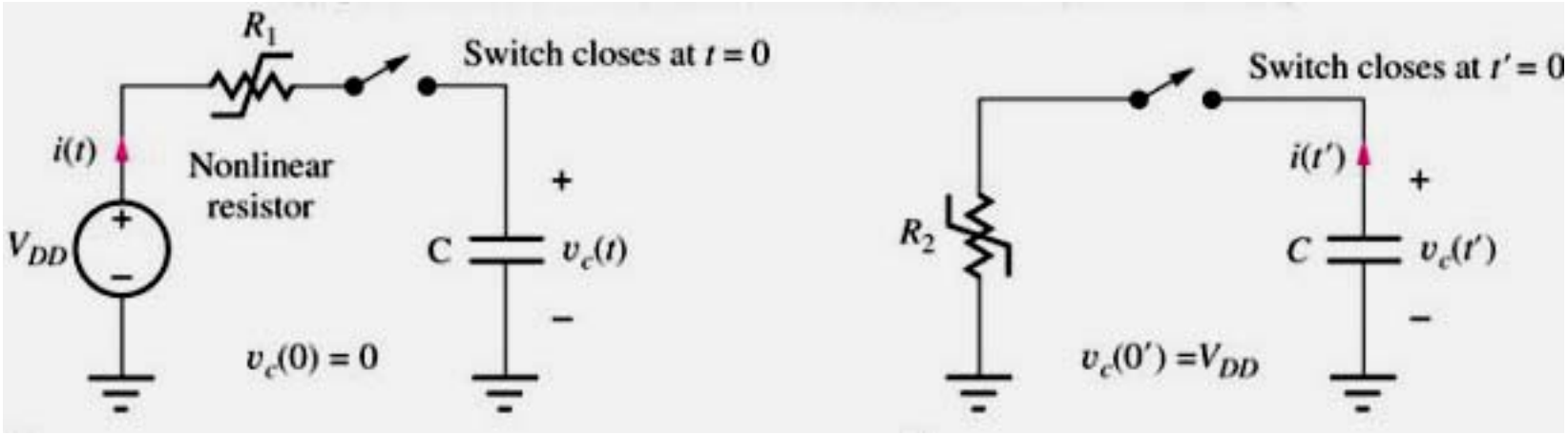
- CMOS logic has no static power dissipation
  - The is no DC path between VDD and GND at any time



- But, when the inverter changes its output…

Dynamic Power Dissipation

- When the inverter charges or discharges the output capacitor, it consumes power.



Charging

Discharging

Dynamic Power Dissipation

- The energy delivered from the VDD is:

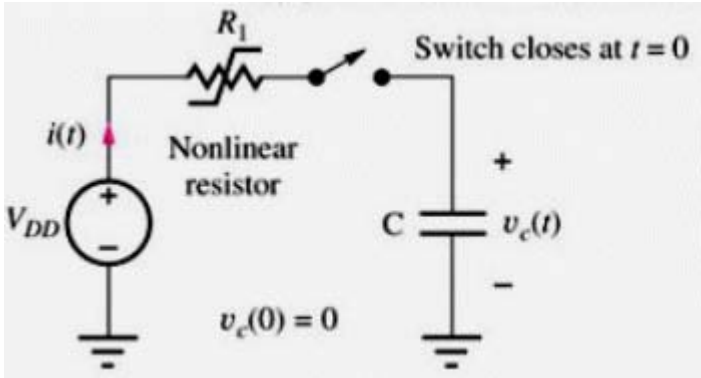
$$E_D = V_{DD}\int_0^{\infty} i(t)dt = V_{DD}\int_0^{\infty}\frac{dq(t)}{dt}dt = CV_{DD}\int_{V_C(0)}^{V_C(\infty)} 1dv_C = CV_{DD}^2$$

- The energy stored by the capacitor is:

$$E_D = \frac{CV_{DD}^2}{2}$$

- The difference between the above two terms represents the energy lost in the resistive elements:

$$E_L = E_D - E_S = \frac{CV_{DD}^2}{2}$$



Dynamic Power Dissipation

- The total energy lost in the first charging and discharging of the capacitor through resistive elements is given by:

$$E_{TD} = \frac{CV_{DD}^2}{2} + \frac{CV_{DD}^2}{2} = CV_{DD}^2$$

- For every clock cycle, the dynamic power dissipation is:

$$P_D = \text{Energy/Time} = CV_{DD}^2 f$$

  - This result can be extended to a complex digital IC, where C represents the area of the IC
  - Lower V_{DD} is very effective for reducing power supply
  - Reducing C also helps reducing power

Topics to cover …

- CMOS Inverter
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- Other CMOS logic gates

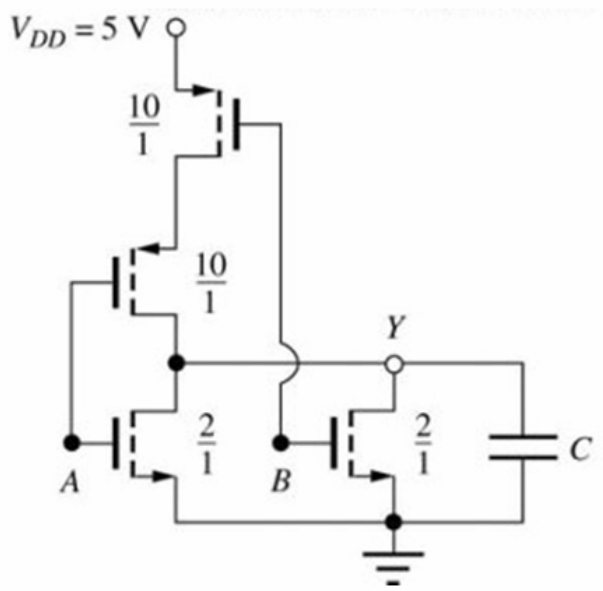
CMOS NOR Gate

Pull-up Network:

$$Y = \overline{A}\,\overline{B}$$

Pull-down Network:

$$\overline{Y} = A + B$$



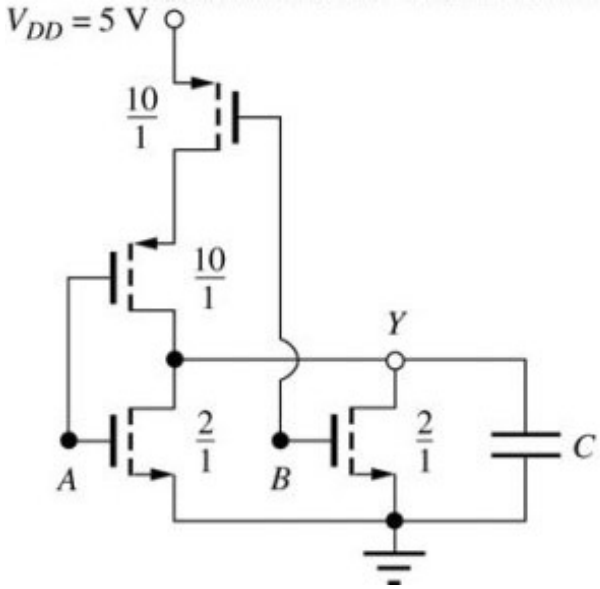
$$Y = \overline{A + B}$$

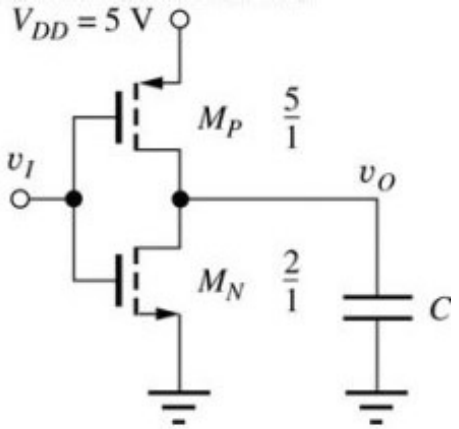
TABLE 7.3
CMOS NOR Gate Truth Table and Transistor States

A	B	$Y = \overline{A + B}$	NMOS-A	NMOS-B	PMOS-A	PMOS-B
0	0	1	Off	Off	On	On
0	1	0	Off	On	On	Off
1	0	0	On	Off	Off	On
1	1	0	On	On	Off	Off

Gate Sizing

- Want to keep the delay times the same as a reference inverter under the worst case input conditions.
- Consider a two-input NOR gate:
  - $(W/L)_n$ should be same as that of the inverter
  - $(W/L)_p$ should be twice as large as that of the inverter





Reference Inverter

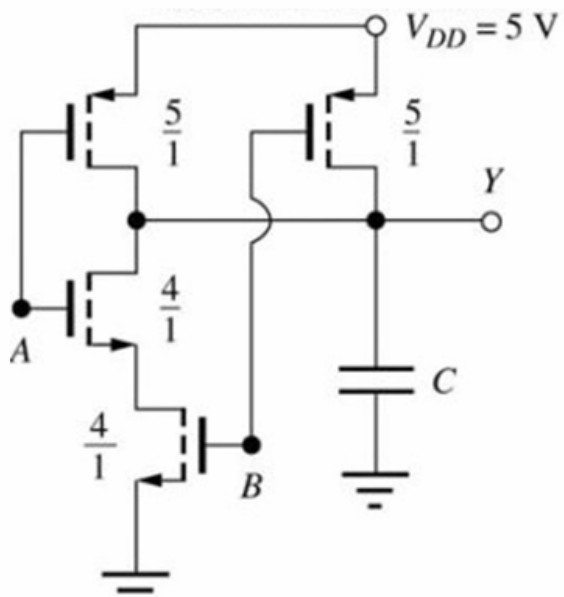
CMOS NAND Gate

Pull-up Network:

$$Y = \overline{A} + \overline{B}$$

Pull-down Network:

$$\overline{Y} = AB$$



$$Y = \overline{AB}$$

TABLE 7.5
CMOS NAND Gate Truth Table and Transistor States

A	B	$Y = \overline{AB}$	NMOS-A	NMOS-B	PMOS-A	PMOS-B
0	0	1	Off	Off	On	On
0	1	1	Off	On	On	Off
1	0	1	On	Off	Off	On
1	1	0	On	On	Off	Off