Week 8: MOSFET I-V Characteristics, DC Analysis and Small Signal Model

Topics to cover …

- MOSFET Non-ideal I-V Characteristics
- P-channel Devices and Other types
- DC Analysis of MOSFET circuits
- MOSFET Small Signal Model
- Reading Assignment:
  Chap 4.1 - 4.4, 4.9 and 13.8 of Jaeger and Blalock or
  Chap 4.1 - 4.6 of Sedra & Smith

Summary of NMOS I-V Characteristics

Region	Cutoff	Triode	Saturation
Conditions	$v_{GS} < V_t$	$v_{GS} \geq V_t$	
		$v_{DS} < v_{GS} - V_t$	$v_{DS} \geq v_{GS} - V_t$
I-V relation	$i_D = 0$	$i_D = K'_n \frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right]$	$i_D = \frac{1}{2}K'_n \frac{W}{L}(v_{GS} - V_t)^2$

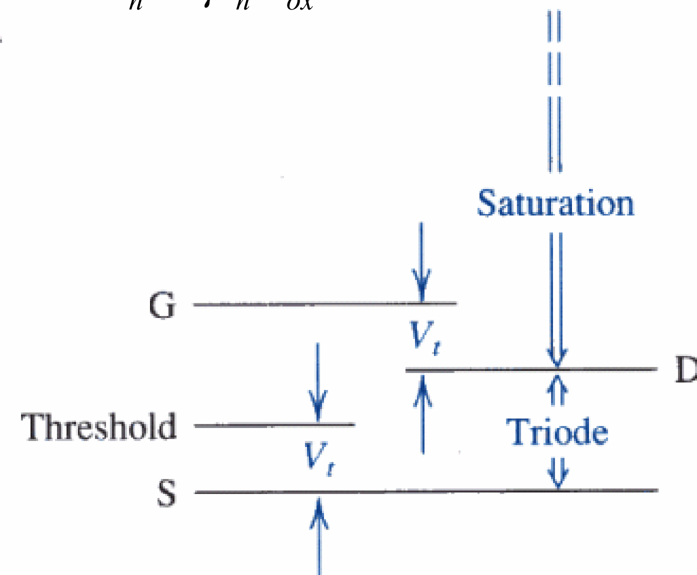
$$K_n' = \mu_n C_{ox}$$

- Cutoff region $v_{GS} < V_t$
- Triode region

$$v_{GS} \geq V_t \quad \text{and}$$
$$v_{DS} < v_{GS} - V_t$$

- Saturation region

$$v_{GS} \geq V_t \quad \text{and}$$
$$v_{DS} \geq v_{GS} - V_t$$



Ideal Characteristics of I_D vs V_{DS}

i_D (mA)

$v_{DS} \leq v_{GS} - V_t$

Triode region

$v_{DS} \geq v_{GS} - V_t$

Saturation region

$v_{DS} = v_{GS} - V_t$

$v_{GS} = V_t + 4$

$v_{GS} = V_t + 3$

$v_{GS} = V_t + 2$

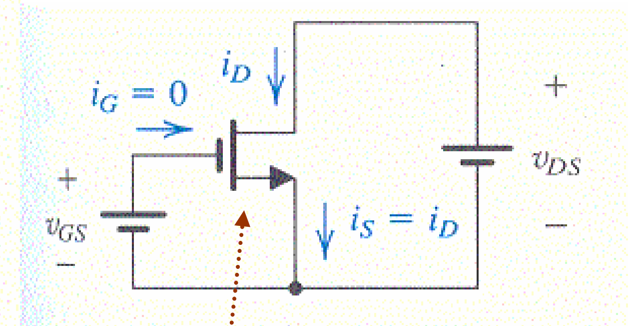
$v_{GS} = V_t + 1$

0 1 2 3 4 5 6 7 8 9 v_{DS} (V)

1 2 3 4

$v_{GS} \leq V_t$ (cut off)

(b)

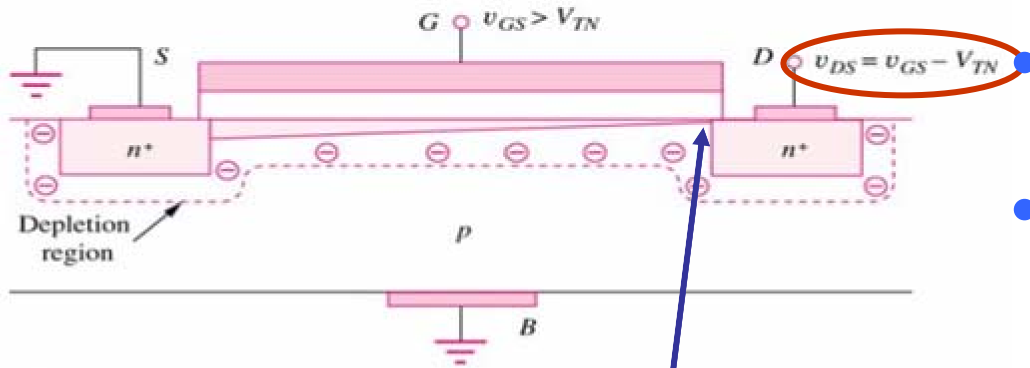


NMOS

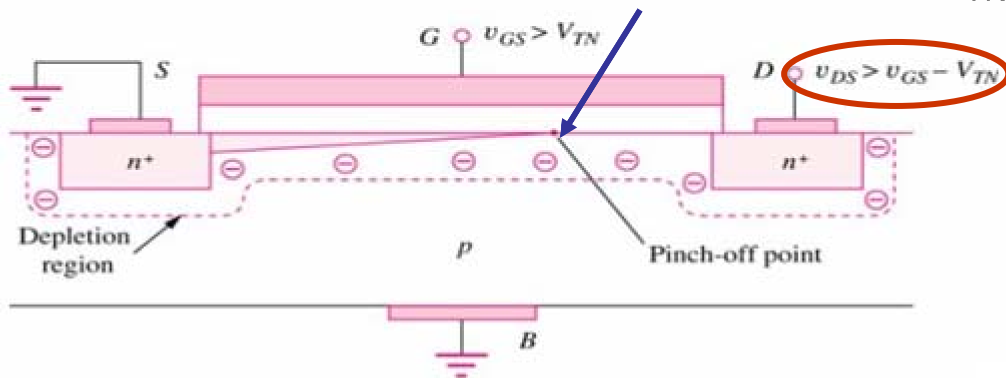
Non-ideal I-V Characteristics

- Finite Output Resistance in Saturation
- The role of the Body
- Temperature Effects
- Breakdown and Input Protection

Channel-Length Modulation

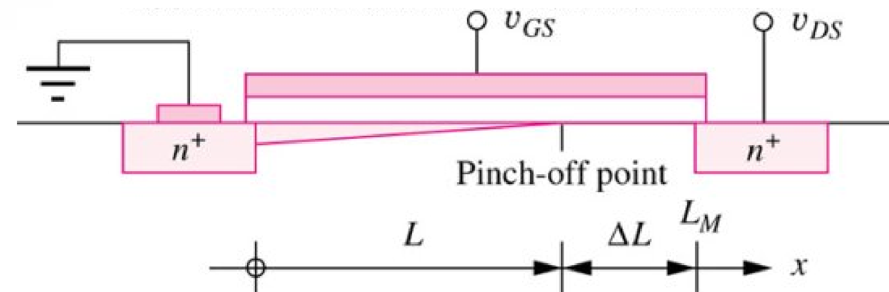


where gate-to-channel voltage = V_{TN}

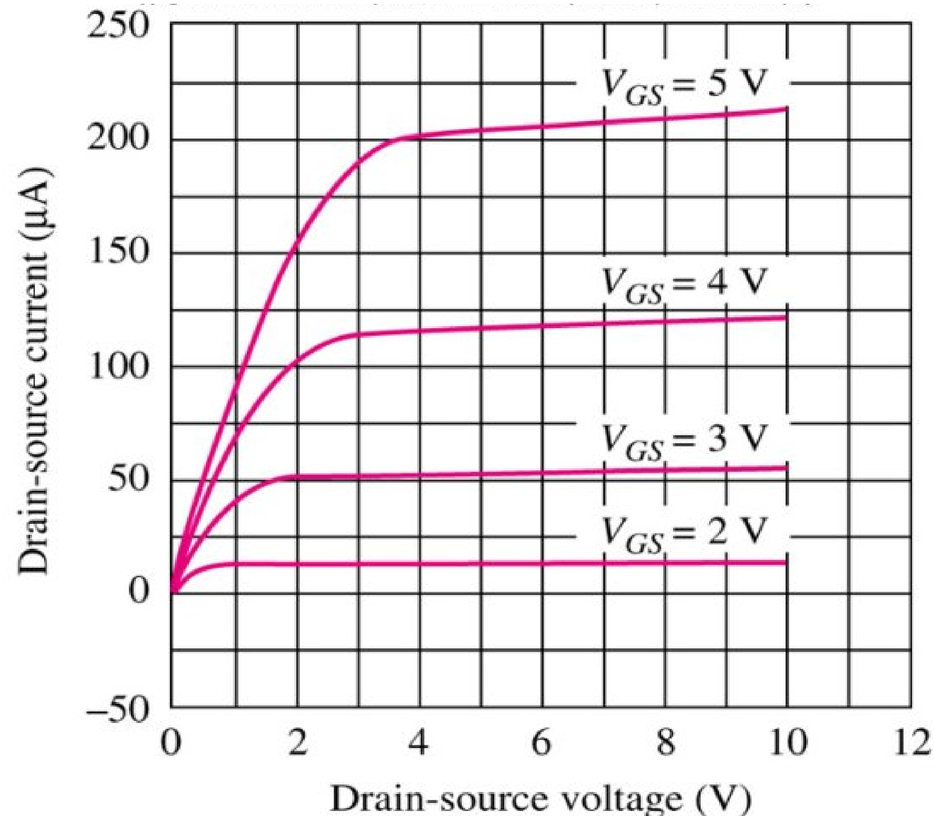


- At $v_{DS}=v_{GS}-V_{TN}=V_{DSsat}$,
  - Channel pinch-off
- As v_{DS} increases beyond v_{DSsat}, the pinch-off point moves away from D towards S
  - Effective channel length L is reduced, or that channel length is modulated by V_{DS}.
  - I_D increases with V_{DS}.
  - Output resistance is finite in saturation mode.

$$i_D = \frac{K_n'}{2}\frac{W}{L}\left(v_{GS} - V_{TN}\right)^2$$



Channel-Length Modulation

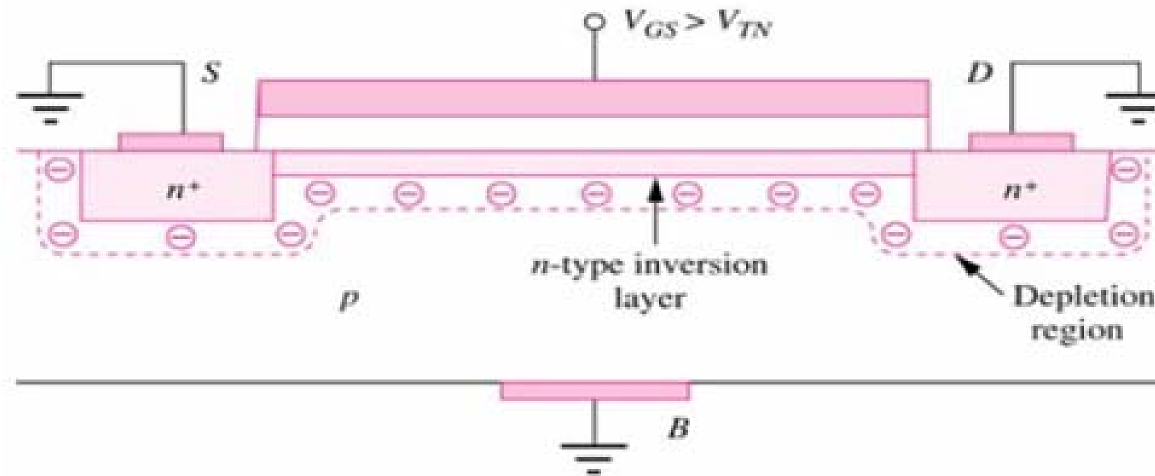


- This effect is modeled by adding a term $(1+\lambda v_{DS})$ to the I-V equation:

$$i_D = \frac{K_n'}{2}\frac{W}{L}\left(v_{GS} - V_{TN}\right)^2\left(1 + \lambda v_{DS}\right)$$

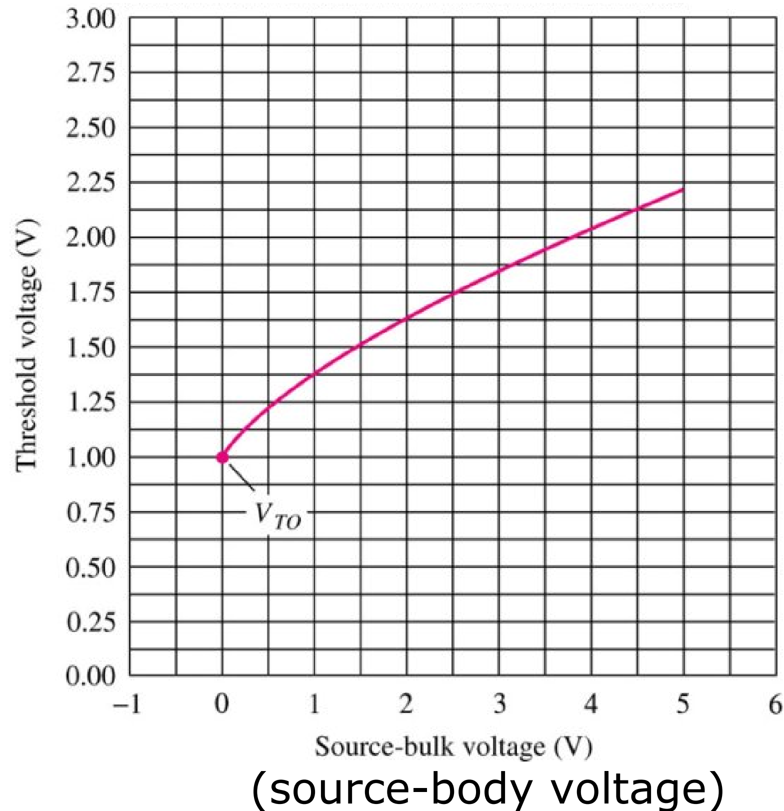
λ = channel length modulation parameter

The Role of Body - Body Effect



- Channel-body can be regarded as a *pn* junction
- If channel-body junction is reverse-biased,
  - Depletion layer beneath the gate oxide becomes wider
  - Since the amount of negative charges in the (channel + depletion) layer = amount of positive charges in the gate (Constant for a fixed gate-source voltage)
    → Channel depth is reduced
  - This is equivalent to an increase in the threshold voltage

Body Effect



(source-body voltage)

- Non-zero v_{SB} changes threshold voltage:

$$V_{TN} = V_{TO} + \gamma\left(\sqrt{v_{SB} + 2\phi_F} - \sqrt{2\phi_F}\right)$$

where

V_{TO}= zero substrate bias for V_{TN} (V)

γ= body-effect parameter ($\sqrt{\text{V}}$)

$2\Phi_F$= surface potential parameter (V)

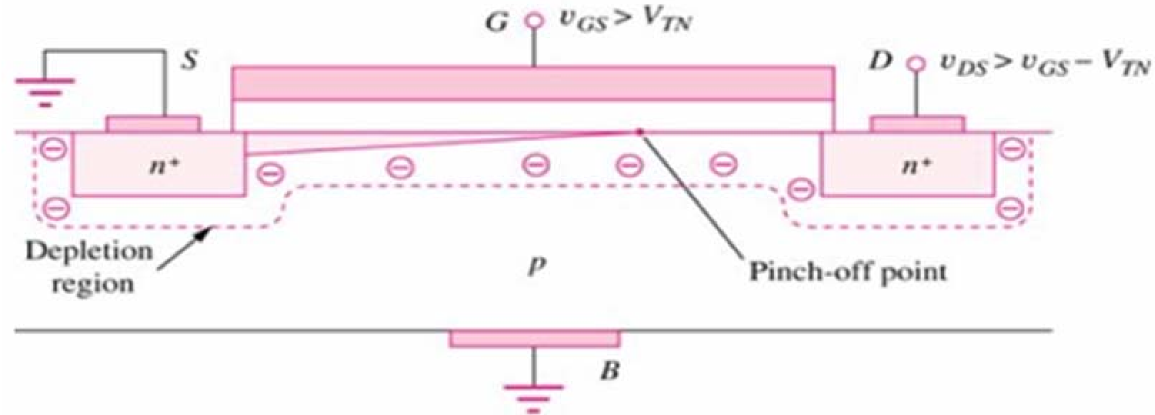
It follows that the body voltage controls i_D.
This phenomenon is known as the **body effect**.

Temperature Effects

- V_t and mobility μ are sensitive to temperature:
  - V_t decreases by 2mV for every 1ºC rise in temperature
  - mobility μ decreases with temperature

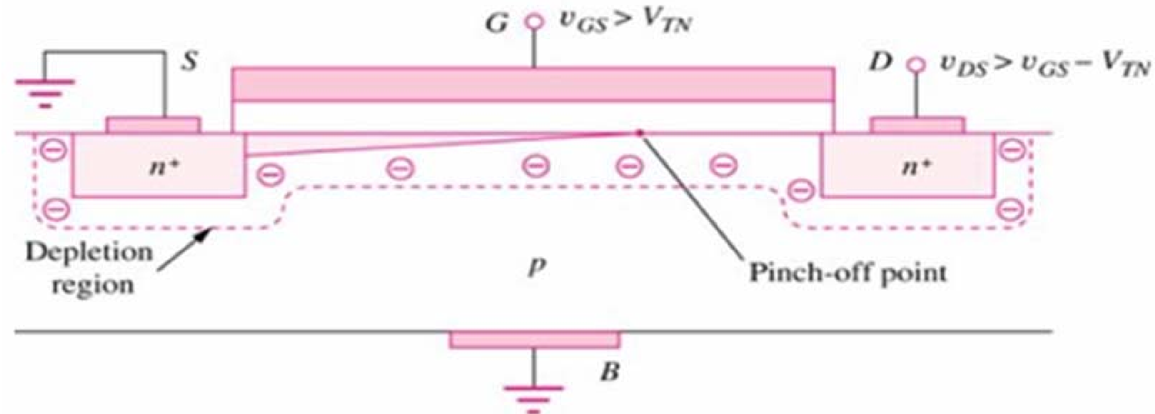
- Overall, increase in temperature results in lower drain currents

Avalanche Breakdown



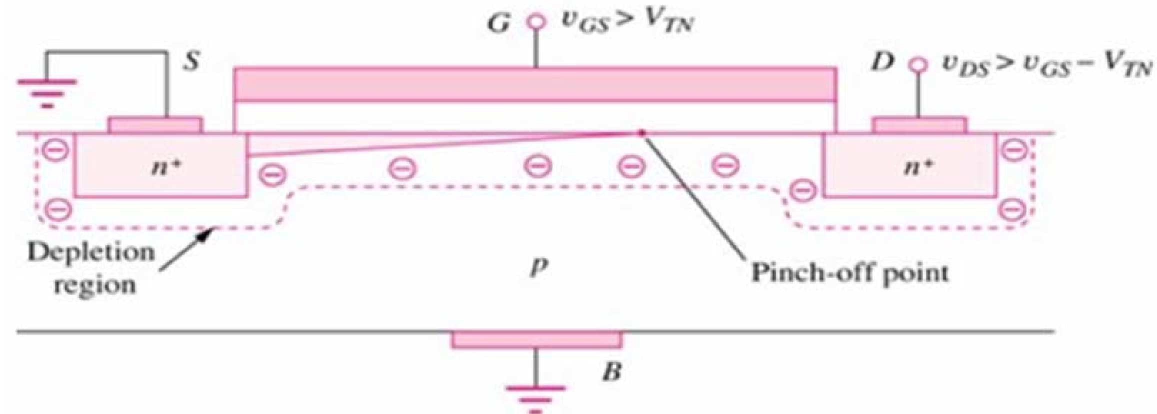
- As V_D is increased, the drain-body junction becomes reversed biased
  → Breakdown occurs at voltages of 20 to 150V
  → Rapid increase in the drain current
- Normally, no permanent damage to the device

Punch-through Breakdown



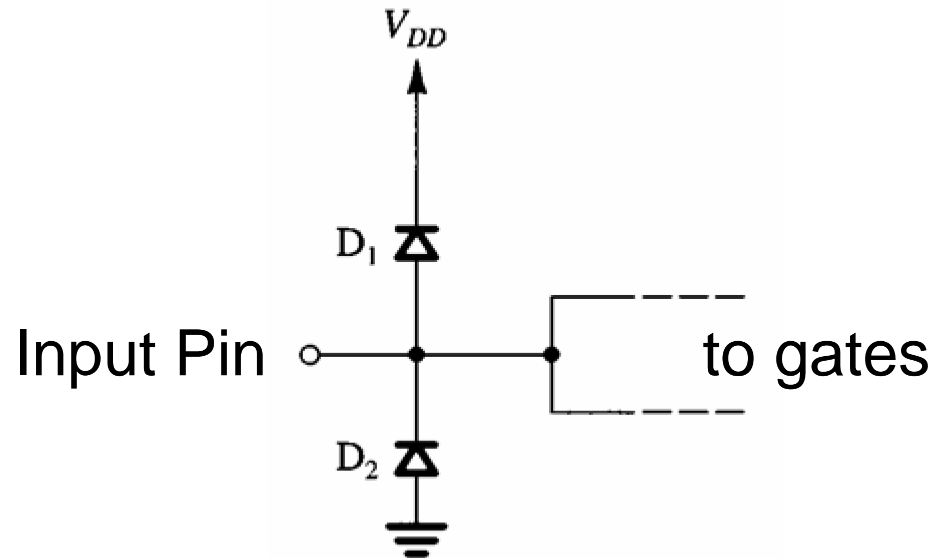
- Whe V_D is increased to a point, → the depletion region surrounding D extends to the S → Punch-through breakdown (about 20 V)
- Occurs in devices with short channels
- Normally, no permanent damage to the device

Gate-Oxide Breakdown



- When V_{GS} exceeds about 30 V (or lower in modern IC technology) → Gate oxide breaks down like in the case of a capacitor
- Results in permanent damage to the device

Input Protection



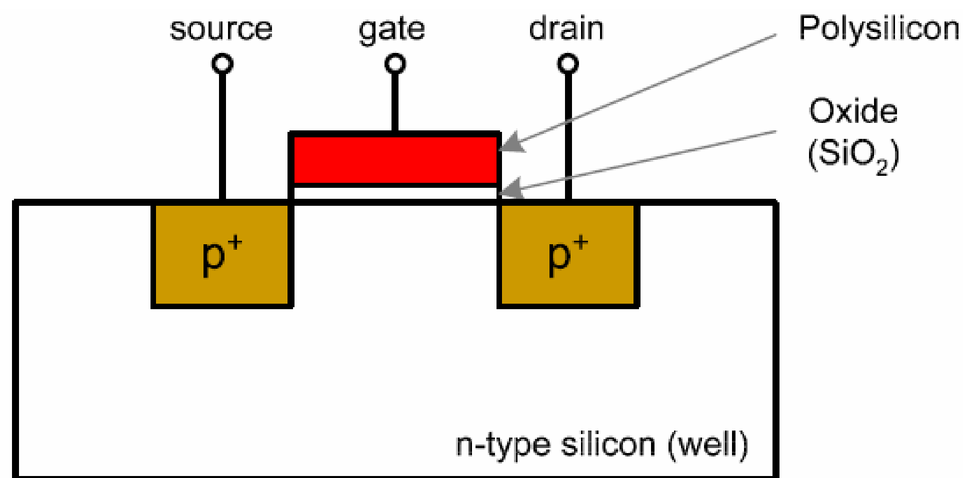
- Since the MOSFET has a very small input capacitance and a very high input resistance, a small amount of static charges accumulating on the gate can cause the gate voltage to exceed the breakdown level
  - e.g., Electrostatic Discharge (ESD) from human body
- Clamping diodes can be used in the I/O pins to protect the circuit from gate-oxide breakdown

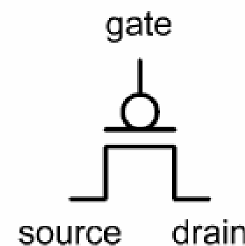
Topics to cover …

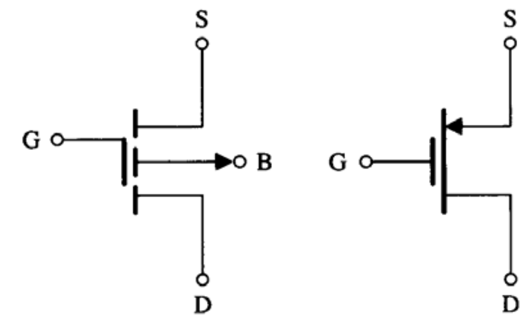
- MOSFET Non-ideal I-V Characteristics
- P-channel Devices and Other types
- DC Analysis of MOSFET circuits
- MOSFET Small Signal Model

P-channel MOSFET (PMOS)

- Similar to NMOS, but doping and voltages reversed
  - Body tied to highest voltage (Vdd) to prevent forward-biasing pn junctions
  - Source typically tied to Vdd too
  - Gate voltage high: transistor is OFF
  - Gate voltage low: transistor is ON when $V_{GS} < V_t$ (threshold voltage)
    - Inverted channel of positively charged holes
  - v_{GS} and v_{DS} are negative and V_t is also negative

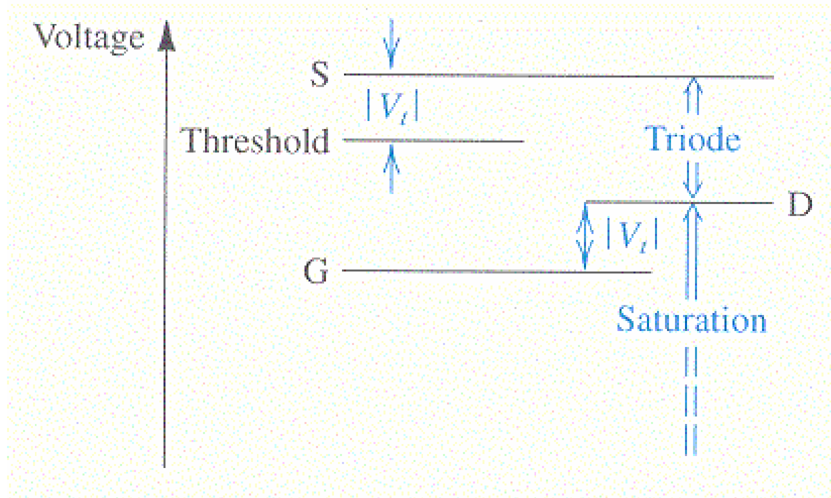






Symbols

PMOS I-V Characteristics



V_t, v_{GS} and v_{DS} are negative.

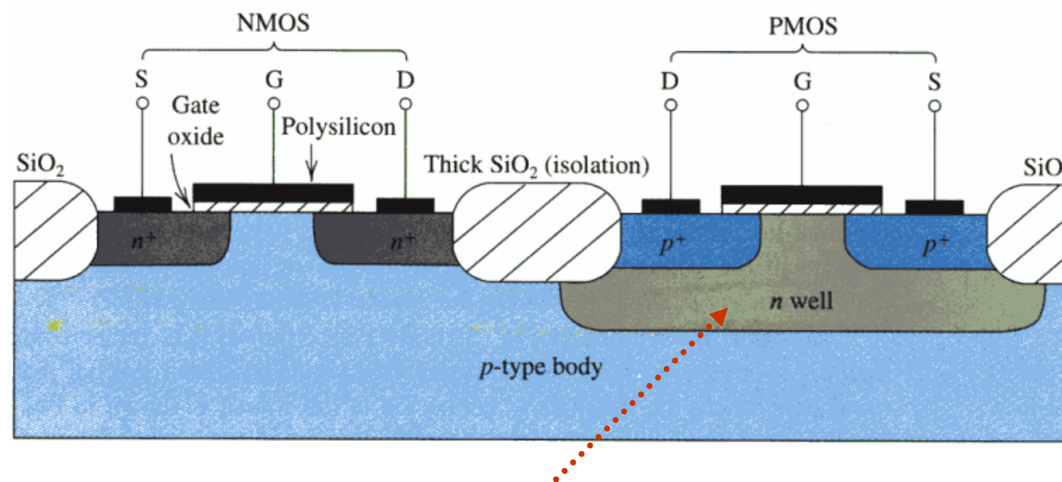
- Cutoff region $|v_{GS}| < |V_t|$
- Triode region
  $|v_{GS}| \geq |V_t|$ and
  $|v_{DS}| < |v_{GS} - V_t|$
- Saturation region
  $|v_{GS}| \geq |V_t|$ and
  $|v_{DS}| \geq |v_{GS} - V_t|$

Cutoff	Triode/Linear	Saturation
$i_D = 0$	$i_D = K_p\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right]$	$i_D = \frac{1}{2}K_p(v_{GS} - V_t)^2$

where $K_p = K_p'\frac{W}{L}$, $K_p' = \mu_p C_{ox}$

μ_p is typically 2 to 3 times lower than μ_n

Complementary MOS (CMOS) Technology

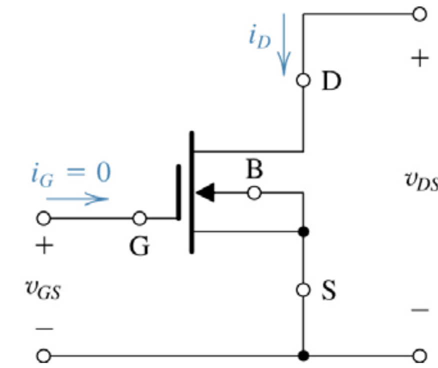


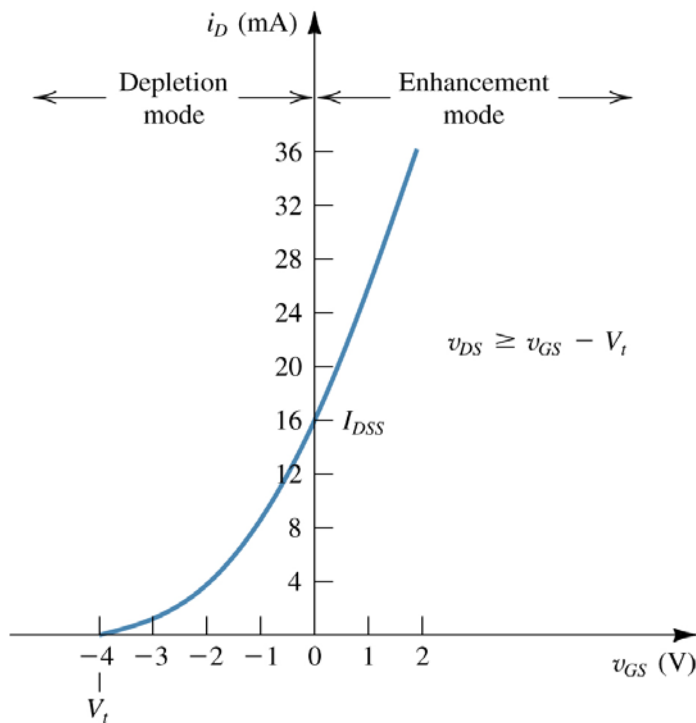
PMOS transistor is fabricated in the ***n* well**

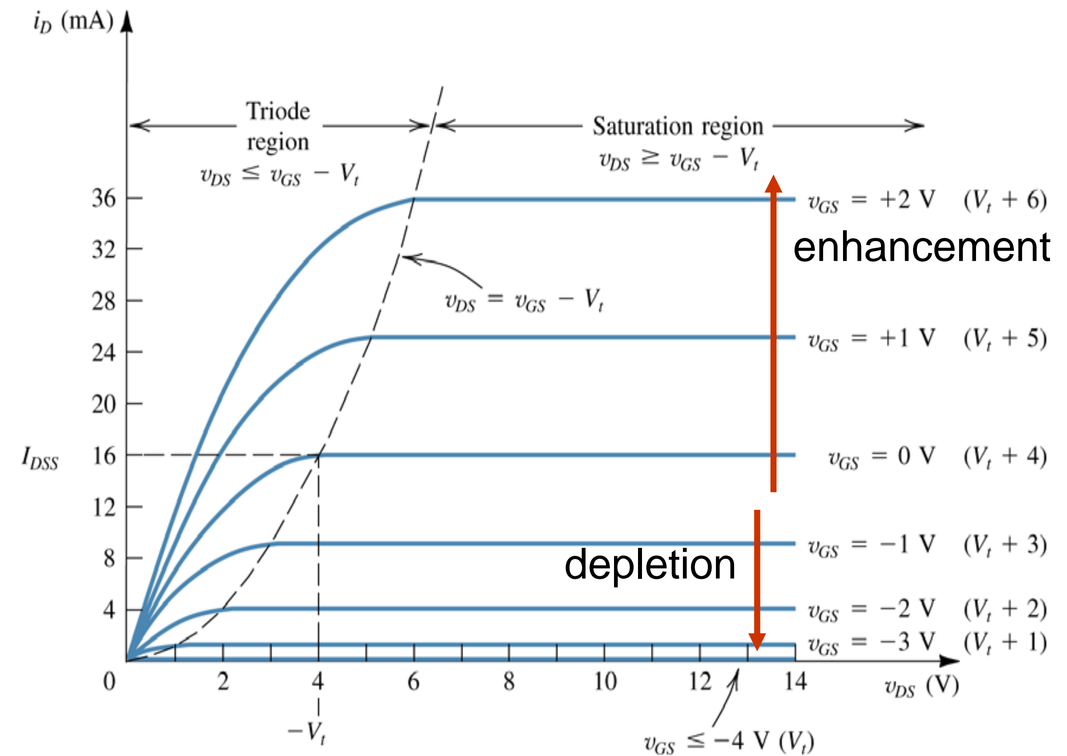
Complementary MOS or CMOS integrated-circuit technologies provide both NMOS and PMOS on a same IC

Depletion-mode MOSFET

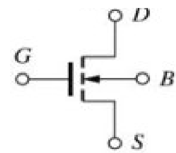
- A depletion-type MOSFET has a built-in channel by fabrication
  - It is ON when no gate-source voltage is applied
  - Must apply a negative v_{GS} to turn off device
- V_t is negative for NMOS



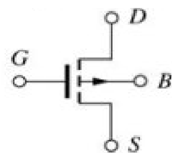




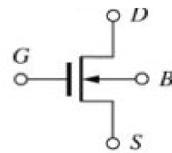
MOSFET Circuit Symbols



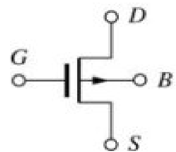
(a) NMOS enhancement-mode device



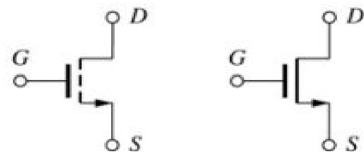
(b) PMOS enhancement-mode device



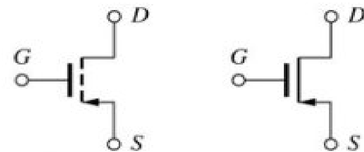
(c) NMOS depletion-mode device



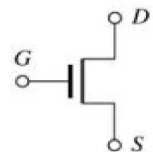
(d) PMOS depletion-mode device



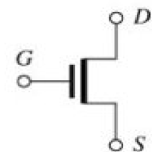
(e) Three-terminal NMOS transistors



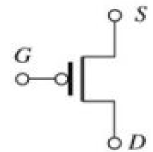
(f) Three-terminal PMOS transistors



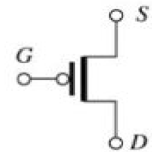
(g) Shorthand notation—NMOS enhancement-mode device



(h) Shorthand notation—NMOS depletion-mode device



(i) Shorthand notation—PMOS enhancement-mode device



(j) Shorthand notation—PMOS depletion-mode device

- (g) and(i) are the most commonly used symbols in VLSI logic design.
- MOS devices are symmetric.
- In NMOS, n^+ region at higher voltage is the drain.
- In PMOS p^+ region at lower voltage is the drain

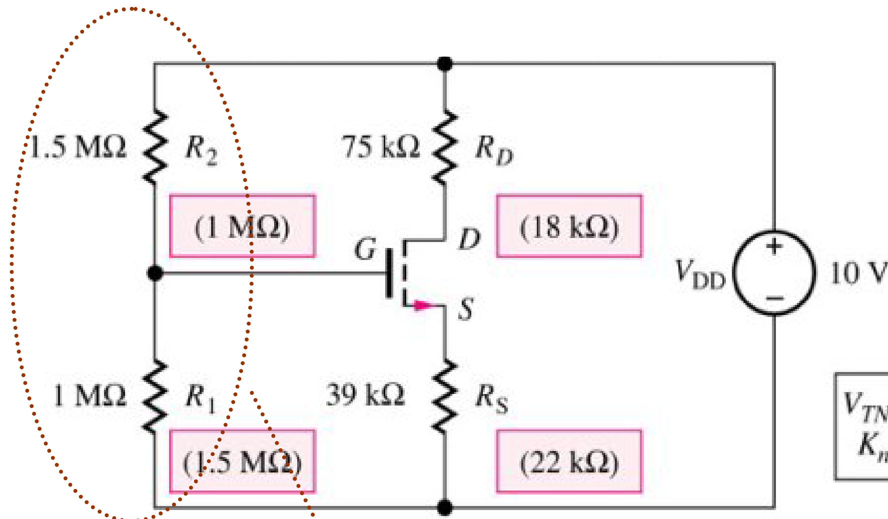
Topics to cover …

- MOSFET Non-ideal I-V Characteristics
- P-channel Devices and Other types
- DC Analysis of MOSFET circuits
- MOSFET Small Signal Model

DC Analysis Approach

- Assume an operation mode (usually the saturation mode)
- Use circuit analysis to find V_{GS}
- Use V_{GS} to calculate I_D, and I_D to find V_{DS}
- Check validity of operation region assumptions
- Change assumptions and analyze again if required.

Example 1

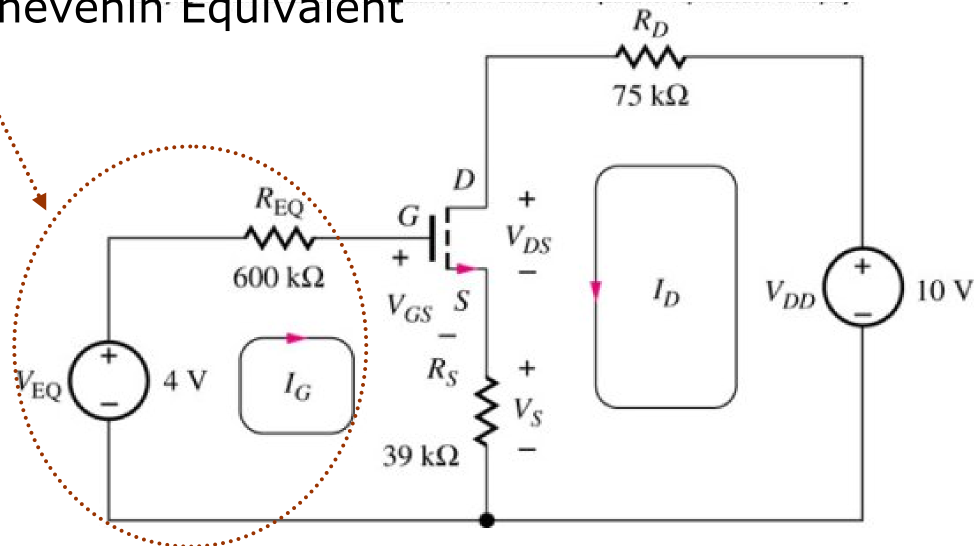


Problem: Find Q-pt (I_D, V_{DS})

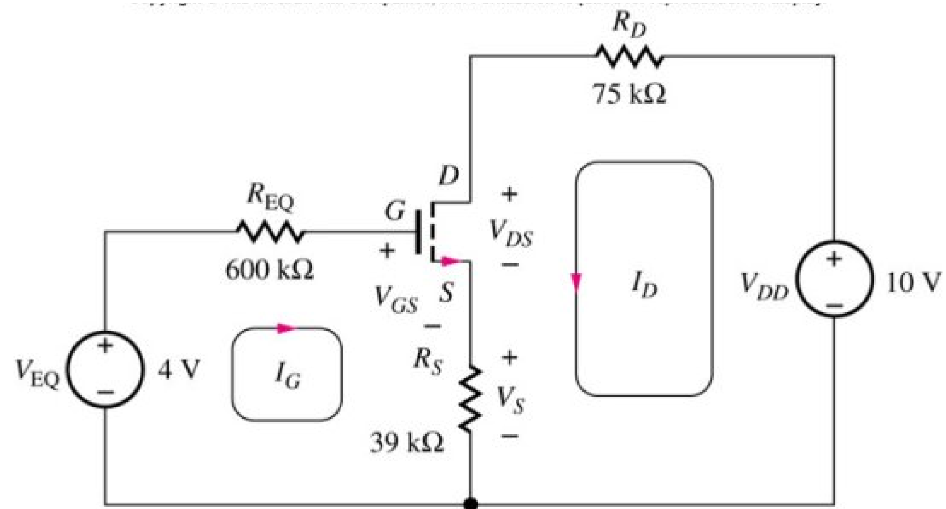
$V_{TN} = 1$ V
$K_n = 25\ \mu A/V^2$

Assumption: Transistor is saturated.
Analysis: Simplify the circuit,

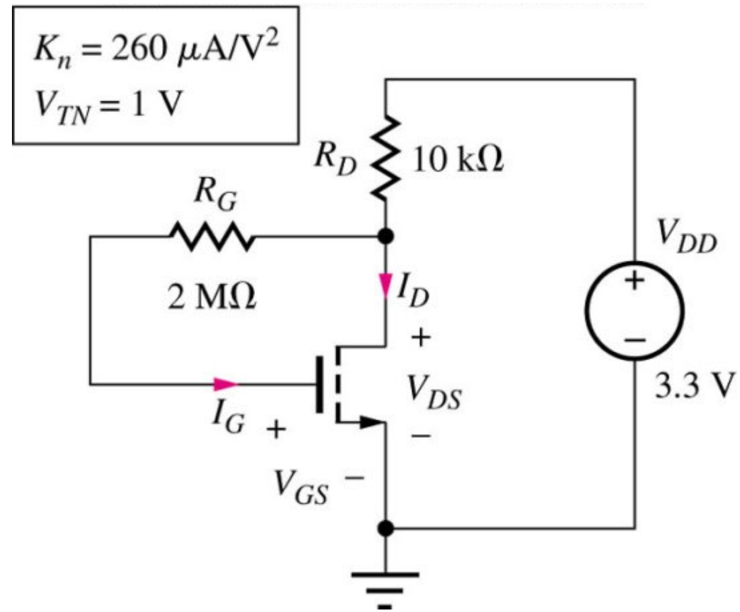
Thevenin Equivalent



Example 1



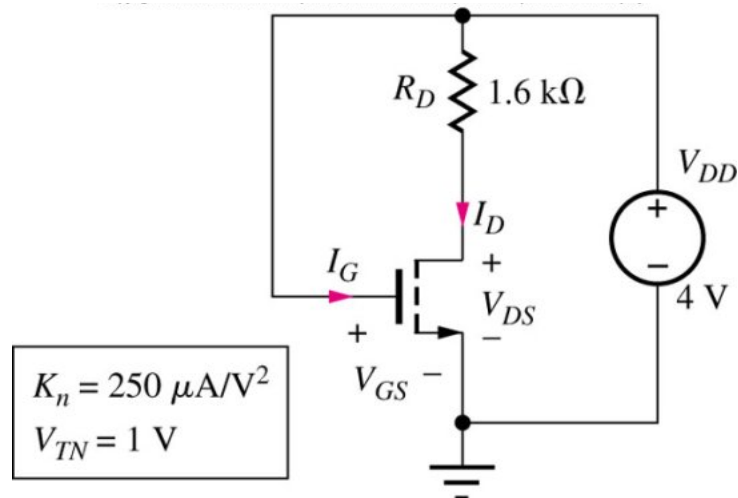
Example 2



Problem: Find Q-pt (I_D, V_{DS})

Assumption: Transistor is saturated
(since $V_{DS}= V_{GS}$)

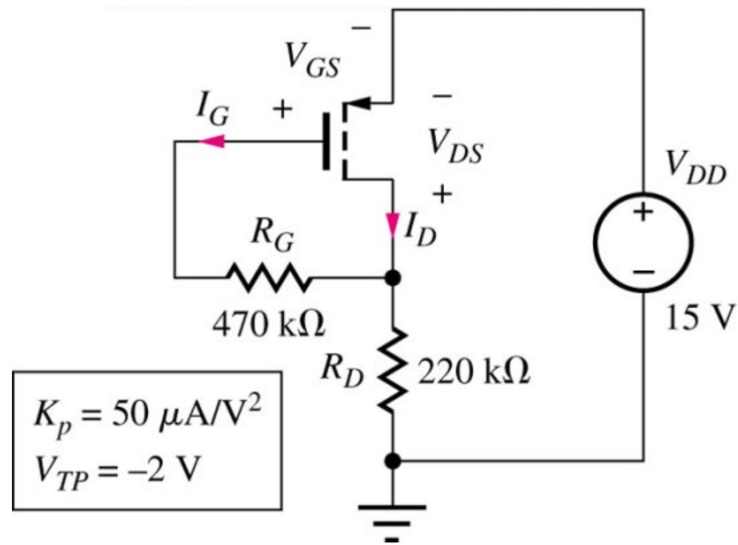
Example 3



Problem: Find Q-pt (I_D, V_{DS})

Assumption: transistor is saturated

Example 4 (PMOS)

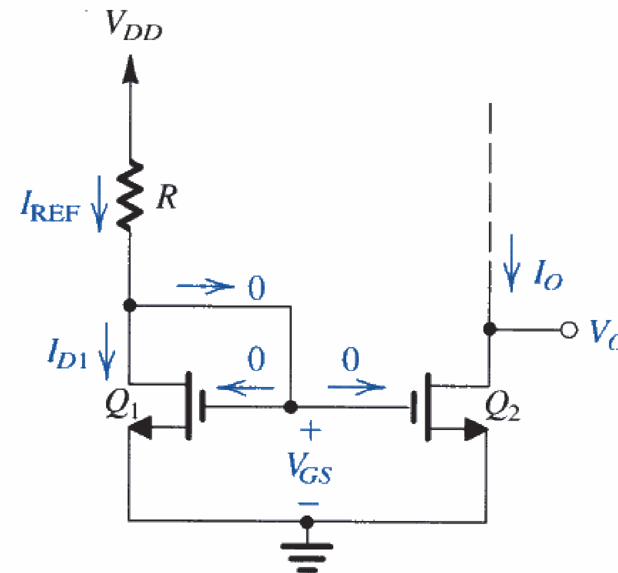


Problem: Find Q-pt (I_D, V_{DS})

Assumption: transistor is saturated (since $V_{DS} = V_{GS}$)

Current Mirror

Current Mirror is an important building block in IC amplifiers.



As Q_1 must be in saturation mode,

$$I_{D1} = \frac{1}{2}k_n'\left(\frac{W}{L}\right)_1 (V_{GS} - V_t)^2$$

$$I_{D1} = I_{REF} = \frac{V_{DD} - V_{GS}}{R}$$

If Q_2 operates in saturation,

$$I_O = I_{D2} = \frac{1}{2}k_n'\left(\frac{W}{L}\right)_2 (V_{GS} - V_t)^2$$

$$\frac{I_O}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1}$$

If $(W/L)_2=(W/L)_1$, $I_O=I_{REF}$, output mirrors the input.

Note that channel modulation effect is neglected.

Current Steering Circuit

Once a constant current is generated, it can be replicated to provide dc bias currents for the various amplifier stages in an IC.

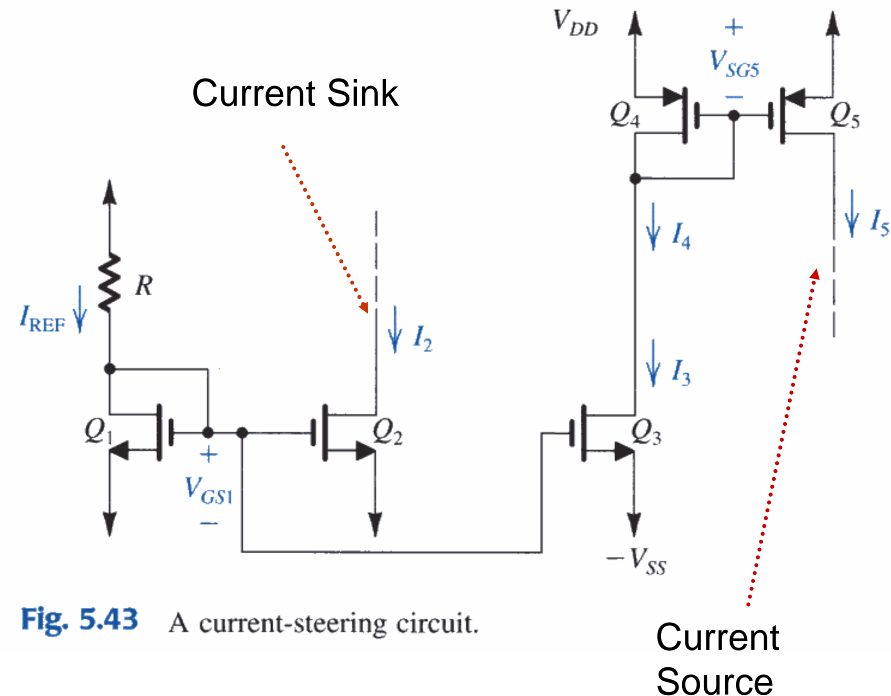


Fig. 5.43 A current-steering circuit.

Assume Q_2, Q_3 and Q_5 are in active mode.

$$I_2 = I_{REF} \frac{(W/L)_2}{(W/L)_1}$$

$$I_3 = I_{REF} \frac{(W/L)_3}{(W/L)_1}$$

$$I_5 = I_4 \frac{(W/L)_5}{(W/L)_4} \qquad \text{where} \quad I_4 = I_3$$

Topics to cover …

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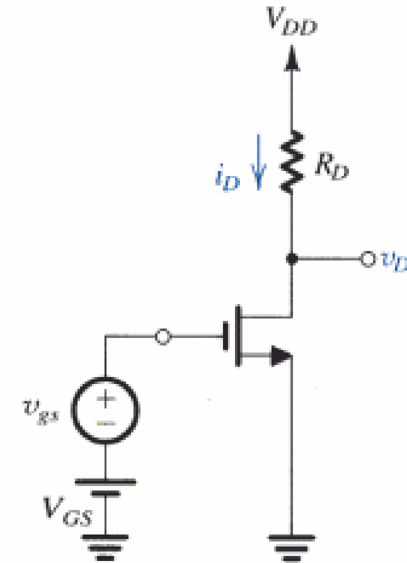
Big Picture: Large Signal Analysis

For the conceptual MOSFET amplifier shown right,



$$v_{GS} = V_{GS} + v_{gs}$$

$$i_D = \frac{1}{2}k_n'\frac{W}{L}(V_{GS} + v_{gs} - V_t)^2$$

$$= \frac{1}{2}k_n'\frac{W}{L}(V_{GS} - V_t)^2 + k_n'\frac{W}{L}(V_{GS} - V_t)v_{gs} + \frac{1}{2}k_n'\frac{W}{L}v_{gs}^2$$

For small input signal that $\frac{1}{2}k_n'\frac{W}{L}v_{gs}^2 << k_n'\frac{W}{L}(V_{GS} - V_t)v_{gs}$

which results in $\boxed{v_{gs} << 2(V_{GS} - V_t)}$ $V_{gs}<0.2(V_{GS} - V_t)$ is commonly required.

we obtain, $$i_D = \underbrace{\frac{1}{2}k_n'\frac{W}{L}(V_{GS} - V_t)^2}_{I_D} + \underbrace{k_n'\frac{W}{L}(V_{GS} - V_t)v_{gs}}_{i_d}$$

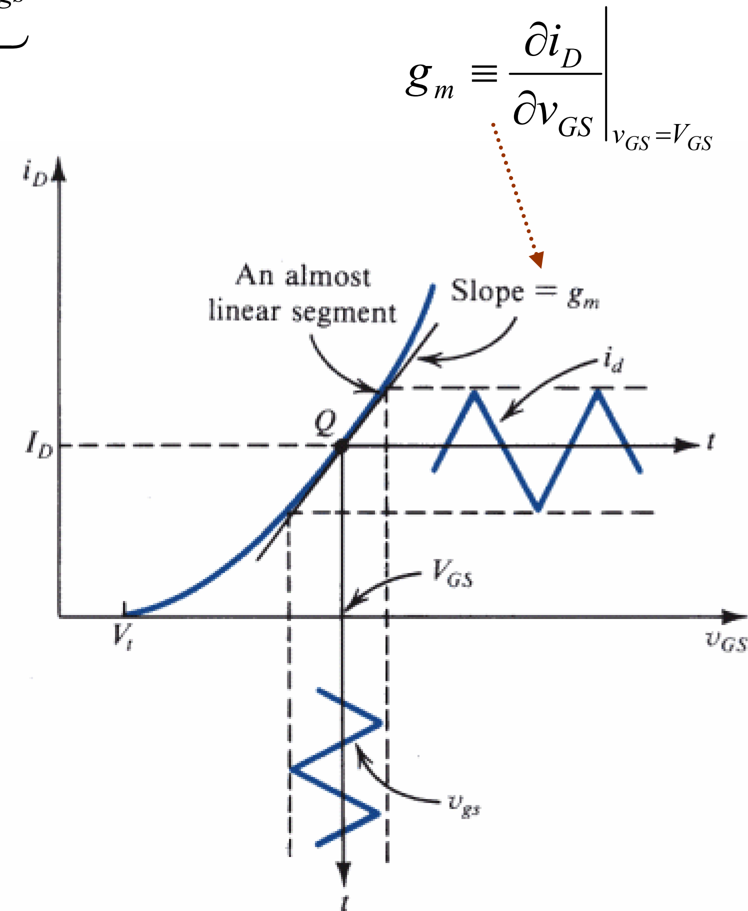
Small Signal Transconductance g_m

$$i_D = \underbrace{\frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2}_{I_D} + \underbrace{k_n' \frac{W}{L} (V_{GS} - V_t) v_{gs}}_{i_d}$$

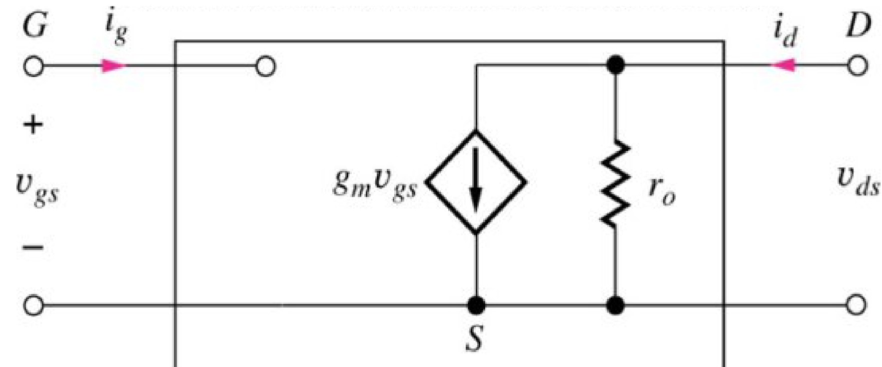
$$g_m \equiv \left. \frac{\partial i_D}{\partial v_{GS}} \right|_{v_{GS} = V_{GS}}$$

$$\Rightarrow \quad g_m = \frac{i_d}{v_{gs}} = k_n' \frac{W}{L} (V_{GS} - V_t)$$

Graphic interpretation:



Small Signal Model



MOSFET small signal model

$$g_m \equiv \left. \frac{\partial i_D}{\partial v_{GS}} \right|_{v_{GS} = V_{GS}} = \frac{i_d}{v_{gs}} = k_n' \frac{W}{L}(V_{GS} - V_t)$$

$$r_0 \equiv \left[\frac{\partial i_D}{\partial v_{DS}} \right]^{-1}_{v_{GS} = \mathrm{V_{GS}}} = \frac{1 + \lambda V_{DS}}{\lambda I_D} \cong \frac{1}{\lambda I_D}$$

r_o is output resistance due to channel length modulation effect.

Observations on Transconductance

Formula 1: $g_m = k_n' \frac{W}{L}(V_{GS} - V_t)$

It shows:

$g_m \propto k'$, W/L, and $(V_{GS} - V_t)$

Formula 2: $g_m = \sqrt{2k_n'}\sqrt{\frac{W}{L}}\sqrt{I_D}$

It shows:

(1) For a given MOSFET,

$$g_m \propto \sqrt{I_D}$$

(2) At a given bias current,

$$g_m \propto \sqrt{W/L}$$

In contrast, the g_m of BJT $\propto I_C$ and is independent of the geometry.

Reference equations:

$$I_D = \frac{1}{2}k'_n \frac{W}{L}(V_{GS} - V_t)^2$$

$$(V_{GS} - V_t) = \sqrt{\frac{2I_D}{k'_n \frac{W}{L}}}$$

For BJT:

$$g_m = \frac{I_C}{V_T}$$

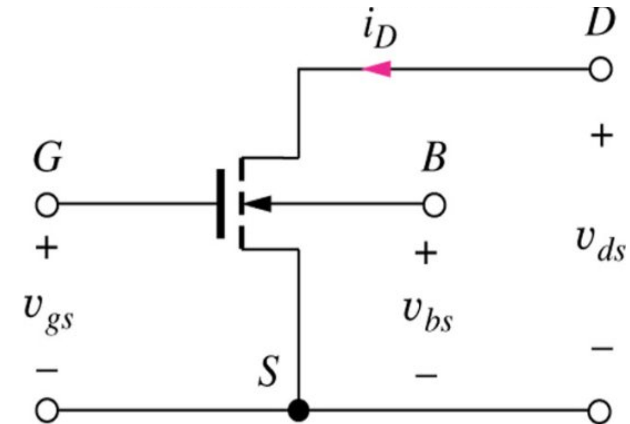
Formula 3: $g_m = \frac{I_D}{(V_{GS} - V_t)/2}$

The g_m of MOSFET is much small than that of BJT for that the values of $(V_{GS}-V_t)/2$ are at least 0.1V or so.

In spite of their low g_m, MOSFETs have many other advantages, such as high R_{in}, small size, low power dissipation and ease of fabrication.

Modeling the Body Effect

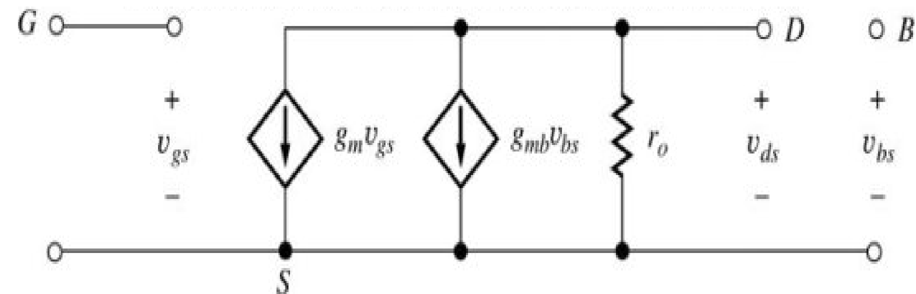
- S-to-B voltage affects threshold voltage and in turn the drain current
- This effect can be modeled by adding a ***back-gate transconductance***:



$$g_{mb} = \left.\frac{\partial i_D}{\partial v_{BS}}\right|_{Q-point} = -\left.\frac{\partial i_D}{\partial v_{SB}}\right|_{Q-point}$$

$$= -\left.\left(\frac{\partial i_D}{\partial V_{TN}}\right)\left(\frac{\partial V_{TN}}{\partial v_{SB}}\right)\right|_{Q-point} = \eta g_m$$

$0<\eta<1$ is called back-gate transconductance parameter.



- Body terminal is a reverse-biased diode. Hence, no current flows through it.