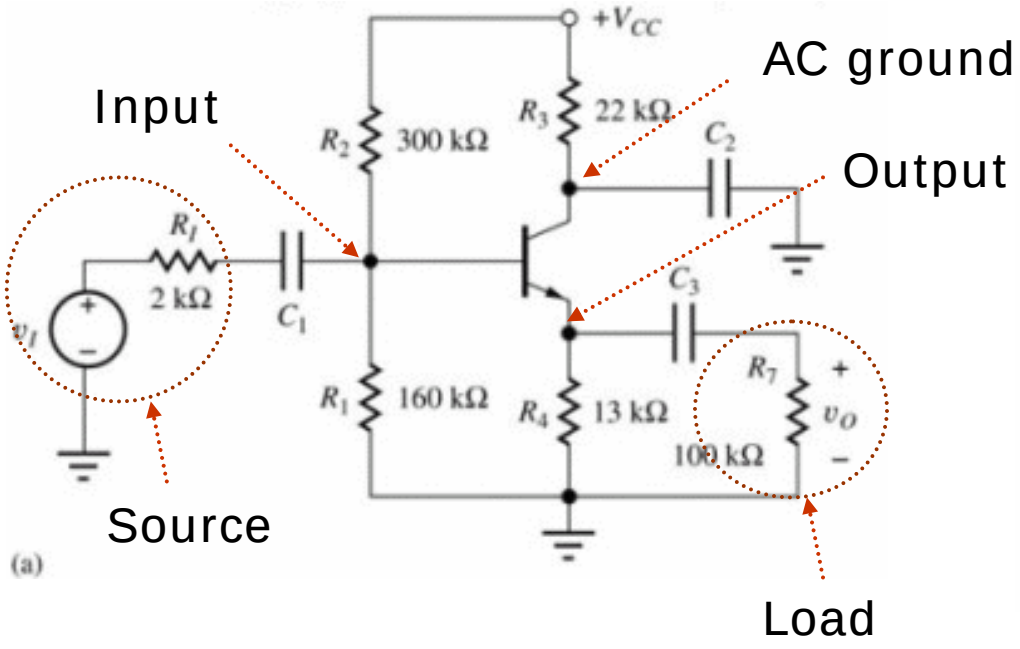
Week 7: Common-Collector Amplifier, MOS Field Effect Transistor

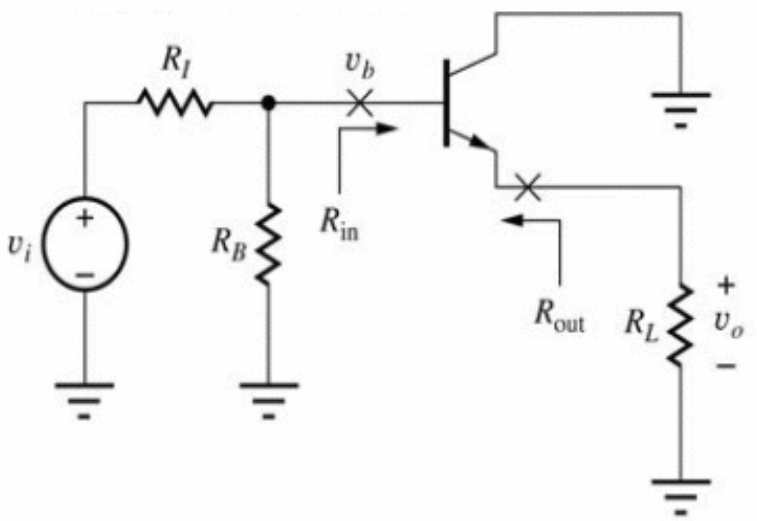
Topics to cover …

- Common-Collector Amplifier
- MOS Field Effect Transistor
  - Physical Operation and I-V Characteristics of n-channel devices
  - Non-ideal effects
  - P-channel devices and other types

- Reading Assignment:
  Chap 14.1 – 14.5 of Jaeger and Blalock , or
  Chap 5.7 of Sedra & Smith
  And
  Chap 4.1 – 4.4 of Jaeger and Blalock or
  Chap 5.1-5.2 of Sedra & Smith

Common-Collector Amplifier





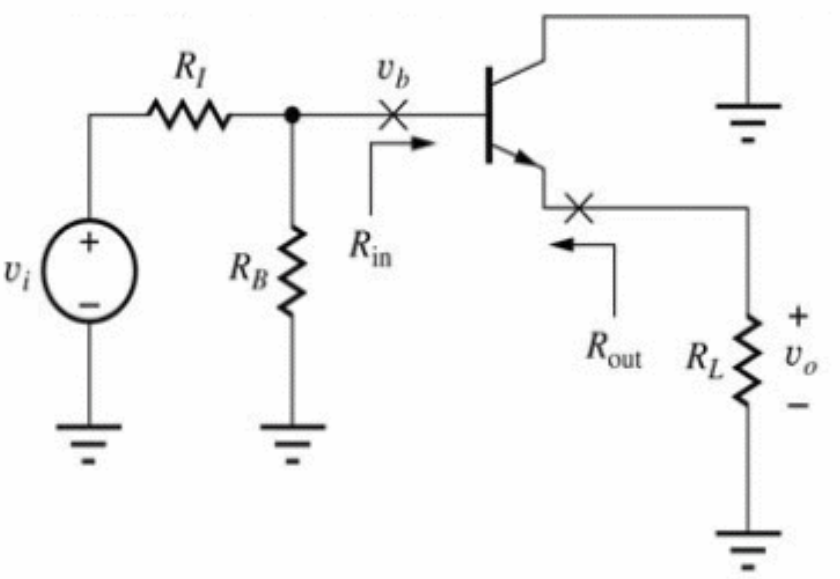
AC/Small signal equivalent

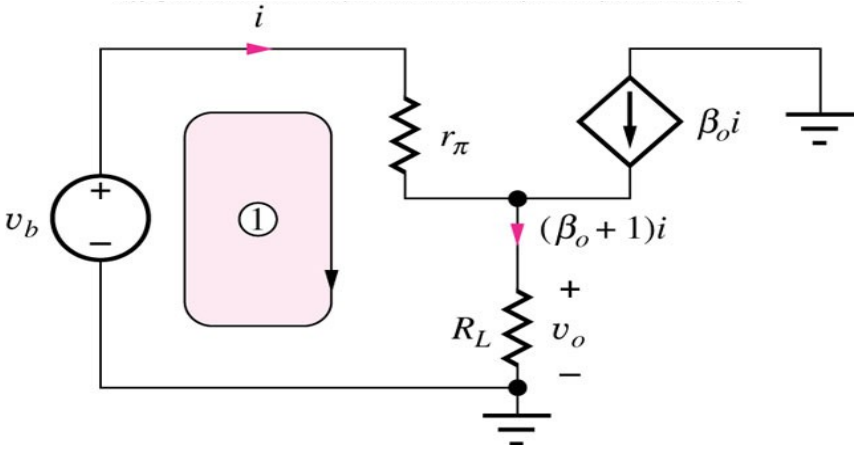
Also called “Emitter follower”

$$R_L = R_4 \parallel R_7$$

$$R_B = R_1 \parallel R_2$$

Terminal Voltage Gain





$$A_{vt}^{CC} = \frac{v_o}{v_b} = \frac{(\beta+1)R_L}{r_\pi + (\beta+1)R_L}$$

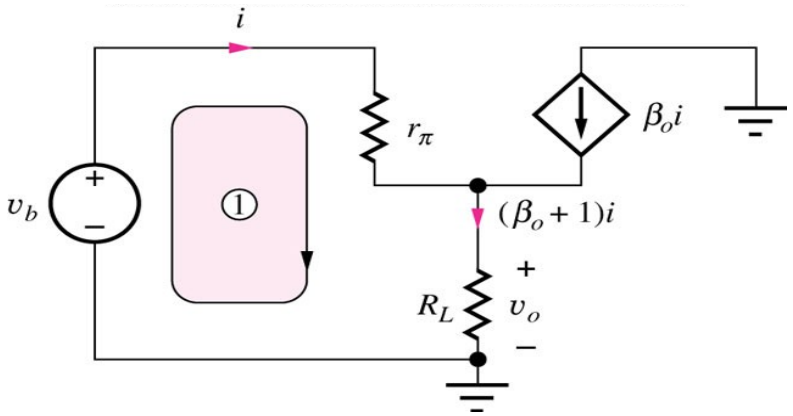
$$\therefore A_{vt}^{CC} \cong \frac{g_m R_L}{1 + g_m R_L} \quad \text{for} \quad \beta >> 1$$

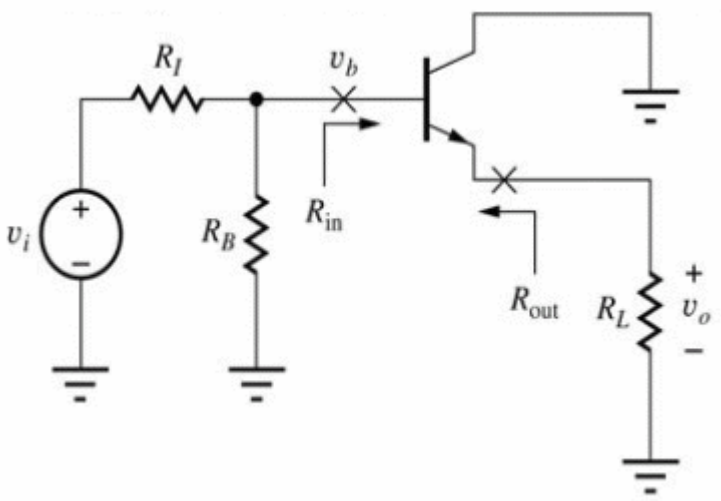
In most C-C amplifiers, $g_m R_L >> 1$

$$\therefore A_{vt}^{CC} \cong 1$$

Output voltage at emitter follows input voltage, hence the circuit is named ***Emitter Followers***.

Input Resistance and Overall Voltage Gain





Input resistance looking into the base terminal is given by

$$R_{in}^{CC} = \frac{v_b}{i} = r_\pi + (\beta + 1)R_L$$

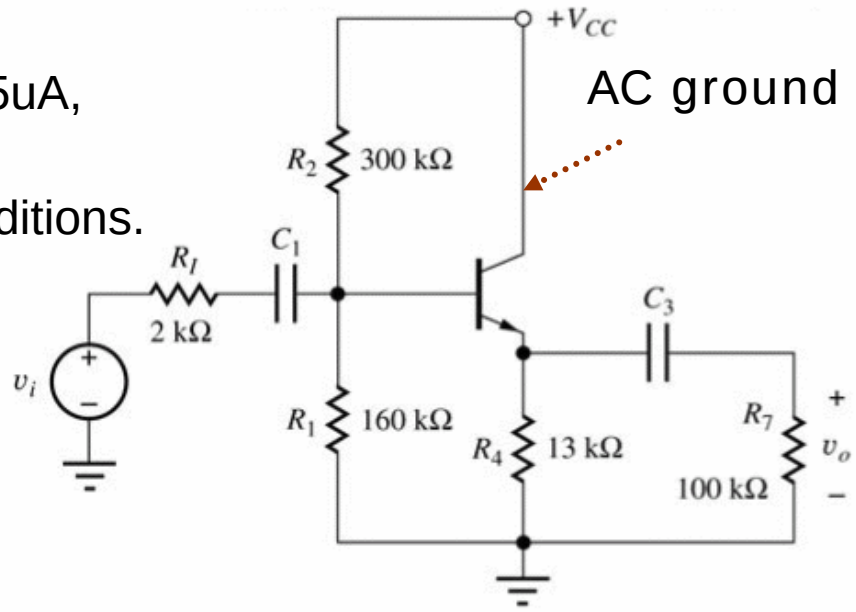
Overall voltage gain is

$$A_v^{CC} = \frac{v_o}{v_i} = \left(\frac{v_o}{v_b}\right)\left(\frac{v_b}{v_i}\right) = A_{vt}\left(\frac{v_b}{v_i}\right)$$

$$= A_{vt}^{CC}\left[\frac{R_B \| R_{in}^{CC}}{R_I + \left(R_B \| R_{in}^{CC}\right)}\right]$$

Example 1

- **Problem:** Find overall voltage gain.
- **Given data:** β=100, Q-point values: I_C=245uA, V_{CE}=3.64V, g_m=9.8mΩ^{-1}, r_π=10.2kΩ.
- **Assumptions:** Small-signal operating conditions.
- **Analysis:**



$$R_B = R_1 \| R_2 = 104k\Omega$$

$$R_L = R_4 \| R_7 = 11.5k\Omega$$

$$R_{in} = r_\pi + (\beta+1)R_L = 10.2k\Omega + 101(10.2k\Omega) = 1.17M\Omega$$

$$A_{vt} = \frac{g_m R_L}{1 + g_m R_L} = 0.991$$

$$A_v = A_{vt}\left[\frac{R_B \| R_{in}^{CC}}{R_I + \left(R_B \| R_{in}^{CC}\right)}\right] = 0.956$$

Input Signal Range

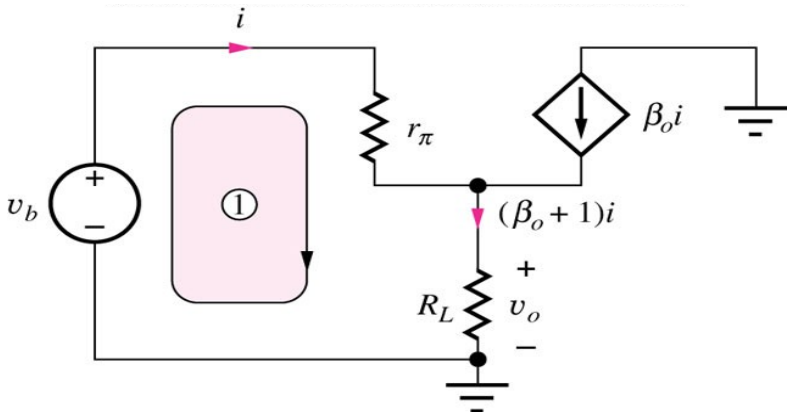
For small-signal operation, magnitude of v_{be} < 5 mV.

$$v_{be} = ir_\pi = \frac{v_b r_\pi}{r_\pi + (\beta+1)R_L} = \frac{v_b}{1 + g_m R_L + \dfrac{R_L}{r_\pi}}$$

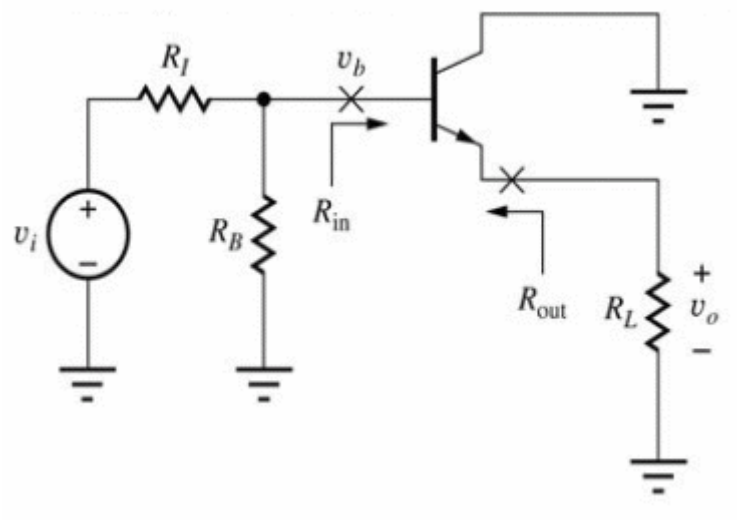
$$\left|v_b\right| \le 0.005\left(1 + g_m\left(R_L + \frac{R_L}{\beta}\right)\right) \cong 0.005(1 + g_m R_L)\,V$$

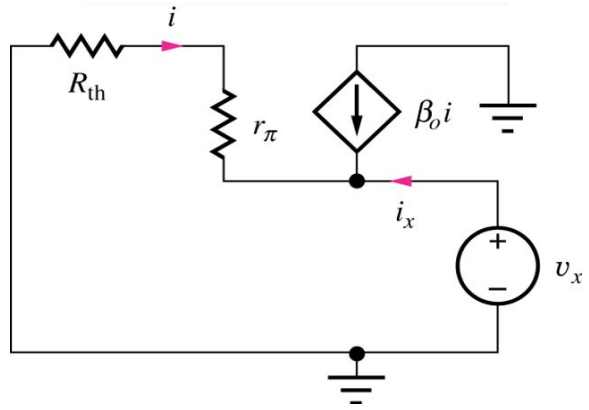
If $g_m R_L >> 1$, v_b can be increased beyond 5 mV limit.

Emitter followers can be used with relatively large input signals!



Output Resistance





$$R_{th} = R_I \,||\, R_B$$

$$i_x = -i - \beta i = \frac{v_x}{R_{th} + r_\pi} - \beta\left(-\frac{v_x}{R_{th} + r_\pi}\right)$$

$$\therefore R_{out}^{CC} \cong \frac{R_{th} + r_\pi}{\beta + 1} = \frac{r_\pi}{\beta + 1} + \frac{R_{th}}{\beta + 1}$$

$$R_{out}^{CC} = \frac{\alpha}{g_m} + \frac{R_{th}}{\beta + 1} \cong \frac{1}{g_m} + \frac{R_{th}}{\beta + 1}$$

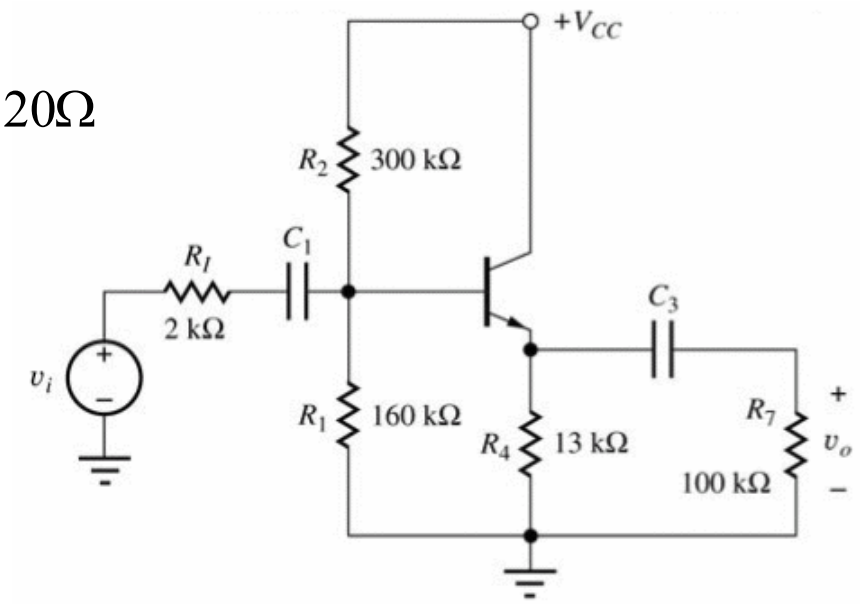
$$R_{out}^{CC} \cong \frac{1}{g_m} + \frac{R \text{ connected to base}}{\beta + 1}$$

Small output resistance!

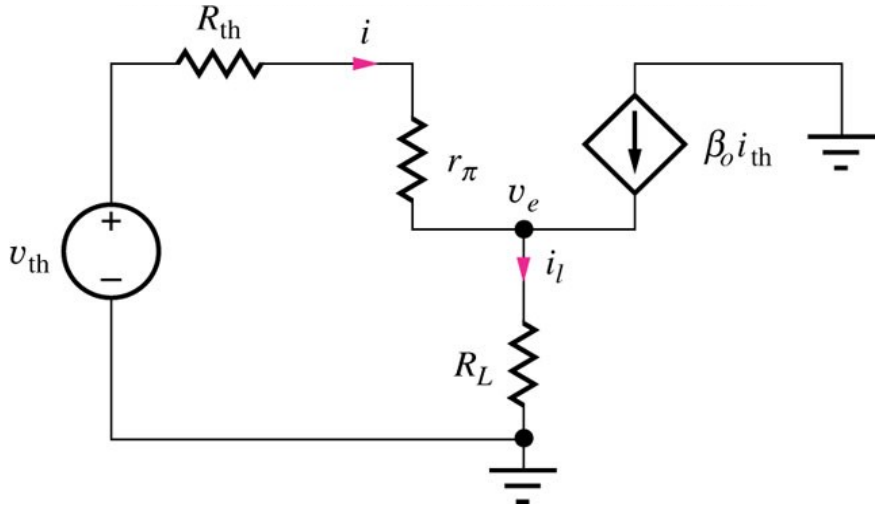
Example 2

- **Problem:** Find output resistance.
- **Given data:** β=100, Q-point values: I_C=245uA, V_{CE}=3.64V, g_m=9.8mS, r_π=10.2kΩ, r_o=219kΩ.
- **Assumptions:** Small-signal operating conditions.
- **Analysis:**

$$R_{out}^{CC} = \frac{\alpha}{g_m} + \frac{R_{th}}{\beta+1} = \frac{0.990}{9.80\text{mS}} + \frac{1.96\text{k}\Omega}{101} = 120\Omega$$



Current Gain



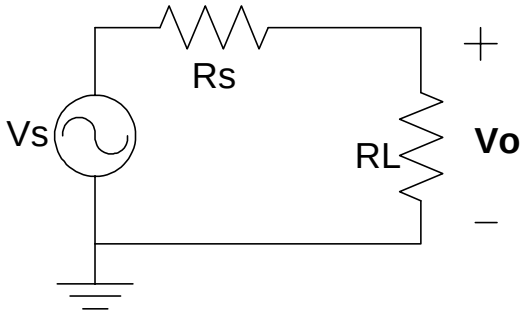
- Terminal current gain $A_{it}^{CC} = \frac{i_l}{i} = \beta + 1$

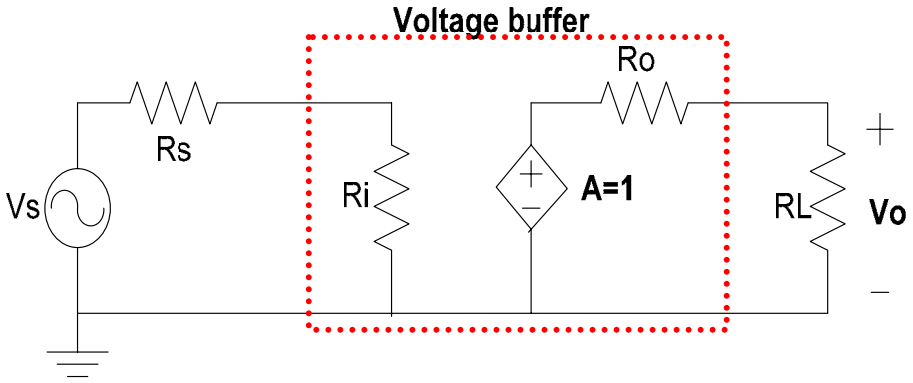
Summary of Emitter Follower

- *Voltage gain*: Close to unity.
- *Input resistance*: Large
- *Output resistance*: Small
- *Input signal range*: relatively large
- *Terminal current gain*: Large $(\beta+1)$

- Excellent for use as a voltage buffer

Voltage Buffer





Without buffer:

$$v_o = \frac{R_L}{R_s + R_L} v_s << v_s \quad \text{if} \quad R_L << R_s$$

With buffer:

$$v_o = \left(\frac{R_i}{R_S + R_i} v_s \right) A \frac{R_L}{R_L + R_O}$$

$$\cong A v_s = v_s \quad \text{for } R_i >> R_S \text{ and } R_O << R_L$$

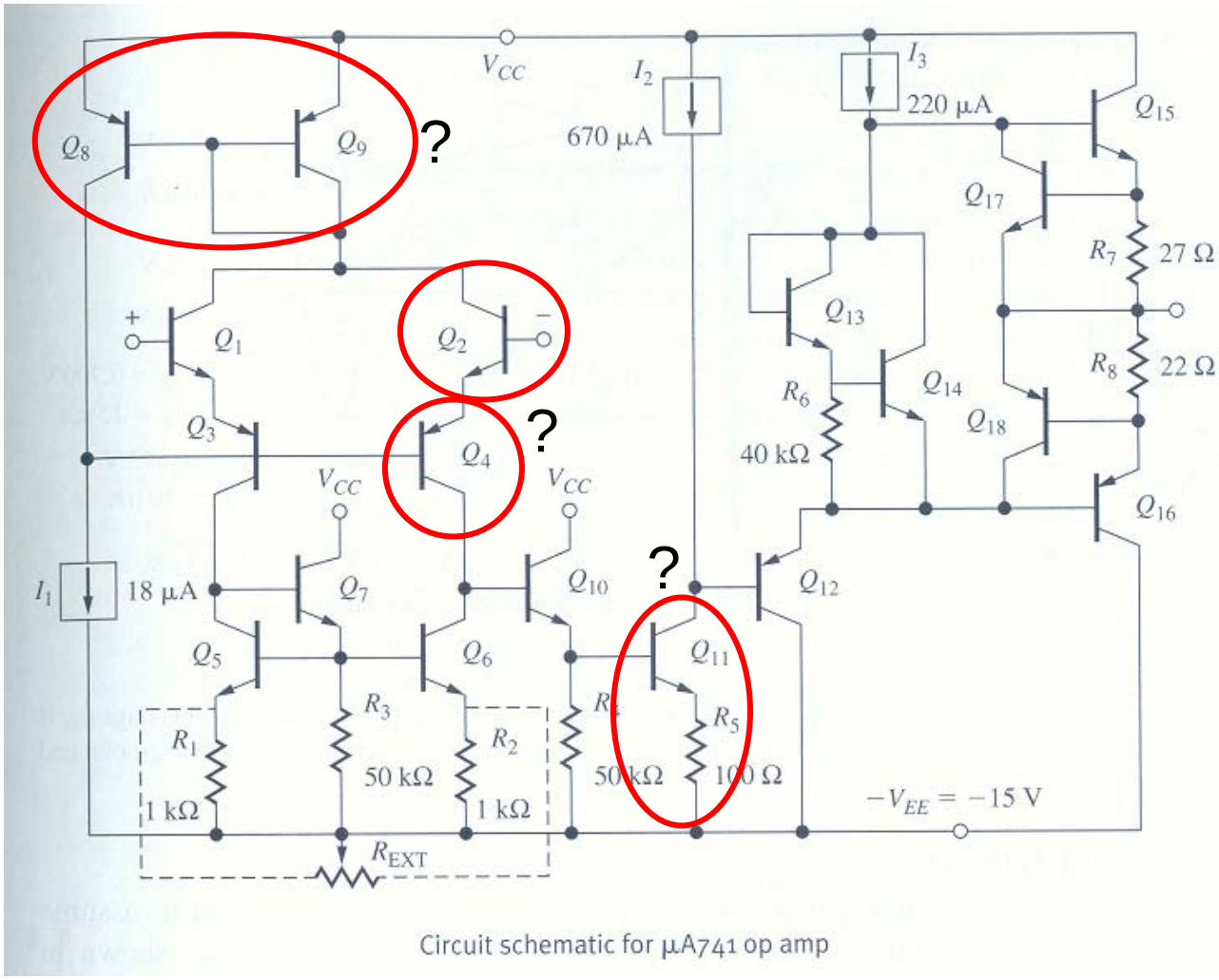
Requirement of voltage buffer:

- High input resistance
- Low output resistance
- Unity voltage gain

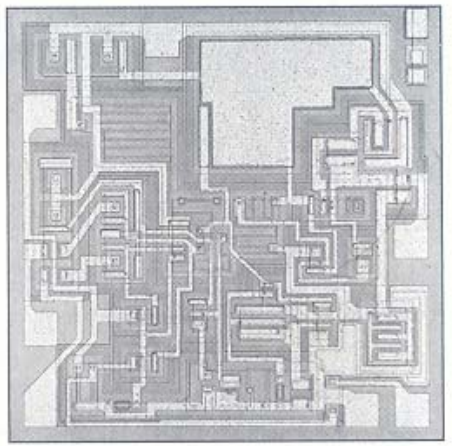
Summary of Single Stage BJT Amplifiers

	C-E (R_E=0)	Emitter Degenerated C-E	C-C	C-B
Terminal Voltage Gain	Inverting & large	Inverting & moderate	1	Non-inverting & Large
Input Resistance	Moderate	Large	Large	Low
Output Resistance	Moderate	Large	Low	Large
Input Voltage Range	Small	Moderate	Large	Moderate
Terminal Current Gain	Inverting & Large	Inverting & Large	Non-inverting & Large	1

More Complicated Amplifier …



Circuit schematic for μA741 op amp



uA741 Die Photograph (Courtesy of Fairchild Semiconductor)

741 Op-amp - Built from single stage amplifiers

Topics to cover …

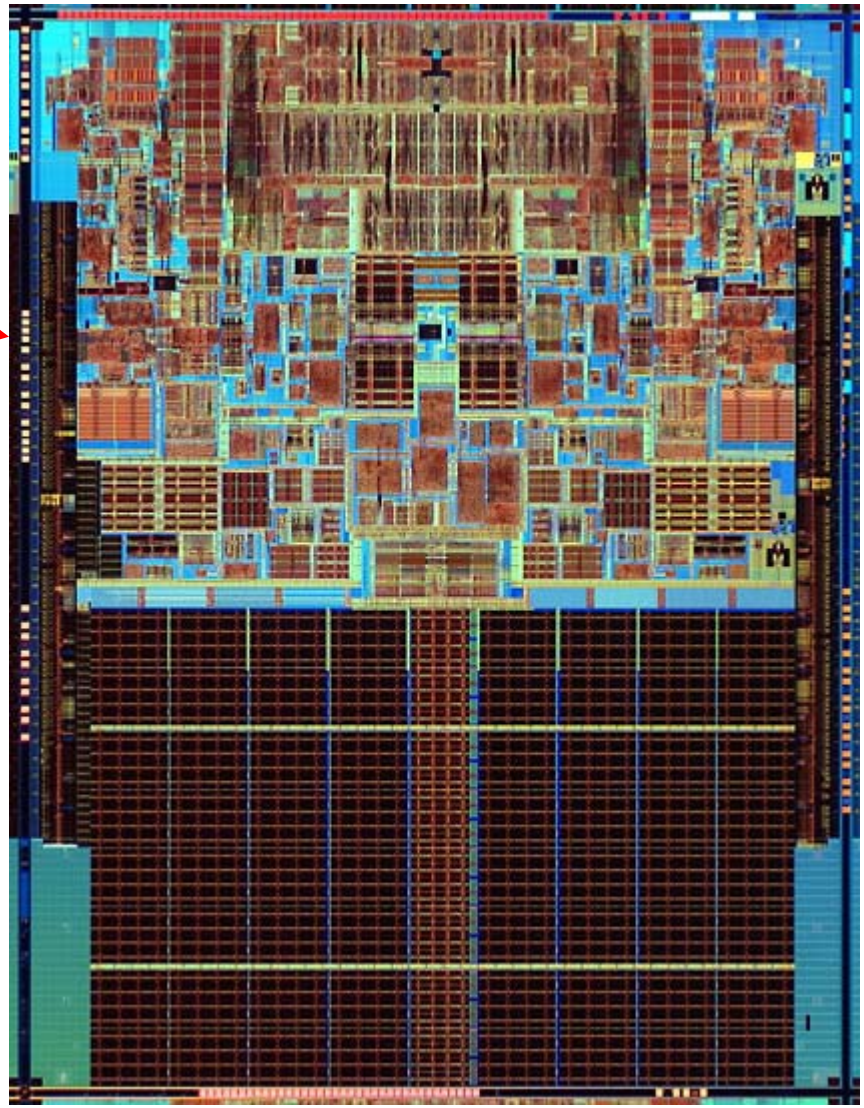
- Common-Collector Amplifier
- MOS Field Effect Transistor
  - Physical Operation and I-V Characteristics of n-channel devices
  - Non-ideal effects
  - P-channel devices and other types

Introduction

- Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET) is the primary component in high-density chips such as memories and microprocessors

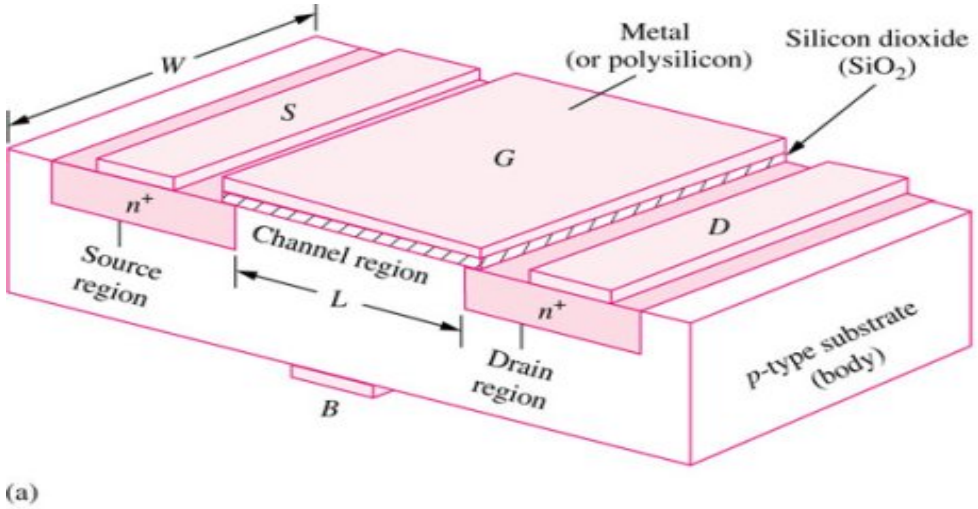
- Compared with BJT, MOSFET has
  - Higher integration scale
  - Lower manufacturing cost
  - Simpler circuitry for digital logic and memory
  - Inferior analog circuit performance in general

- Recent trend: more and more analog circuits are implemented in MOS technology for
  - lower cost
  - integration with digital circuits in a same chip (mixed-signal IC)

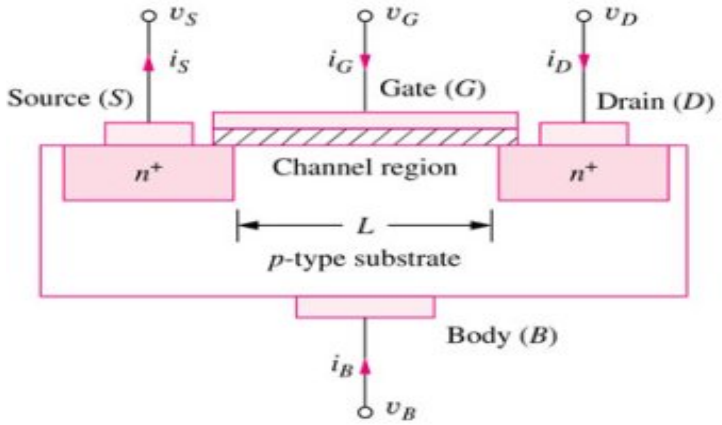


Microphotograph of
a state-of-the-art CPU chip

Structure of MOSFET



(a)



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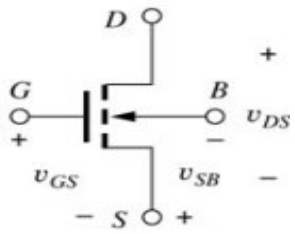
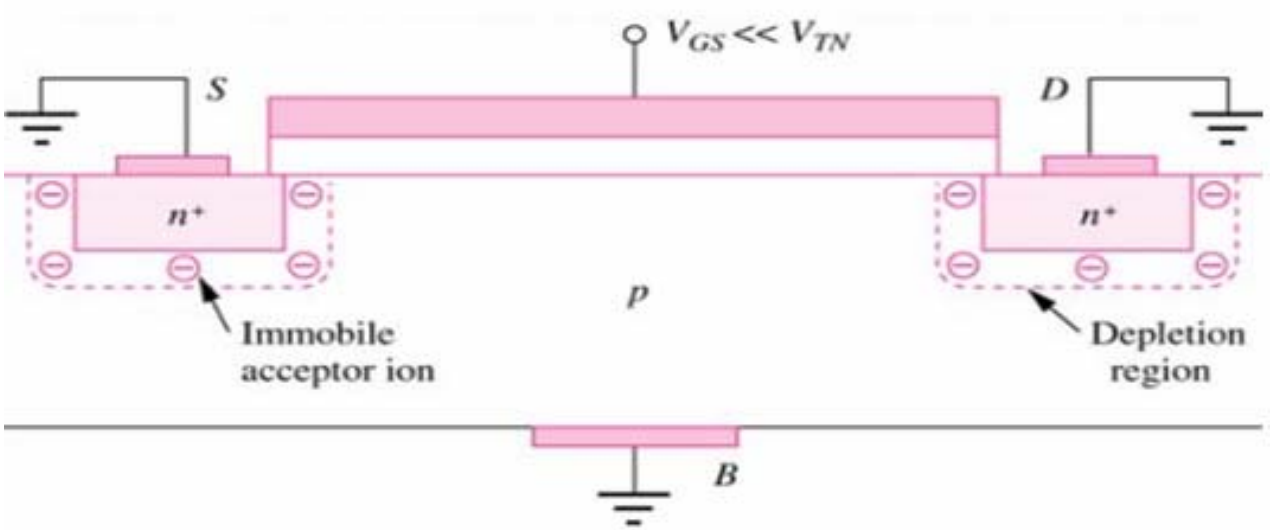


symbol

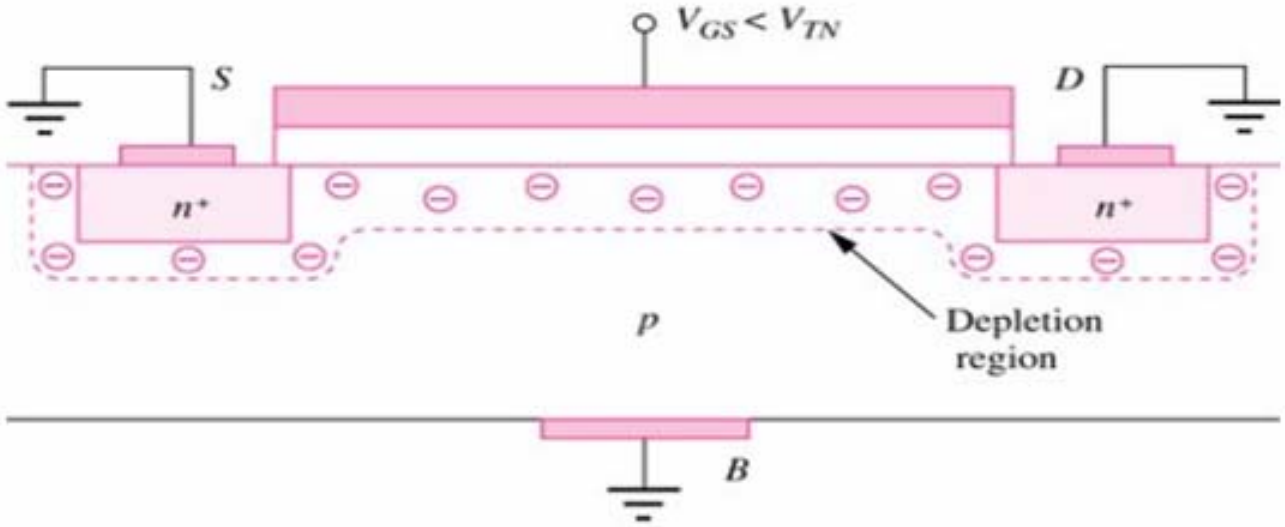
- Four terminals:
  - **Gate**, **Source**, **Drain** and **body**
- Two types
  - n-Channel (NMOS)
  - p-Channel (PMOS)
- The minimum value of L is referred as the **feature size** of the fabrication technology.
  - E.g., 45nm is used for Intel's Core 2 processors.

Low Gate Voltage



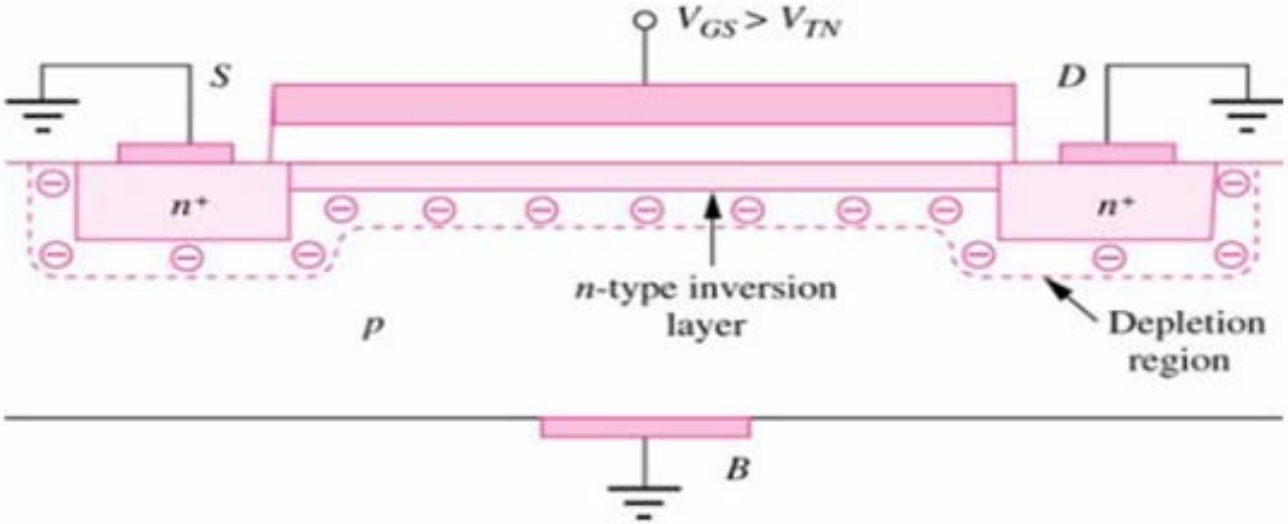
- Body is commonly tied to ground
- When the gate is at a low voltage (V_{GS} ~ 0):
  - P-type body is at low voltage
  - Source-body and drain-body diodes are OFF (reverse bias)
  - i_G=0 (always), i_{DS} = 0
- Depletion region between n+ and p-type bulk
  - No current can flow, transistor is said in "**Cutoff**" mode

Increase Gate Voltage



- Vertical electric field established
- Under the gate-oxide:
  - Holes (positive charges) repelled
  - Depletion region under gate oxide formed

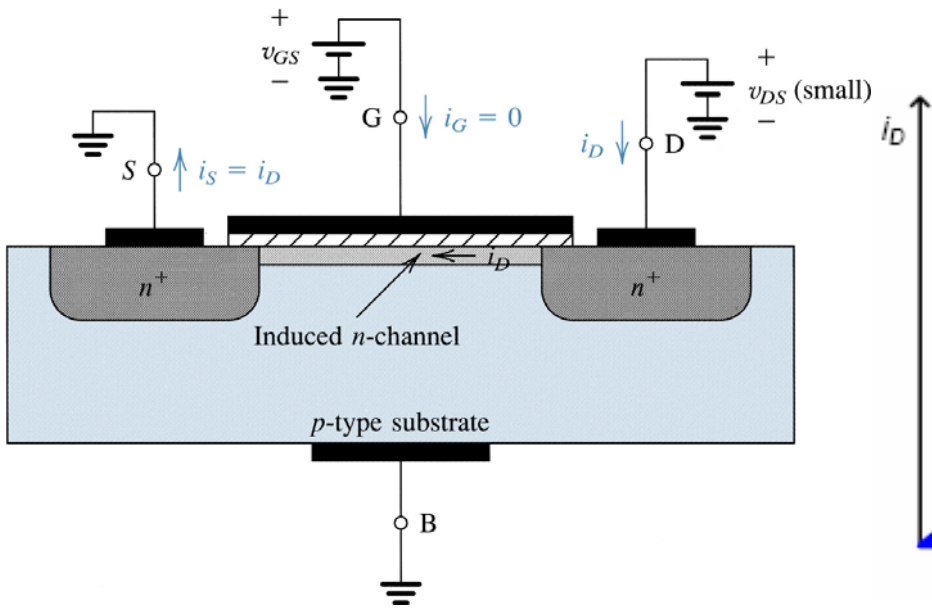
Further Increase Gate Voltage

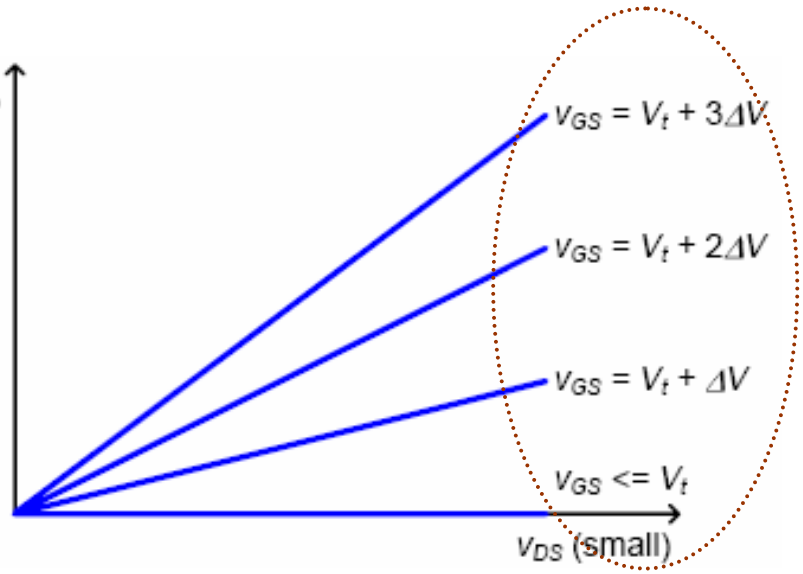


- Electrons (minorities in the *p* region) attracted by the electric field towards the gate, and stopped by the gate oxide
- A n-type inversion layer formed underneath the gate oxide when V_{GS} reaches a certain value, called **threshold voltage** (V_t, or V_{TN} for NMOS)
- The channel connects the S and D and now currents can flow between them

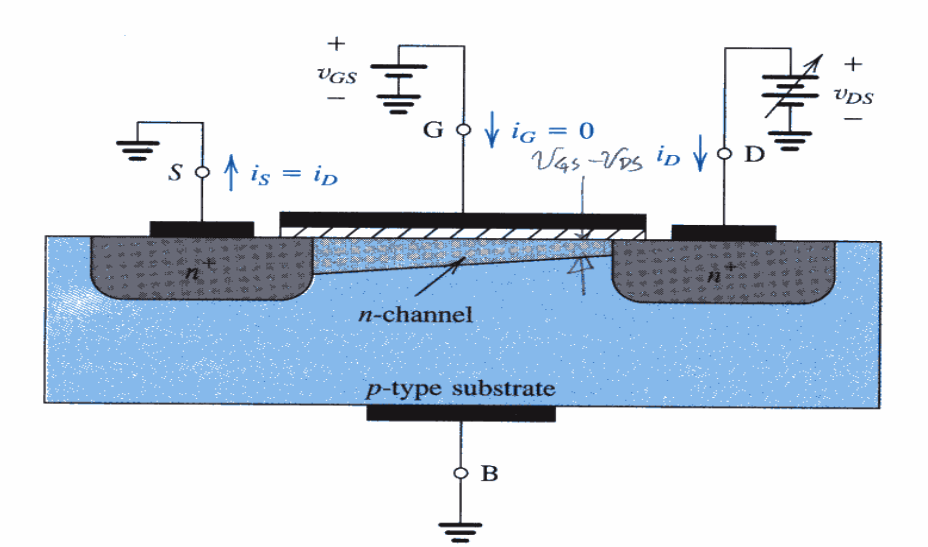
Linear (Triode) Mode of Operation

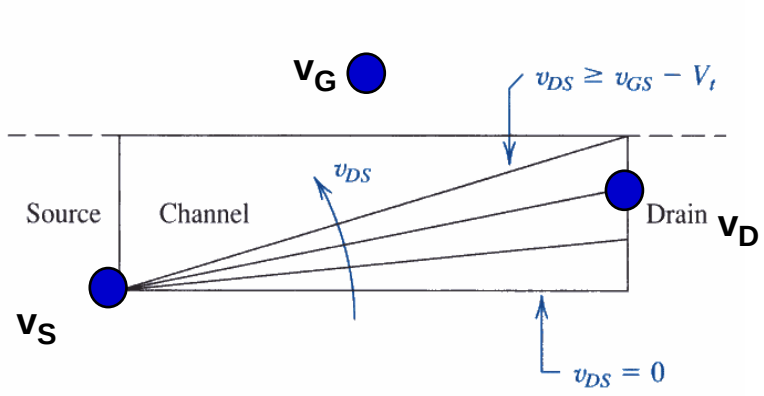
- When $v_{GS} > V_t$ and a small v_{DS} is applied
  - Current flows from D to S (Electrons flow from S to D)
  - $i_{DS} \propto v_{DS}$
- Increasing v_{GS} above V_t increases the electron density in the channel, and in turn increases the conductivity between D & S
- Such devices are called enhancement-type MOSFET
- In this mode, transistor = a voltage controlled resistor





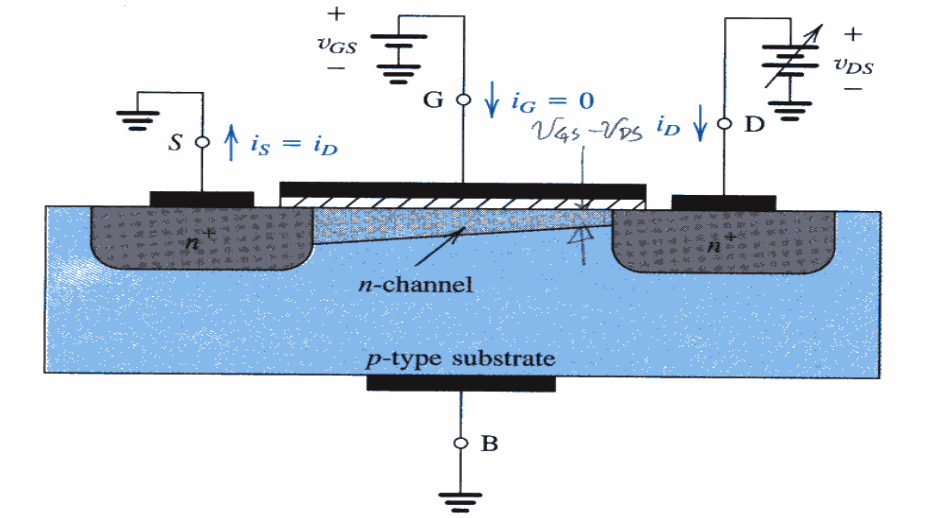
Increase Drain Voltage: Channel Pinch-Off

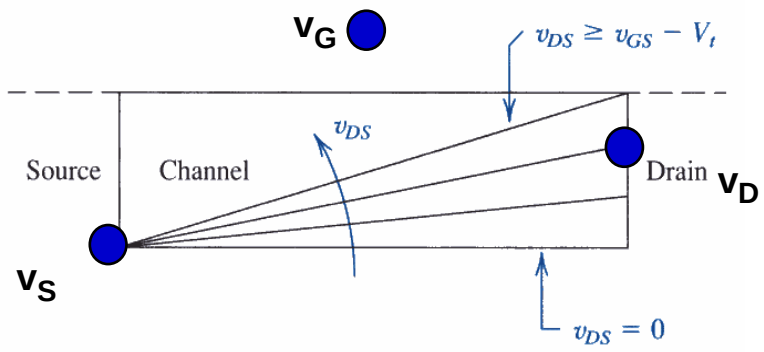




- Increase v_{DS} → Decrease v_{GD} → less electrons at the drain side of the channel
- When $v_{DS} \geq v_{GS} - V_t$
  → $V_{GD} \leq V_t$
  → no channel exists at the drain side. The channel "***pinches-off***"

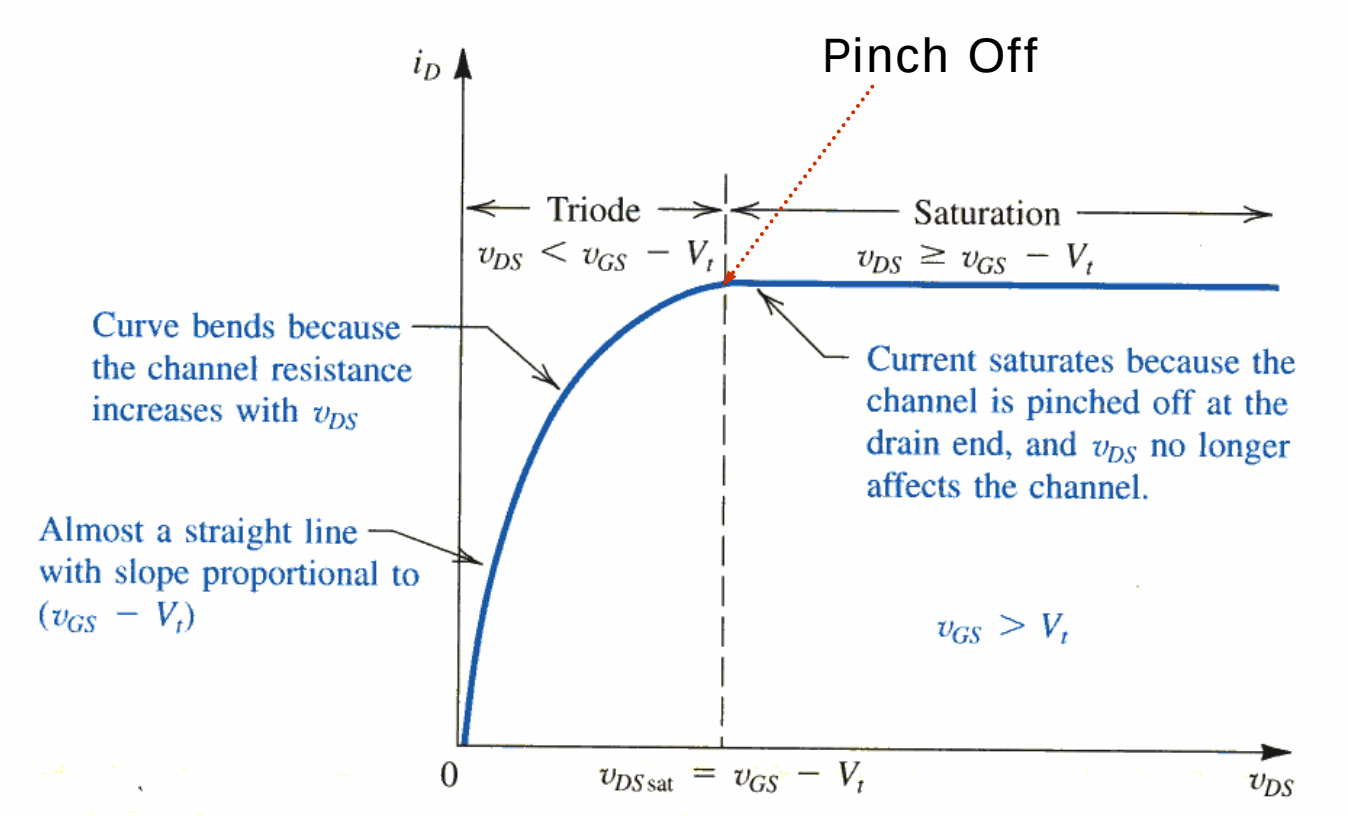
Saturation Mode of Operation





- When channel pinches off, electrons still flows from S to D
  - Electrons are diffused from the channel to the depletion region near D, where they are drifted by the lateral *E*-field to the D
  - Similar to a reverse-biased B-C junction in a BJT
- Further increase of v_{DS} → no effect on the channel → current is "saturated" and the transistor is in "***Saturation Mode***"
- In this mode, transistor = a voltage controlled current source

Qualitative I-V Characteristic



I-V Characteristics

- In the Linear region, drain current depends on
  - How much charge is in the channel
  - How fast the charge is moving

$$I \equiv \frac{dQ}{dt} = \frac{\text{amount of charge in the channel}}{\text{time it takes the carriers to get across the channel}}$$

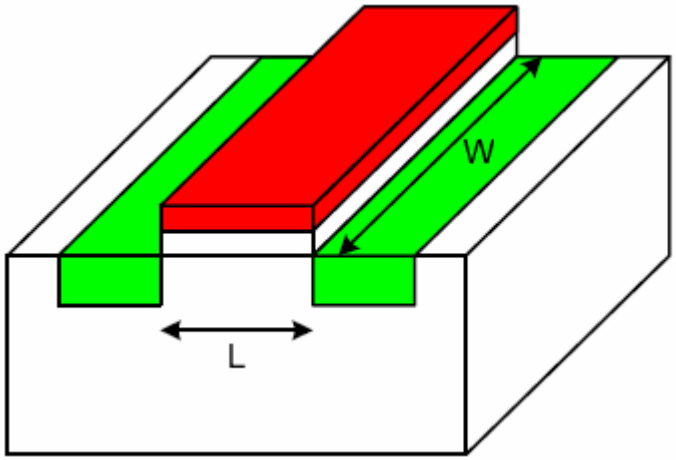
Amount of Channel Charge

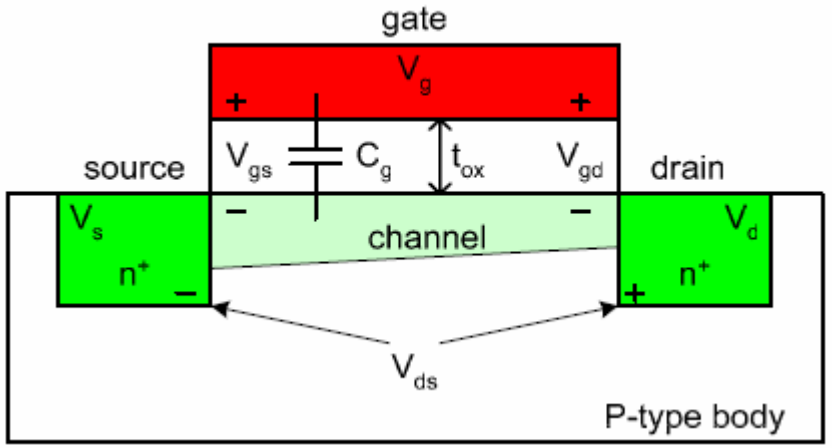
- MOS structure looks like a parallel plate capacitor
- V_{GC} is composed of two components
  - V_t to form the channel
  - $(V_{GC}-V_t)$ to accumulate negative charges in the channel

$$Q_{channel} = CV$$

$$C = \varepsilon_{ox}\frac{WL}{t_{ox}} = C_{ox}WL \quad \text{where } C_{ox} = \varepsilon_{ox}/t_{ox}$$

$$V = V_{GC} - V_t = \underbrace{\left(v_{GS} - v_{DS}/2\right)}_{\text{Average gate-channel voltage}} - V_t$$





Ref: G.-Y. Wei, notes ES154, Harvard University

Carrier Velocity

- Charge is carried by electrons.
- Carrier velocity v is proportional to the lateral E-field between source and drain

$$v = \mu_n E \quad \text{where } \mu_n \text{ is the mobility}$$

$$E = v_{DS} / L$$

- Time for carriers to cross the channel is

$$t = L / v = \frac{L}{\mu_n E} = \frac{L^2}{\mu_n v_{DS}}$$

I-V Behavior: Linear Mode

- Combine the channel charge and velocity to find the current flow
  - Current = amount of charge in the channel / time it takes the carriers to get across the channel

$$i_D = \frac{Q_{channel}}{t} = C_{ox} WL(v_{GS} - V_t - v_{DS}/2)\frac{\mu_n v_{DS}}{L^2}$$

$$= \mu_n C_{ox}\frac{W}{L}(v_{GS} - V_t - v_{DS}/2)v_{DS}$$

$$= K_n(v_{GS} - V_t - v_{DS}/2)v_{DS} \quad \text{where } K_n = \mu_n C_{ox}\frac{W}{L}$$

$$i_D = (\mu_n C_{ox})\frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

- $(\mu_n C_{ox})$ is a constant determined by the processing technology, and is denoted by K'_n
- W/L is a main design parameter in integrated circuit design.

I-V Behavior: Saturation Mode

- If $v_{GD} \leq V_t$, channel pinches off near the drain
  - When $v_{DS} \geq V_{dsat} = v_{GS} - V_t$
- Now, drain voltage no longer increases with v_{DS}
- Putting $v_{DS} = v_{GS} - V_t$ to the equation:

$$i_D = (\mu_n C_{ox}) \frac{W}{L} \left[(v_{GS} - V_t) v_{DS} - \frac{1}{2} v_{DS}^2 \right]$$

$$\Rightarrow \boxed{i_D = \frac{1}{2} (\mu_n C_{ox}) \frac{W}{L} (v_{GS} - V_t)^2}$$

for $V_{GS} > V_t$ and $V_{DS} \geq v_{GS} - V_t$

- i_D independent of v_{DS}.

Summary of NMOS I-V Characteristics

Region	Cutoff	Triode	Saturation
Conditions	$v_{GS} < V_t$	$v_{GS} \geq V_t$	
		$v_{DS} < v_{GS} - V_t$	$v_{DS} \geq v_{GS} - V_t$
I-V relation	$i_D = 0$	$i_D = K'_n \frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right]$	$i_D = \frac{1}{2}K'_n \frac{W}{L}(v_{GS} - V_t)^2$

- Cutoff region $v_{GS} < V_t$
- Triode region

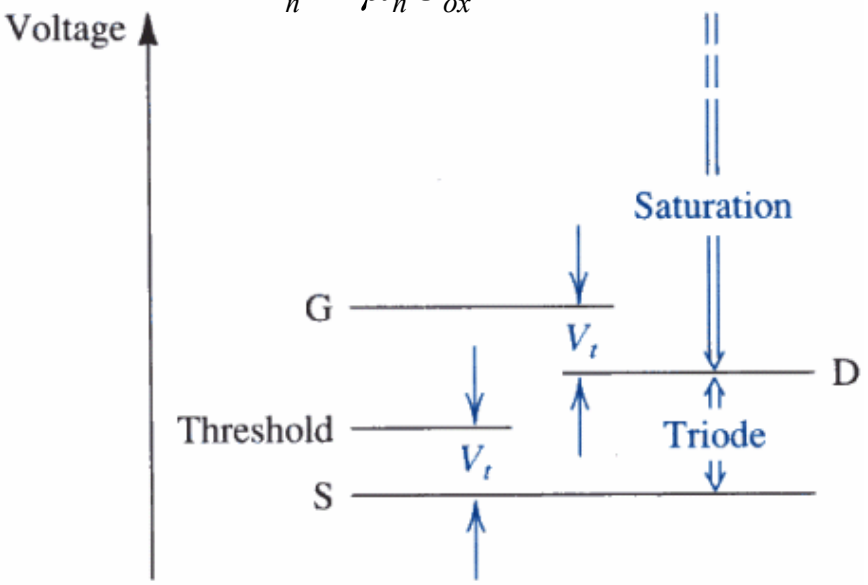
  $v_{GS} \geq V_t$ and

  $v_{DS} < v_{GS} - V_t$
- Saturation region

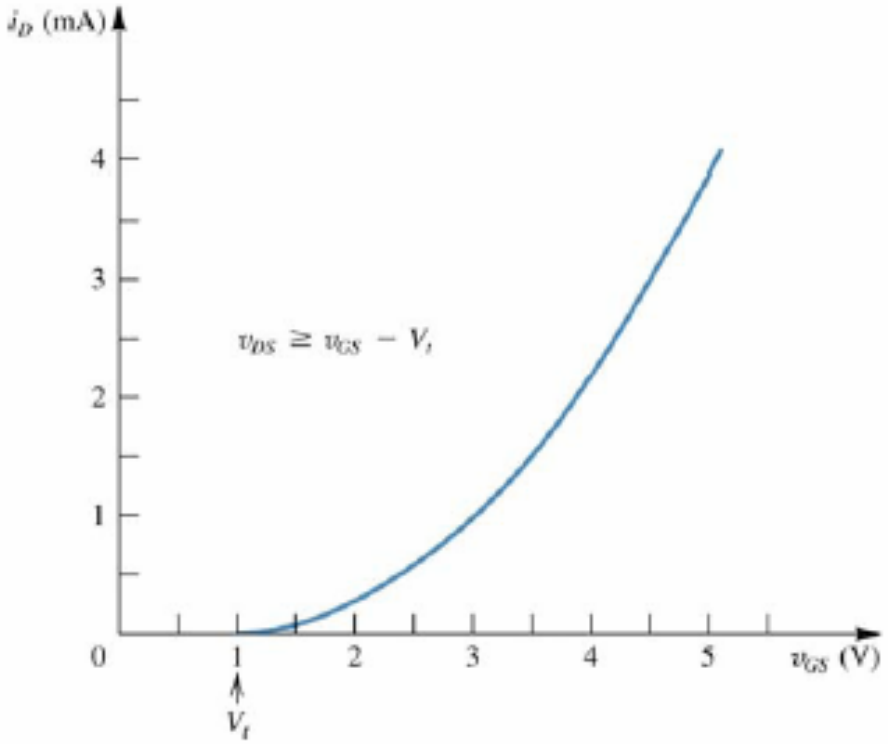
  $v_{GS} \geq V_t$ and

  $v_{DS} \geq v_{GS} - V_t$

$K_n' = \mu_n C_{ox}$



Ideal Square Law Model: I_D vs V_{GS}

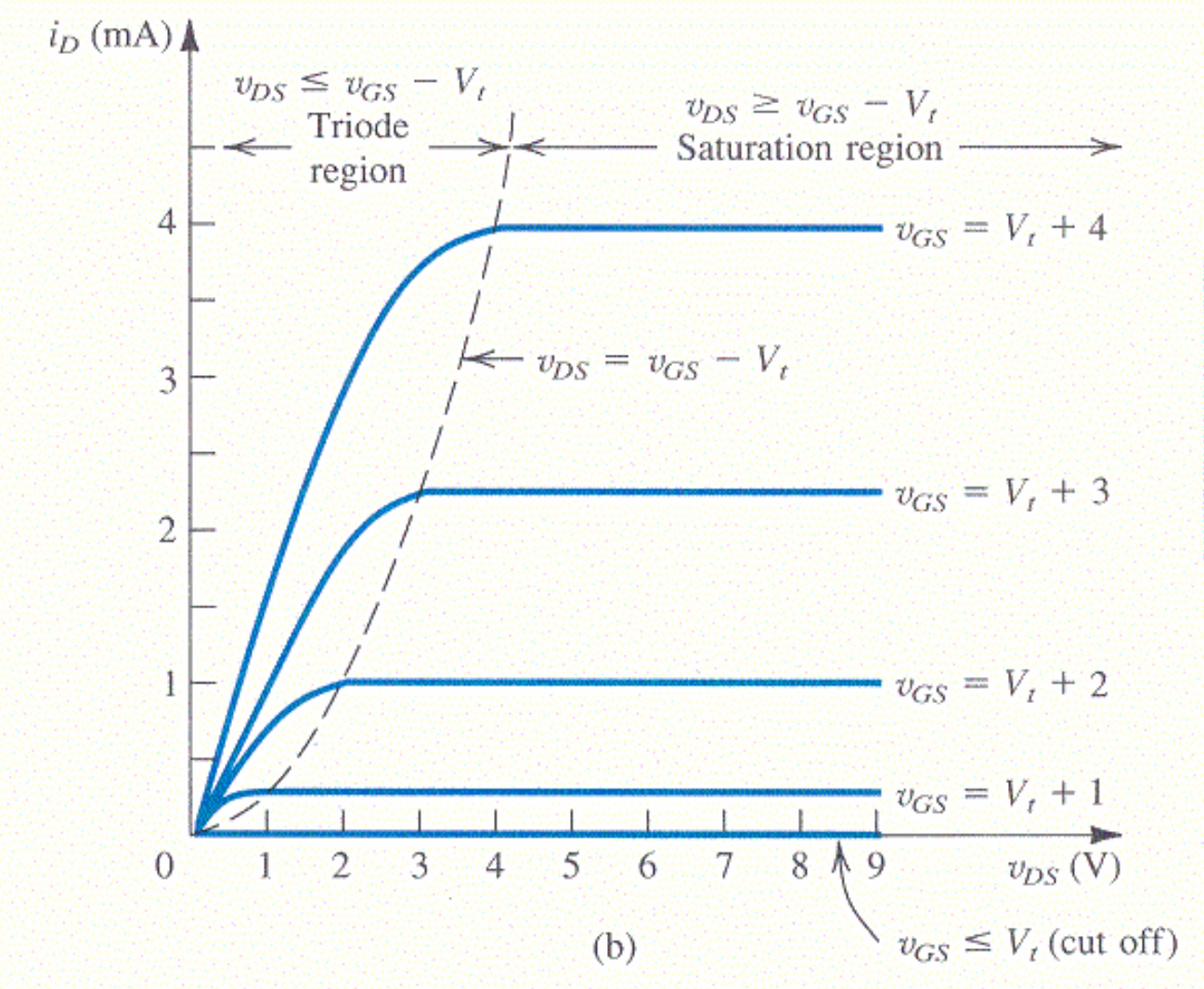


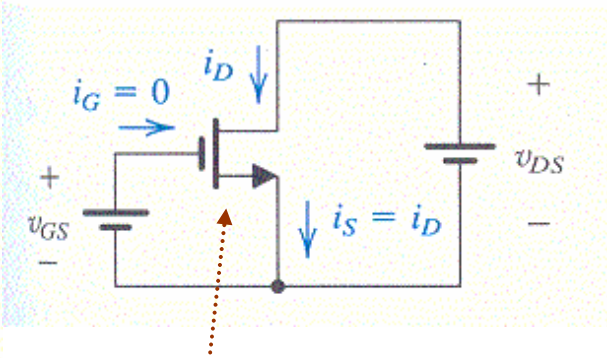
In saturation mode:

$$i_D = \frac{1}{2}(\mu_n C_{ox})\frac{W}{L}(v_{GS} - V_t)^2$$

- MOS vs. BJT
  - Current is quadratic with voltage in MOS vs.
  - exponential relationship in BJT
- Saturation mode of MOS corresponds to active mode of BJT

Ideal Square-Law Model: I_D vs V_{DS}





NMOS

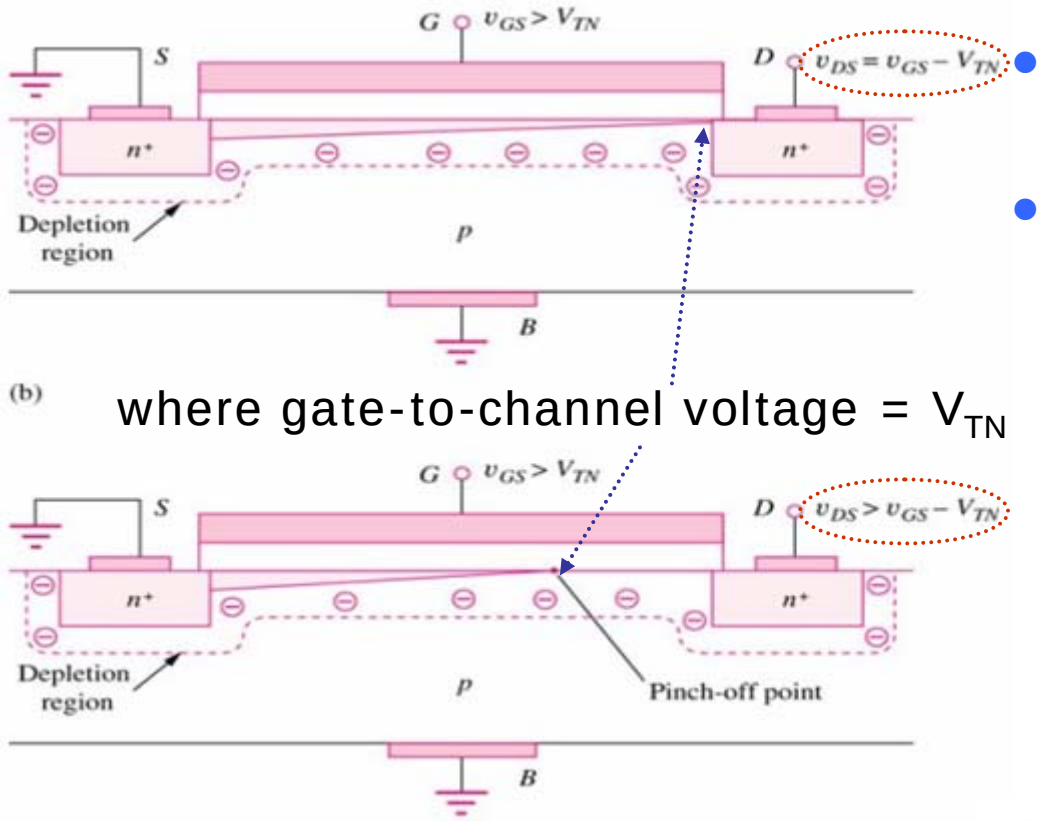
Topics to cover …

- Common-Collector Amplifier
- MOS Field Effect Transistor
  - Physical Operation and I-V Characteristics of n-channel devices
  - Non-ideal effects
  - P-channel devices and other types

Non-ideal Effects

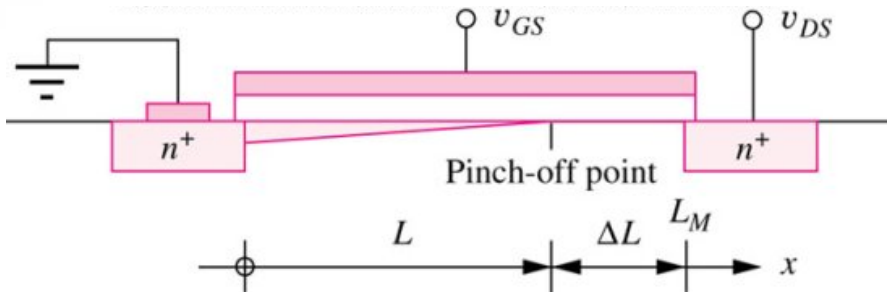
- Channel length modulation
- Body effect
- Temperature influence
- Breakdown

Channel-Length Modulation

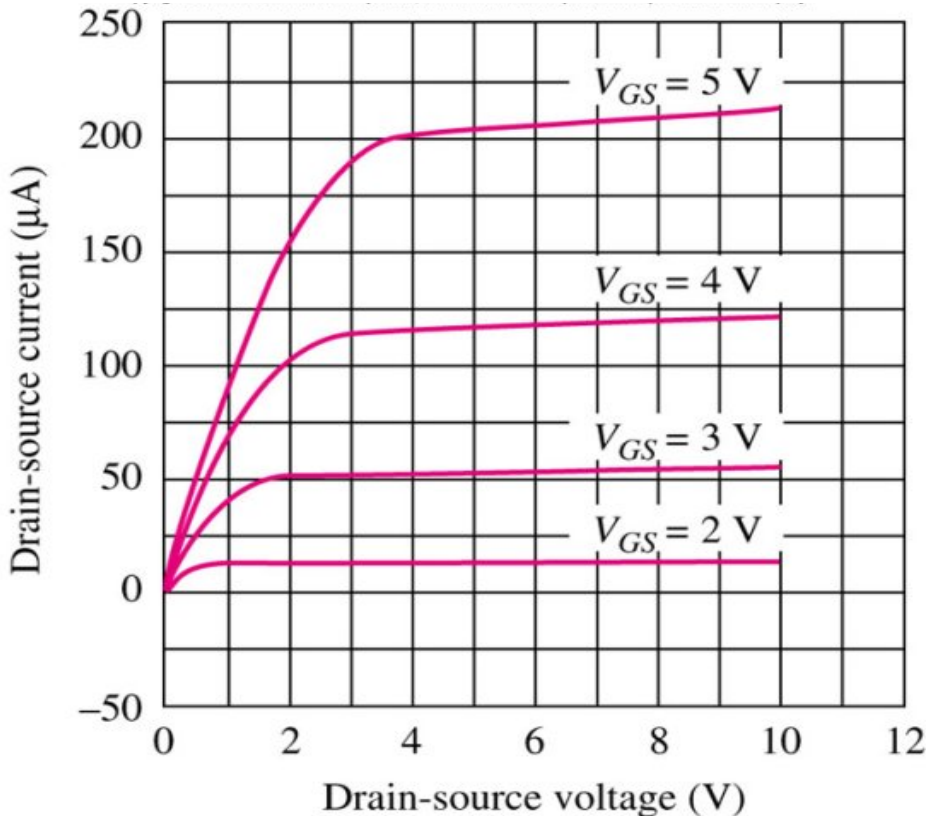


- At $v_{DS}=v_{GS}-V_{TN}=V_{DSsat}$,
  - Channel pinch-off
- As v_{DS} increases beyond v_{DSsat}, the pinch off point moves away from D towards S
  - The effective channel length L is reduced by ΔL
  - I_D increases
  - An effect similar to Early effect in BJT

$$i_D = \frac{K_n'}{2}\frac{W}{L}\left(v_{GS}-V_{TN}\right)^2$$



Channel-Length Modulation

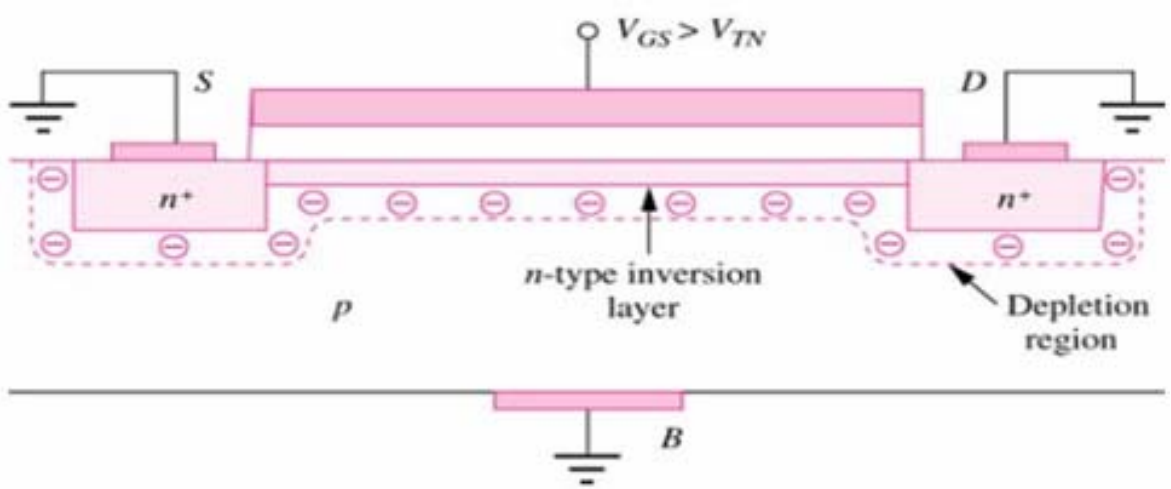


- This effect is modeled by adding a term $(1+\lambda v_{DS})$ to the I-V equation:

$$i_D = \frac{K_n'}{2}\frac{W}{L}\left(v_{GS}-V_{TN}\right)^2\left(1+\lambda v_{DS}\right)$$

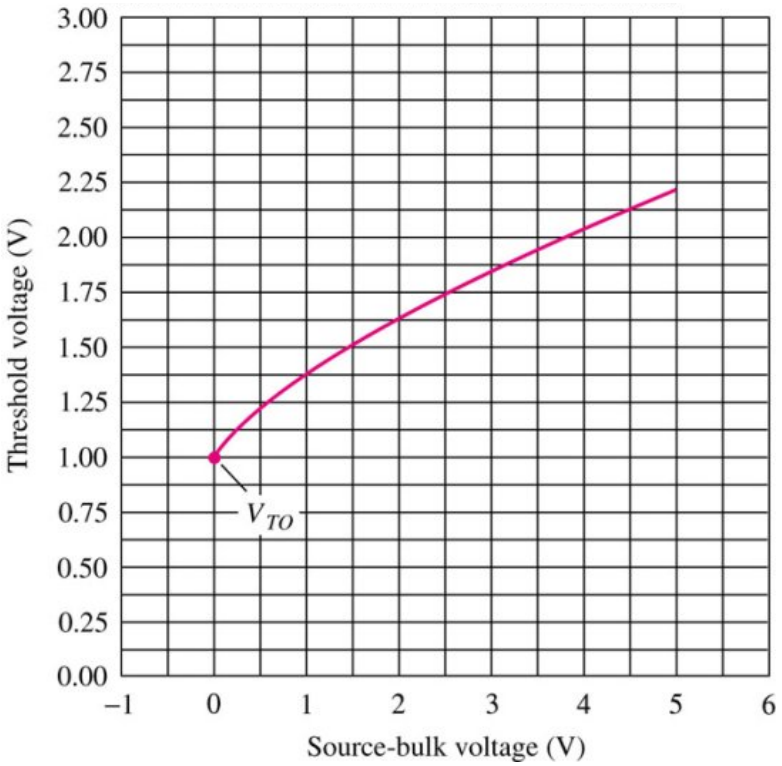
λ = channel length modulation parameter

Body Effect



- Channel-body can be regarded as a *pn* junction
- If channel-body junction is reverse-biased,
  - Depletion layer beneath the gate oxide becomes wider
  - Since the amount of negative charges in the (channel + depletion) layer = amount of positive charges in the gate (Constant for a fixed gate-source voltage)
    → Channel depth is reduced
  - This is equivalent to an increase in the threshold voltage

Body Effect



(source-body voltage)

- Non-zero v_{SB} changes threshold voltage:

$$V_{TN} = V_{TO} + \gamma\left(\sqrt{v_{SB} + 2\phi_F} - \sqrt{2\phi_F}\right)$$

where

V_{TO}= zero substrate bias for V_{TN} (V)

γ= body-effect parameter $(\sqrt{V})$

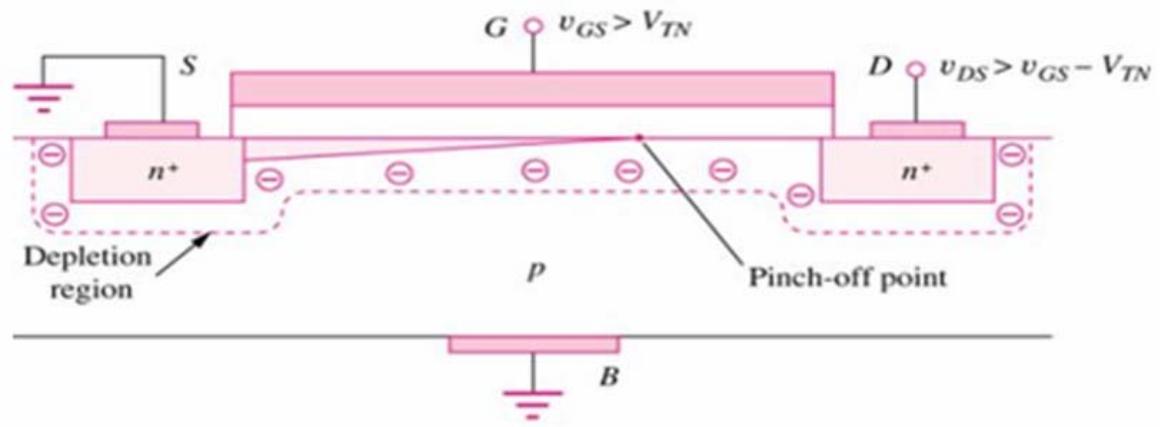
$2\Phi_F$= surface potential parameter (V)

It follows that the body voltage controls i_D.
This phenomenon is known as the **body effect**.

Effects of Temperature

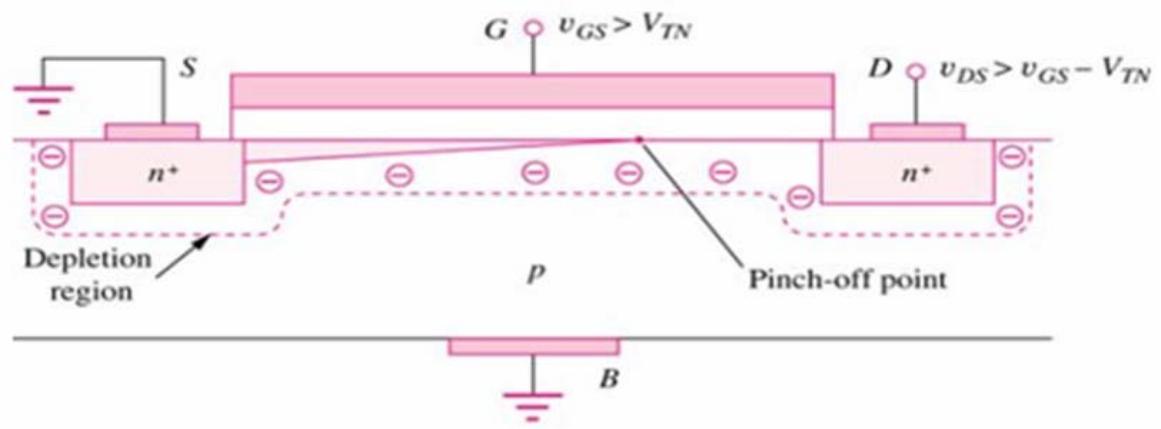
- V_t and mobility μ are sensitive to temperature:
  - V_t decreases by 2mV for every 1ºC rise in temperature
  - mobility μ decreases with temperature
- Overall, increase in temperature results in lower drain currents

Avalanche Breakdown



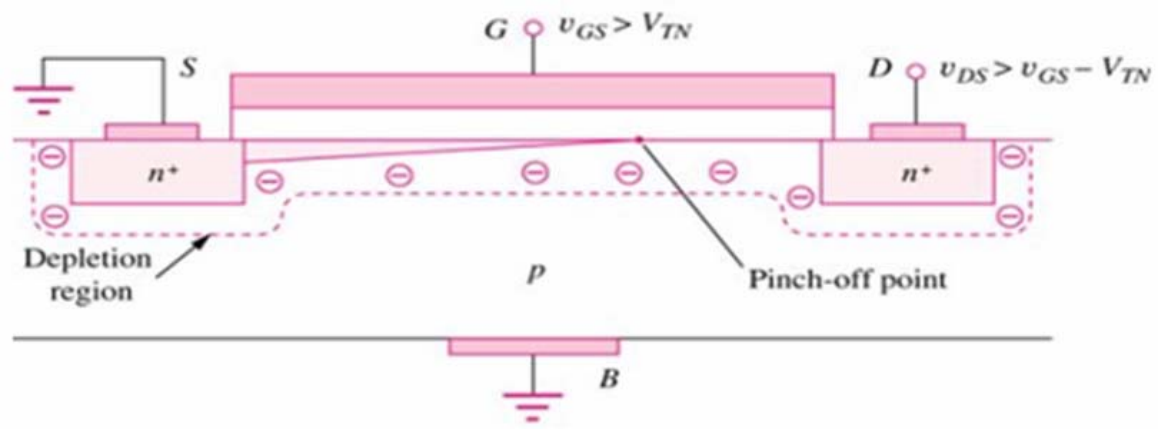
- As V_D is increased, the drain-body junction becomes reversed biased
  → Breakdown occurs at voltages of 20 to 150V
  → Rapid increase in the drain current
- Normally, no permanent damage to the device

Punch-through Breakdown



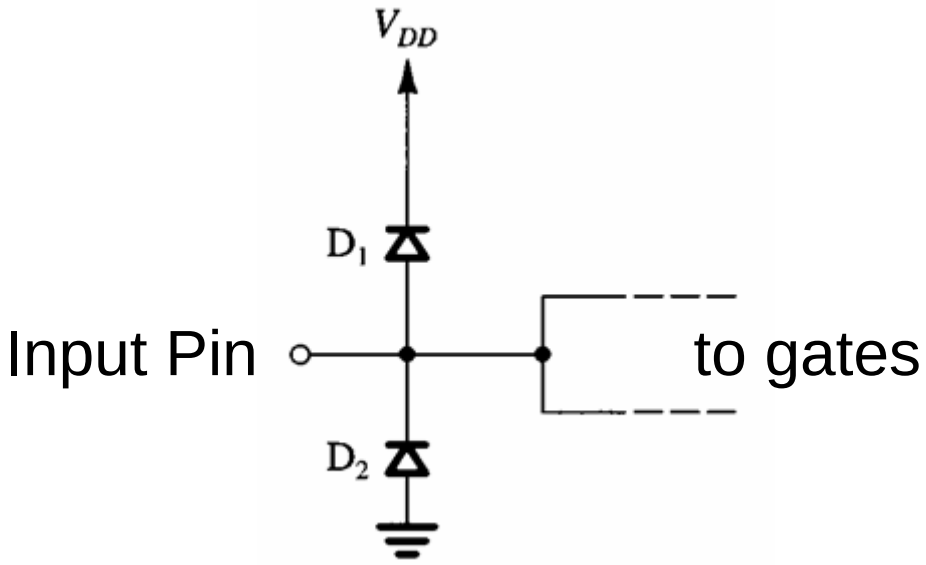
- Whe V_D is increased to a point, → the depletion region surrounding D extends to the S → Punch-through breakdown (about 20 V)
- Occurs in devices with short channels
- Normally, no permanent damage to the device

Gate Oxide Breakdown



- When V_{GS} exceeds about 30 V (or lower in modern IC technology)
  → Gate oxide breaks down like in the case of a capacitor
- Results in permanent damage to the device

Input Protection



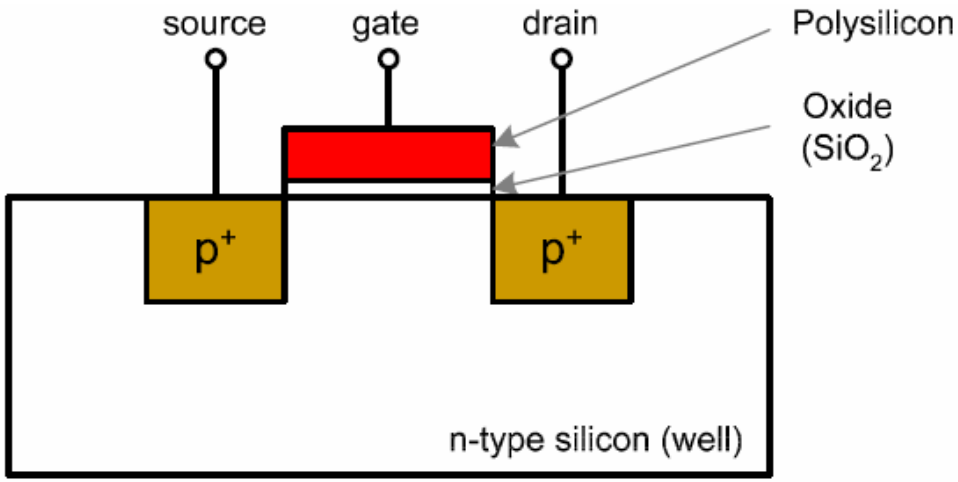
- Since the MOSFET has a very small input capacitance and a very high input resistance, a small amount of static charges accumulating on the gate can cause the gate voltage to exceed the breakdown level
  - e.g., Electrostatic Discharge (ESD) from human body
- Clamping diodes can be used in the I/O pins to protect the circuit from gate-oxide breakdown

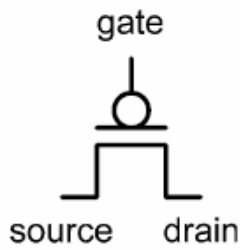
Topics to cover …

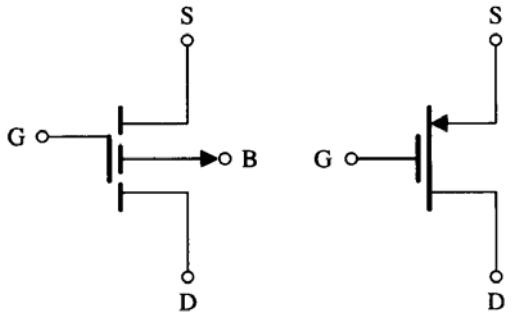
- Common-Collector Amplifier
- MOS Field Effect Transistor
  - Physical Operation and I-V Characteristics of n-channel devices
  - Non-ideal effects
  - P-channel devices and other types

P-channel MOSFET (PMOS)

- Similar to NMOS, but doping and voltages reversed
  - Body tied to highest voltage (Vdd) to prevent forward-biasing pn junctions
  - Source typically tied to Vdd too
  - Gate voltage high: transistor is OFF
  - Gate voltage low: transistor is ON when $V_{GS} < V_t$ (threshold voltage)
    - Inverted channel of positively charged holes
  - v_{GS} and v_{DS} are negative and V_t is also negative

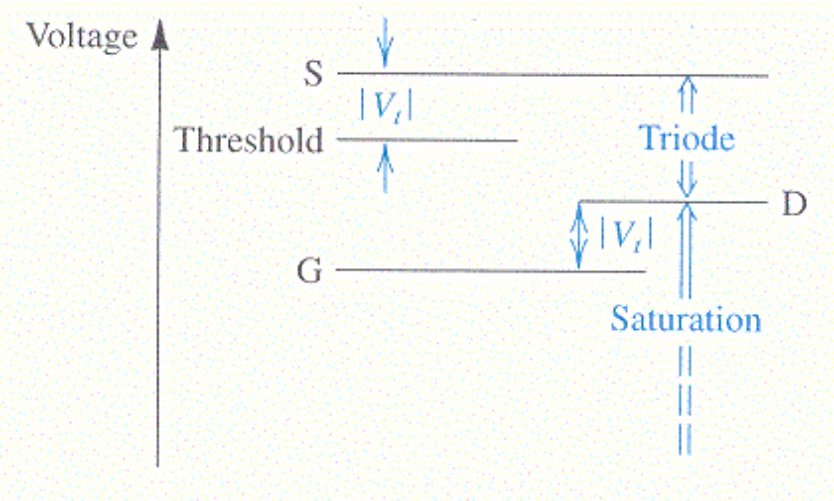






Symbols

PMOS I-V Characteristics



V_t, v_{GS} and v_{DS} are negative.

- Cutoff region $|v_{GS}| < |V_t|$
- Triode region

  $|v_{GS}| \geq |V_t|$ and

  $|v_{DS}| < |v_{GS} - V_t|$
- Saturation region

  $|v_{GS}| \geq |V_t|$ and

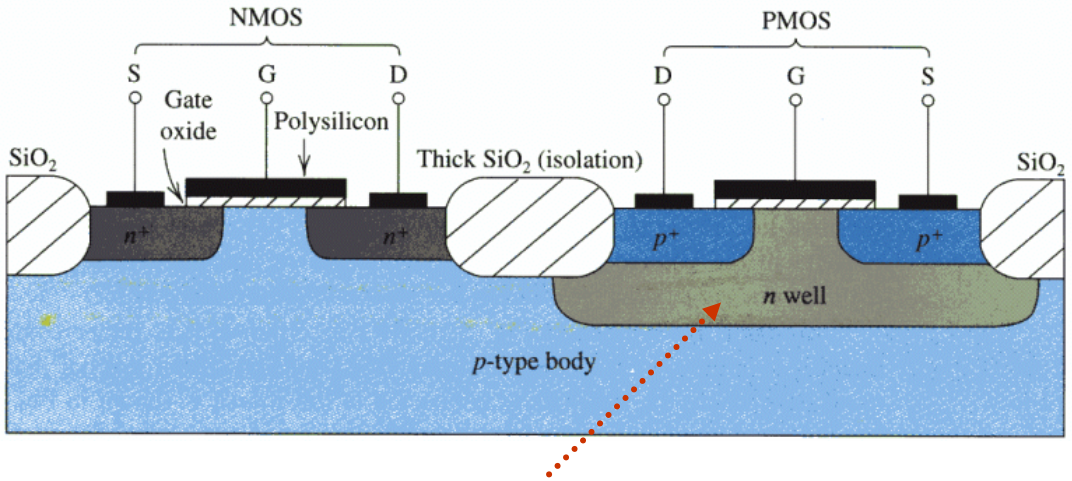
  $|v_{DS}| \geq |v_{GS} - V_t|$

Cutoff	Triode/Linear	Saturation
$i_D = 0$	$i_D = K_p\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right]$	$i_D = \frac{1}{2}K_p(v_{GS} - V_t)^2$

where $K_p = K_p'\frac{W}{L}$, $K_p' = \mu_p C_{ox}$

μ_p is 2 or 3-times lower than μ_n

Complementary MOS (CMOS) Technology

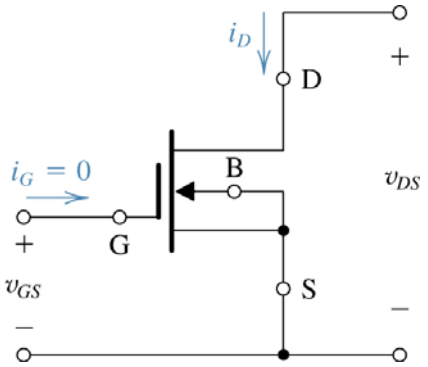


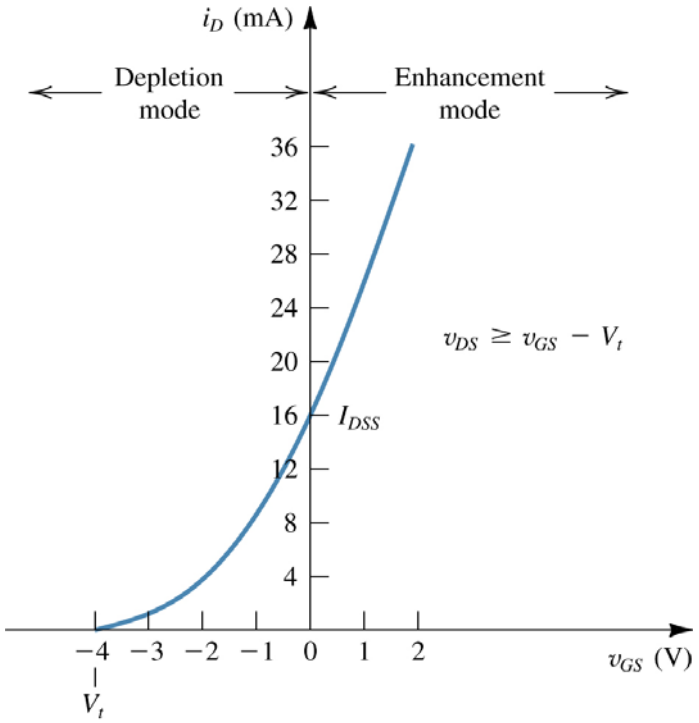
PMOS transistor is fabricated in the ***n* well**

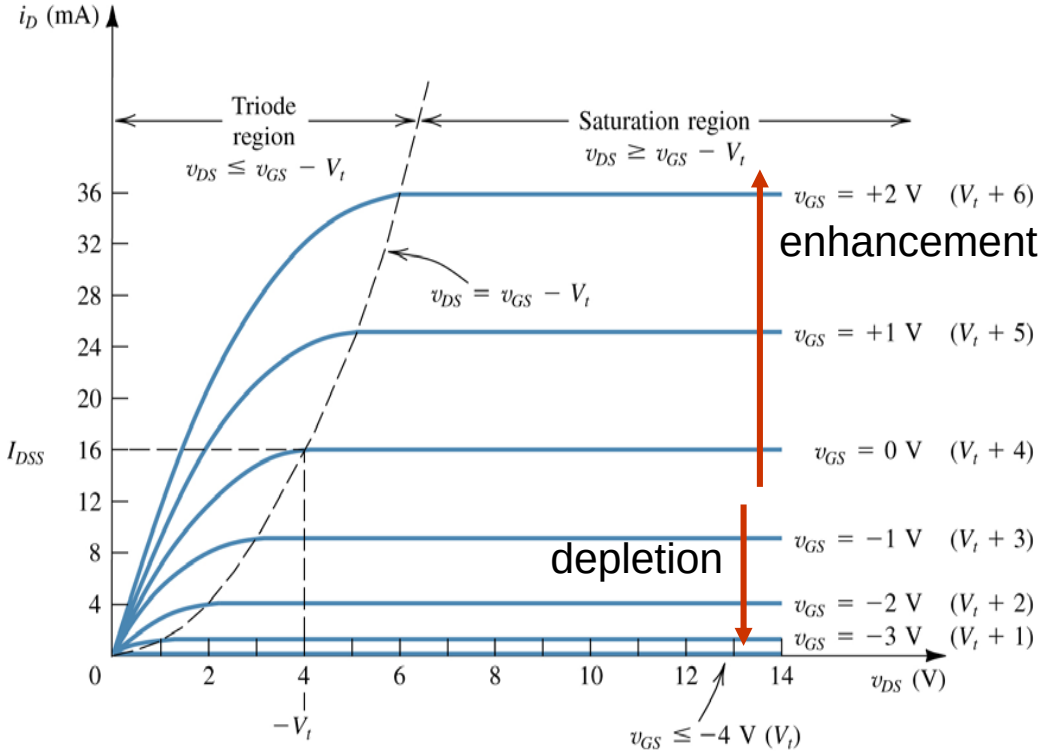
Complementary MOS or CMOS integrated-circuit technologies provide both NMOS and PMOS on a same IC

Depletion-mode MOSFET

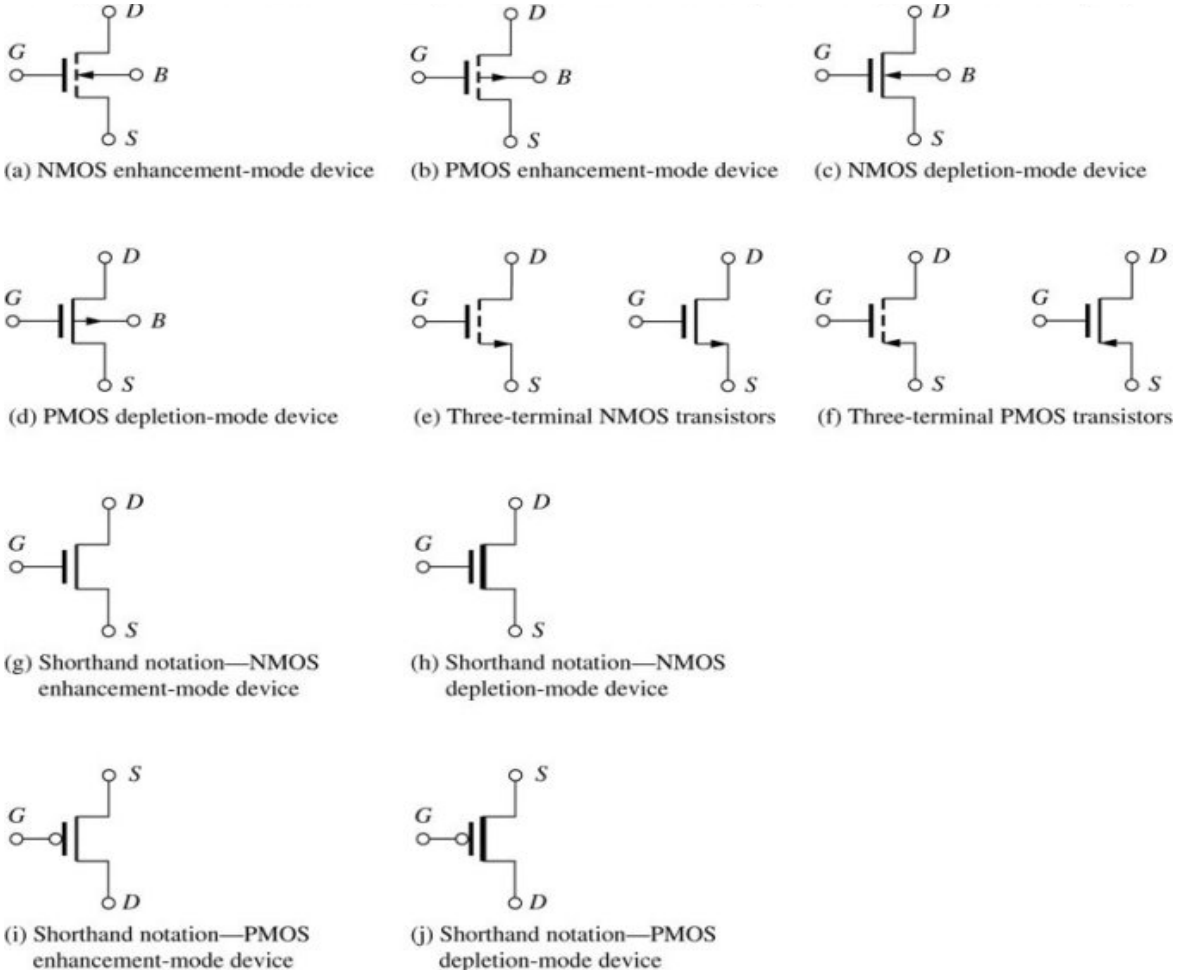
- A depletion-type MOSFET has a built-in channel by fabrication
  - It is ON when no gate-source voltage is applied
  - Must apply a negative v_{GS} to turn off device
- V_t is negative for NMOS







MOSFET Circuit Symbols



(a) NMOS enhancement-mode device
(b) PMOS enhancement-mode device
(c) NMOS depletion-mode device
(d) PMOS depletion-mode device
(e) Three-terminal NMOS transistors
(f) Three-terminal PMOS transistors
(g) Shorthand notation—NMOS enhancement-mode device
(h) Shorthand notation—NMOS depletion-mode device
(i) Shorthand notation—PMOS enhancement-mode device
(j) Shorthand notation—PMOS depletion-mode device

- (g) and(i) are the most commonly used symbols in VLSI logic design.
- MOS devices are symmetric.
- In NMOS, n^+ region at higher voltage is the drain.
- In PMOS p^+ region at lower voltage is the drain