Chapter 28

Basic Transistor Theory

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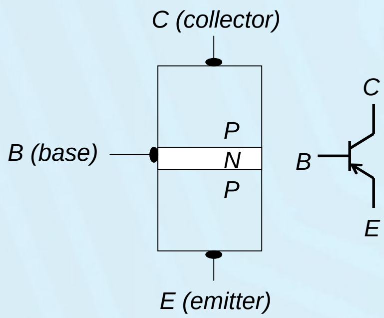
Transistor Construction

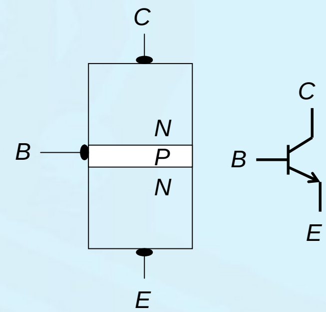
- Bipolar Junction Transistor (BJT)
  - 3 layers of doped semiconductor
  - 2 *p-n* junctions
  - Layers are: Emitter, Base, and Collector
  - Can be *NPN or PNP*
  - Emitter and Collector both *P* or both *N* type

Transistor Construction

- Structure and Electronic Symbol



***PNP* Transistor**



***NPN* Transistor**

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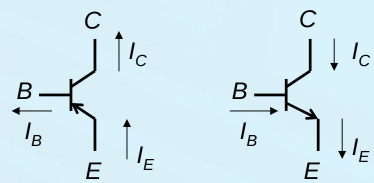
Transistor Operation

- Amplifier
  - *B-E* junction forward biased
    - $V_{BE} \approx 0.7$ V for Si
  - *C-B* junction reverse biased
  - *KCL:* $I_E = I_C + I_B$



Transistor Operation

- Transistor Bias Circuits

Transistor Operation

- dc Beta (β_{dc})
  - $I_E = I_C + I_B$
  - $I_B << I_E$
  - $I_C \approx I_E$
  - $40 < \beta_{dc} < 400$

$$\beta_{dc} = \frac{\Delta I_C}{\Delta I_B}$$

Transistor Operation

- 2N3904 NPN transistor spec
  - $100 < \beta_{dc} < 300$
- β_{dc} dependent on
  - Operating point
  - Temperature

Transistor Operation

- dc Alpha (α_{dc})
  - $\alpha < 1$
- α - β Relationship

$$\alpha_{dc} = \frac{I_C}{I_E}$$

$$\alpha = \frac{\beta}{\beta + 1}$$

$$\beta = \frac{\alpha}{1 - \alpha}$$

Transistor Specifications

- Maximum voltage between *C & E* with Base open, V_{CEO}
- Maximum reverse voltage between *C & B* with Emitter open, V_{CBO}
- Maximum reverse voltage between E & B with Collector open, V_{EBO}

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Transistor Specifications

- Maximum collector current, I_C
- Maximum power dissipated, P_D

$$P_D = I_C * V_{CE}$$

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Transistor Specifications

- Minimum *C-E* voltage for breakdown, $V_{(BR)CEO}$
- Carefully examine absolute max ratings
- dc current gain
  - variable
  - $\beta = h_{FE}$ in specs

Collector Characteristic Curves

- Saturation region
  - I_C increases rapidly for small values of V_{CE}
  - *BJT* behaves like closed switch

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Collector Characteristic Curves

- Active region
  - *BJT* acts as a signal amplifier
  - B-E junction is forward biased & C-B junction is reverse biased

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Collector Characteristic Curves

- β_{dc} not constant
- β_{dc} dependent on dc operating point
- Quiescent point = operating point
- Active region limited by
  - Maximum forward current, $I_{C(MAX)}$
  - Maximum power dissipation, P_D

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dc Load Line

- Drawn on characteristic curves
- Component values in a bias circuit
  - Determine quiescent point, *Q*
  - *Q* is between saturation and cutoff
- Best *Q* for a linear amplifier
  - Midway between saturation and cutoff

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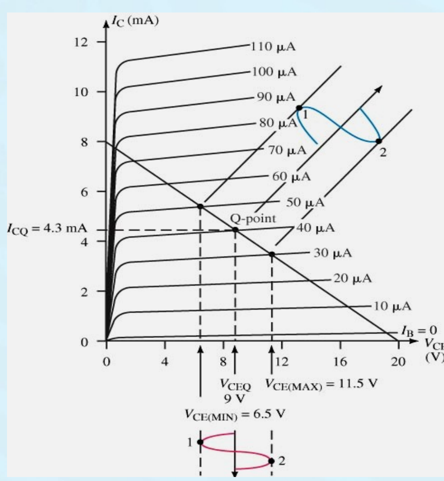
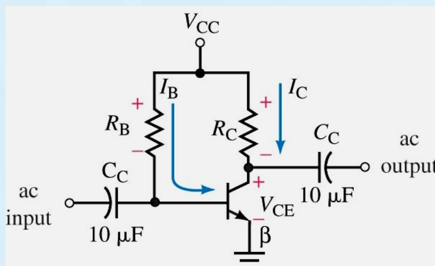
DC Load Line

- Characteristic curve with Load Line
- *Q*-point, and current gain



Transistor Biasing

- Fixed-Bias Circuit
  - Single power supply
  - Coupling capacitors



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Transistor Biasing

- Equations for Fixed-Bias circuit

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_C = \beta I_B$$

$$V_{CE} = V_{CC} - I_C R_C$$

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Transistor Biasing

- Fixed Bias Circuit highly dependent on β_{dc}
- Emitter-Stabilized Bias Circuit
  - Add emitter resistor
  - Greatly reduces effect of change of β
  - Equations

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Transistor Biasing

$$V_{CC} = R_B I_B + V_{BE} + R_E I_E$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + R_E(\beta + 1)}$$

$$V_{CE} = V_{CC} - (R_C + R_E) I_C$$

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Transistor Biasing

- Universal-Bias circuit
  - Sometimes referred to as voltage divider bias
  - Most stable
  - Equations:

$$I_B = \frac{V_{BB} - V_{BE}}{R_{BB} + R_E(\beta + 1)}$$

$$I_C = \beta I_B$$

$$V_{CE} = V_{CC} - (R_C + R_E) I_C$$

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Transistor Biasing

- Universal-Bias circuit
  - Need $I_B << I_C$
  - Make $R_2 \leq \frac{1}{10}\beta R_E$
  - Simple Voltage divider between V_{CC}, Base, and ground

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Transistor Biasing

$$I_E = \frac{V_E}{R_E} \equiv I_C$$

$$V_{CE} \cong V_{CC} - (R_C + R_E) I_C$$

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Transistor Biasing

- Common Collector Circuit
  - Less common than CE circuit
  - Collector connected to ground
  - Similar analysis
  - Voltage gain < 1

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Transistor Biasing

- Common Base Circuit
  - Least common
  - High frequency applications
  - Current gain < 1

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The Transistor Switch

- *BJT* less used as amplifiers
  - IC amplifiers available
- Switching is a principal application of *BJT's*
  - Current amplifier turn on LED's
  - Power amplifier to turn on small motors

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The Transistor Switch

- A buffer has high input impedance and low output impedance

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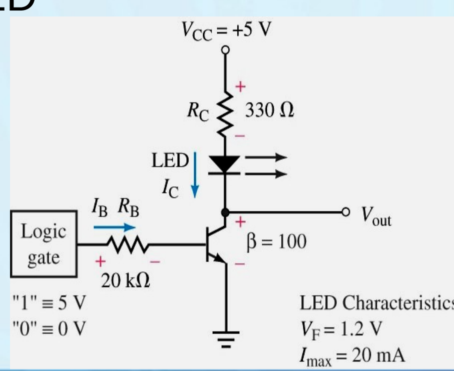
The Transistor Switch

- *BJT* as a buffer between digital input and LED



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Testing a Transistor with a Multimeter

- Ohmmeter
  - dc voltage generates small current
- Test *CB* and *BE* junctions
  - Forward bias = small resistance
  - Reverse bias = large resistance

Testing a Transistor with a Multimeter

- Fail test
  - *BJT* will not operate correctly
- Pass test
  - Not a guarantee that *BJT* is good

Testing a Transistor with a Multimeter

- Six measurements required
- An O.C. between two terminals (both directions) means other terminal is *B*
- Only two low Ω readings if *BJT* is good

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Testing a Transistor with a Multimeter

- Lower of the two low *Ω* readings is *C*
- Other one of low *Ω* readings is *E*

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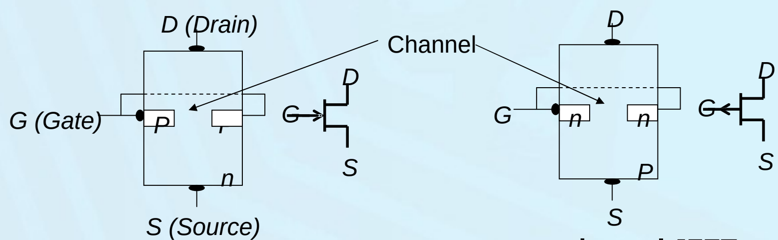
Junction Field Effect Transistor Construction and Operation

- Construction and symbols



***n*-channel JFET**

***p*-channel JFET**

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Junction Field Effect Transistor Construction and Operation

- *BJT*
  - Current amplification
  - *BE* junction forward biased
  - Input impedance (Common Emitter) low

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Junction Field Effect Transistor Construction and Operation

- *JFET*
  - Voltage amplification
  - *GS* junction reverse biased
  - Input impedance very high

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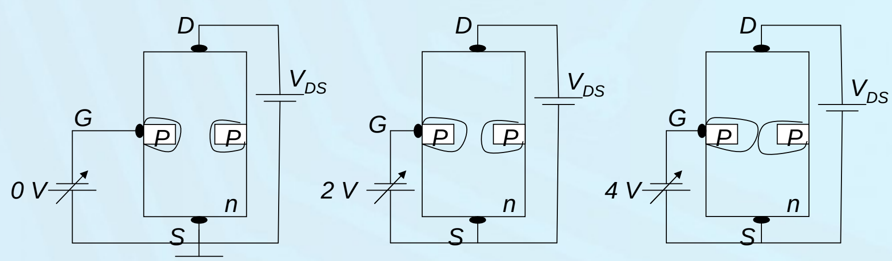
Junction Field Effect Transistor Construction and Operation

- Basic operation of an n-channel *JFET*



Junction Field Effect Transistor Construction and Operation

- $I_S = I_D$
- Decrease V_{GS} from 0 to –4
  - Decrease current flowing
  - Pinchoff voltage reached

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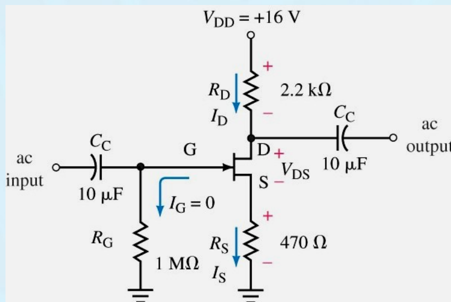
Junction Field Effect Transistor Construction and Operation

- I_D vs V_{GS} (Transconductance curve) described by Shockley's equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(OFF)}}\right)^2$$

Junction Field Effect Transistor Construction and Operation

- Self-bias circuit



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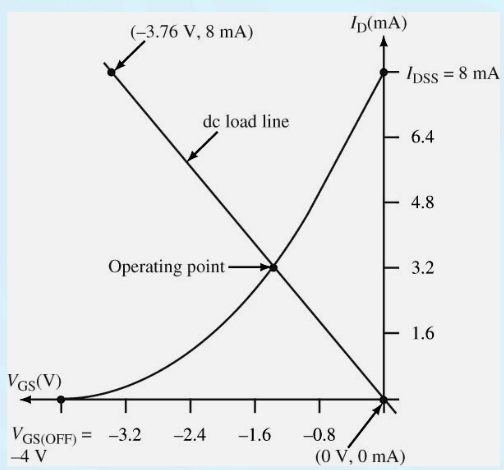
Junction Field Effect Transistor Construction and Operation

- Load line



Junction Field Effect Transistor Construction and Operation

- Another biasing circuit: similar to universal bias circuit for *BJT's*
  - Voltage divider
  - Resistor from from V_{DD} to the Gate
  - Resistor from Gate to ground

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Junction Field Effect Transistor Construction and Operation

- Basic JFET circuit analysis: use
  - KVL and KCL
  - $I_G = 0$
  - $I_D = I_S$

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MOSFETs

- Metal Oxide Semiconductor Field Effect Transistors
  - Small
  - Low power
  - Higher current capability, I_{DS}
  - Do not have to reverse bias the gate
  - Depletion or Enhancement types

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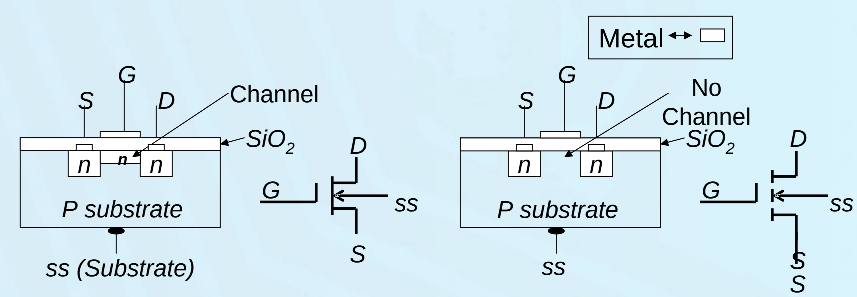
MOSFETs

- Construction and symbols



***n*-channel depletion MOSFET** **_n_-channel enhancement MOSFET**

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MOSFETs

- Depletion MOSFETs
  - Have a channel
  - Shockley's equation still valid
  - Depletion mode
  - Enhancement mode

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MOSFETs

- Enhancement MOSFETs
  - No channel
  - Positive V_{GS} required prior to current
  - Enhancement mode only
  - No depletion mode
  - Shockley's equation no longer valid

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MOSFETs

- Biasing
  - Voltage Divider
  - Drain-feedback circuit shown here

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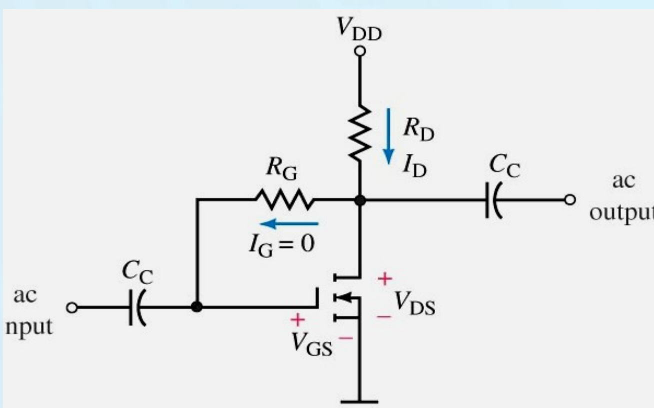
MOSFETs



MOSFETs

- Handling precautions
  - Subject to damage by electrostatic charges
  - Packaged in static resistant bags
  - Handle at static safe workstation
  - Use grounded wrist strap

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Troubleshooting a Transistor Circuit

- Ensure correct biasing
- Measure V_{BE}
- Determine V_{CEQ} and I_{CQ}
- Determine I_{BQ}
- Calculate β